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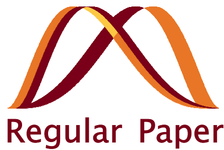

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Device Optimization of N-Channel MOSFETs with Lateral Asymmetric Channel Doping Profiles

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In this paper, we discuss design considerations for an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) with a lateral asymmetric channel (LAC) doping profile. We employed a 0.35 μm standard complementary MOSFET process for fabrication of the devices. The gates to the LAC doping overlap lengths were 0.5, 1.0, and 1.5 μm. The drain current (I_{ON}), transconductance (g_m), substrate current (I_{SUB}), drain to source leakage current (I_{OFF}), and channel-hot-electron (CHE) reliability characteristics were taken into account for optimum device design. The LAC devices with shorter overlap lengths demonstrated improved I_{ON} and g_m characteristics. On the other hand, the LAC devices with longer overlap lengths demonstrated improved CHE degradation and I_{OFF} characteristics.

Keywords: Metal–oxide–semiconductor field-effect transistor, Lateral asymmetric channel doping, Transconductance, On-state drain current, Channel-hot-carrier degradation

1. INTRODUCTION

Transconductance (g_m) and output resistance ($r_{out} = 1/g_{ds}$) of metal-oxide-semiconductor field-effect transistors (MOSFETs) are two of the most important parameters for analog applications such as amplification stages, current sinks, current sources, etc. For an amplifier, a higher g_m and r_{out} can improve the intrinsic gain ($A_v = g_m \times r_{out}$). However, it is difficult to increase both g_m and r_{out} simultaneously. The channel length of a MOSFET must be scaled down to improve g_m. Subsequently, a MOSFET with a scaled channel length does not have sufficient r_{out} due to the channel-length-modulation effect. Therefore, hardware designers usually choose a MOSFET with both a longer channel length and a wider channel width to satisfy the desired A_v. Unfortunately, this approach consumes valuable silicon area.

Up to now, several efforts have been reported for improving the g_m and r_{out} of these MOSFETs. Among them, the lateral asymmetric channel (LAC) doping profile approach provides one of the most effective ways to improve the electrical characteristics of MOSFETs [1]-[7]. For the LAC MOSFET, the doping concentration of the source side is higher than that of the drain side in the channel. Usually, a single halo ion implantation (II) has been applied to the implementation of the LAC MOSFET. The channel potential transition at the source side channel region is much steeper than those of the

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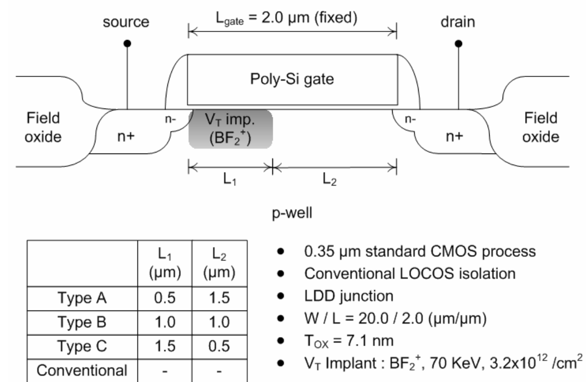
other channel regions while the device is operating due to non–uniform channel doping. Such a steep potential distribution near the source side enhances the lateral channel electric field and thus increases the carrier mobility of the devices. That is why g_m and the drain current (I_{ON}) of the transistor are typically improved in LAC MOSFETs. Physical insight into LAC devices has been presented in previous reports [1]-[3]. Recently, several circuit level considerations and the layout effects for analog and mixed-signal applications were also reported [4]-[7]. In previous literature, it has been reported that a LAC doping profile which is close to the source side can provide significantly improved electrical performance [2], [7]. Thus, a smaller tilt angle of the single halo II can drive an electrical improvement. Up to now, only a few researchers have discussed the hot carrier reliabilities of LAC devices [2], [9], [10]. However, these discussions simply compare the LAC device with conventional devices. The geometric effects of LAC doping profiles and the relationships with their hot carriers' reliabilities still need to be understood for LAC devices.

This paper presents direct current (DC) and hot carrier reliability characteristics of the LAC devices with various gates to LAC doping overlap lengths. We fabricated N-channel MOSFETs with a LAC doping profile using a 0.35 μm standard complementary metal oxide semiconductor (CMOS) logic process. In consideration of actual analog integrated circuit applications, the channel lengths of the fabricated devices were several times longer than that of the minimum design rule [5]. To form a LAC doping profile a photolithography and zero–degree II method were employed, as opposed to a single halo II method. For the fabricated LAC devices, the LAC doping positions were varied along the channel length directions. From the experimental results for DC and hot-carrier degradation, we were able to determine the relationship between the geometry of the LAC doping profile and the device characteristics.

2. EXPERIMENTS

The cross section of the fabricated devices is shown in Fig. 1. We employed a standard 0.35 μm CMOS logic process to fabricate the devices. The polysilicon gate and LAC doping II overlap lengths varied from 0.5 to 1.5 μm, while identically maintaining the other physical parameters. The channel widths (W) and lengths (L) of the fabricated devices were 20.0 and 2.0 μm, respectively. Other major process parameters are annotated in Fig. 1. The fabrication process flow of the fabricated devices was as follows. First, the conventional local oxidation of silicon was applied for device isolation on the p-type (100) silicon wafer. Second, a retrograde p–well was formed by multiple II and furnace annealing at 1000℃ for 30 min. The multiple II conditions for the retrograde p–well were: (1) boron, 400 KeV, 1.0 × 10^{13} cm^{-2}, (2) boron, 200 KeV, 1.5 × 10^{13} cm^{-2}, and (3) boron, 50 KeV, 5.0 × 10^{12} cm^{-2}. After the p–well formation, photolithography and zero–degree II for LAC doping were performed sequentially. We implemented LAC doping with 70 KeV and BF_2^+ at a dose of 3.2 × 10^{12} cm^{-2}. Then, we performed thermal gate oxidation, phosphorus-doped polysilicon (150 nm), and WSi_2 deposition (120 nm) processes. The electrical gate oxide thickness was 7.1 nm. Then, self-aligned n–type lightly doped drain, oxide spacer, and n+ source/drain junctions were formed. After junction formation, we performed a deposition of polysilicon-to-metal dielectrics, contact hole formation, and the metal interconnection steps.



	L_1 (μm)	L_2 (μm)
Type A	0.5	1.5
Type B	1.0	1.0
Type C	1.5	0.5
Conventional	-	-

Fig. 1. The cross section of the fabricated lateral asymmetric channel (LAC) metal-oxide-semiconductor field-effect transistor. The LAC doping region is varied, 0.5, 1.0, and 1.5 μm, while maintaining the total device gate length.

3. RESULTS AND DISCUSSSION

We applied a two–dimensional device simulator, MEDICI [8], to gain physical insights into the fabricated devices. Fig. 2(a) shows the channel and source/drain impurity concentrations of the LAC and conventional devices, at 10 nm from the Si–SiO_2 interface. For both of these devices, all of the physical conditions were identical except for the acceptor impurity profile in the channel. The simulated potential and lateral electric field contours for the fabricated devices are shown in Figs. 2(b) and (c), respectively. The drain and gate bias conditions were 3.3 and 1.2 V, respectively. In the conventional device, the surface potential transition at the drain side was much higher than that of any other channel region and thus had a single lateral electric field peak at the drain edge. On the contrary, for the LAC devices, positions of the surface potential transitions were shifted in the source direction. These transition positions exactly coincided with the LAC impurity profiles, as shown in Fig. 2(a). All of the LAC devices had two lateral electric field peaks inside the channel because they had abrupt potential transitions, as shown in Figs. 2(b) and (c), we expected that the channel carriers of the LAC devices would have additional acceleration near the source side as compared to those of conventional devices. Thus, g_m of the LAC device should be higher than that of the conventional device. For the three LAC devices shown in Fig. 2(c), the lateral electric field peaks inside the channel had almost identical magnitudes, although the positions were variable. In other words, from Fig. 2(c), we expect that the type-A device would have the fastest channel carriers among the LAC devices because the electric field peak was placed much closer to the source junction. Note that channel carriers of the type-A

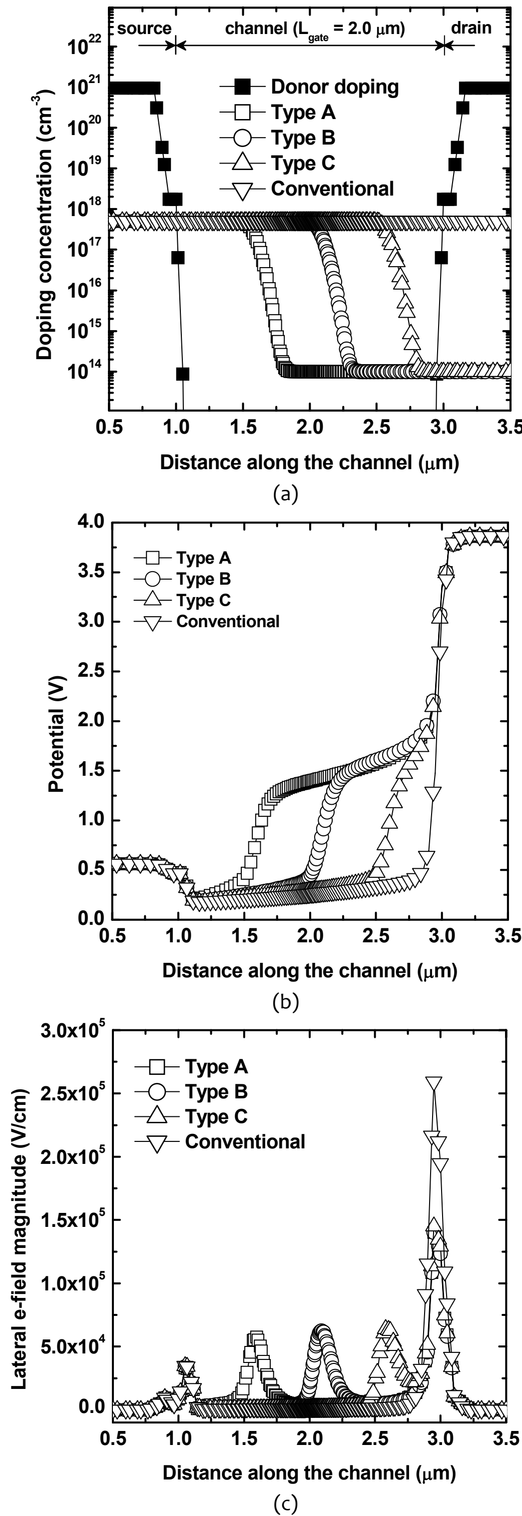


Fig. 2. The two–dimensional device simulation results. (a) Impurity concentrations in the channel and source/drain regions of four different types of transistors. (b) Potential distribution. (c) Lateral electric field. The cross section is taken at 10 nm below the Si/SiO_2 interface. Bias conditions are V_{DS} = 3.3 V and V_{GS} = 1.2 V.

device can be accelerated earlier than those of other LAC devices. Therefore, the I_{ON} of a type-A device should be superior to those of any other device.

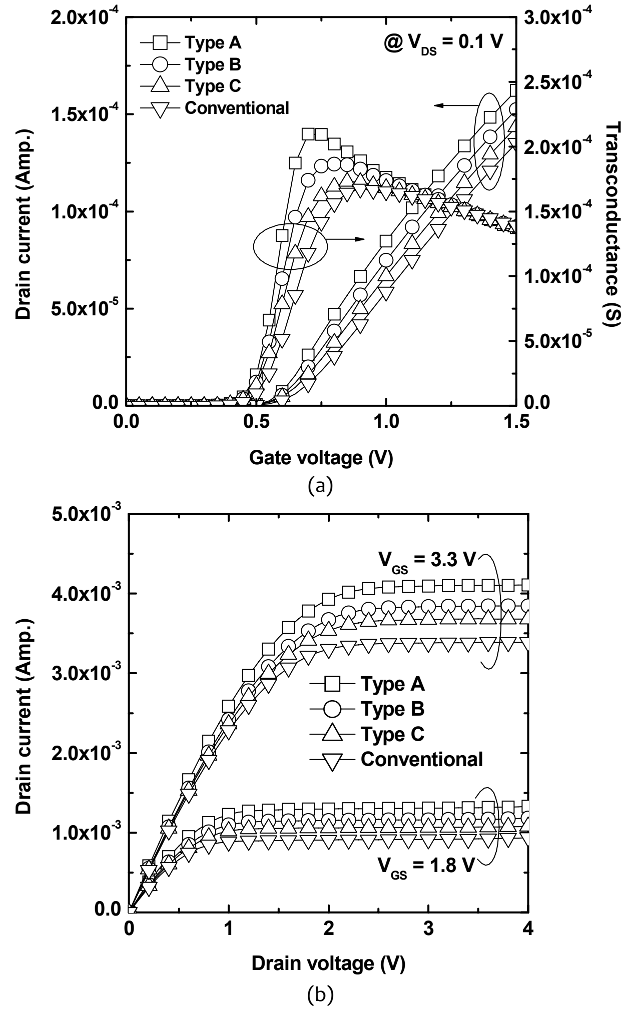


Fig. 3. (a) $I_D - V_{GS}$ characteristics of the fabricated devices (V_{DS} = 0.1). (b) $I_D - V_{DS}$ characteristics for different gate biases (V_{GS} = 1.8 and 3.3 V).

Figure 3(a) shows I_{ON} and g_m versus the gate voltage of the fabricated devices at a triode regime (V_{DS} = 0.1 V). The measured threshold voltages, V_T, of types A, B, C, and the conventional devices as determined by the extrapolation method were 0.53, 0.54, 0.56, and 0.60 V, respectively. The conventional devices had a higher V_T than did the LAC devices because the total amount of impurity in the channel affects V_T. In this manner, type A had a slightly lower V_T than did the other LAC devices. Also in Fig. 3(a), the maximum g_m and the drain current of the LAC were always higher than those of the conventional devices. In addition, the type A device had enhanced g_m curves as compared to those of the type B or type C devices. Fig. 3(a) demonstrates that g_m and the drain current of the LAC devices strongly depend on the LAC II position. When the LAC doping position was closer to the source side, g_m, then the drain current of the device was improved. This dependency can be also seen in Fig. 3(b). Additionally, Fig. 3(b) shows the I_{DS}–V_{DS} characteristics of the fabricated devices. The type A device showed a superior

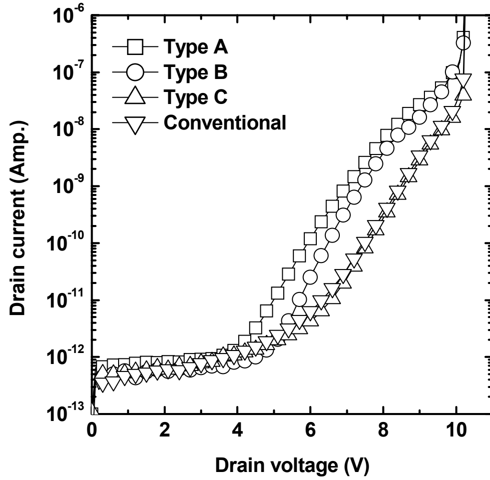


Fig. 4. The breakdown characteristics of the fabricated lateral asymmetric channels and the conventional device.

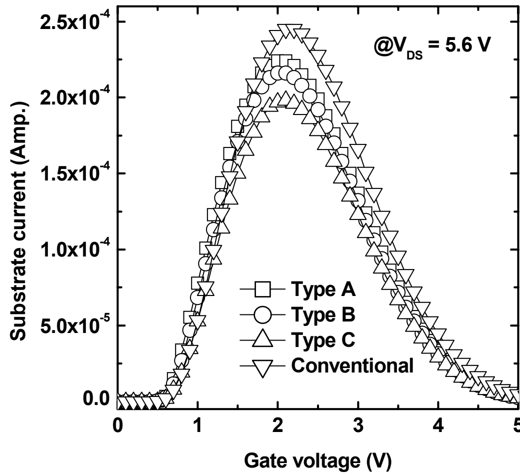


Fig. 5. I_{SUB} *vs.* V_{GS} characteristics of the fabricated lateral asymmetric channels and the conventional device (V_{DS} = 5.6 V).

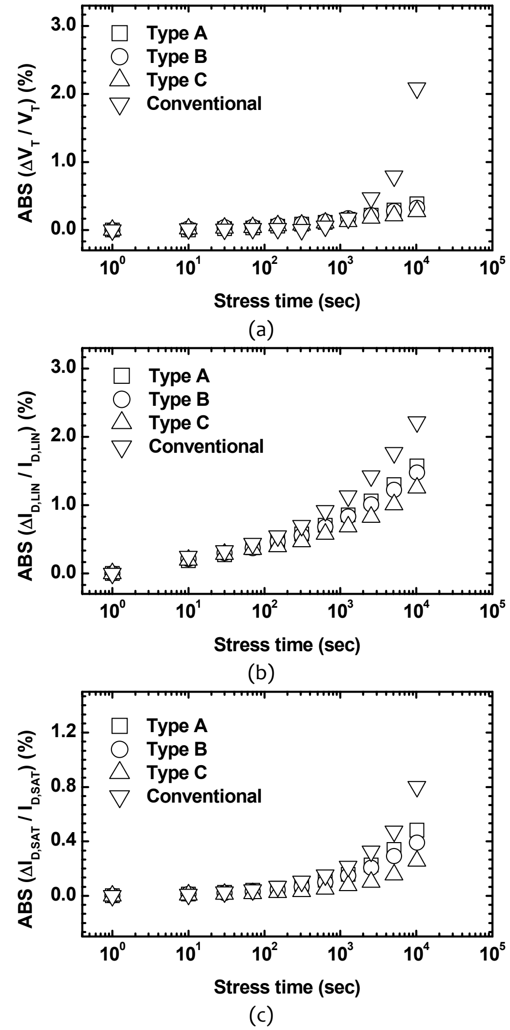


Fig. 6. Channel hot carrier degradation characteristics of the fabricated lateral asymmetric channels and the conventional device. (a) V_T . (b) $I_{D,LIN}$. (c) $I_{D,SAT}$. Stress conditions are V_{DS} = 5.6 V and V_{GS} = maximum $I_{D,SUB}$ at a given V_{DS} .

drain current driving capability than those of any of the other devices, for both saturation and triode regimes. More specifically, the drain current of the type A device was about 21 and 41% higher than those of the conventional device for V_{GS} , being equal to 3.3 and 1.8 V, respectively (V_{DS} = 4.0 V). From Figs. 3(a) and (b), the LAC doping position toward the source side has a positive effect on both g_m and the drain current driving. The previous two-dimensional device simulation results, as shown in Figs. 2(b) and (c), confirm these experimental results.

Fig. 4 shows the breakdown characteristics of the fabricated devices. For all devices, there was no significant difference in the drain leakage current (I_{OFF}) characteristics up to 4.0 V or for the junction breakdown voltages (approximately 10 V). However, the type A device had a higher I_{OFF} value in the 4.0 to 10.0 V range when compared with those of the other devices. This characteristic can be explained by the LAC doping impurity area. Both the type C and the conventional devices showed almost identical I_{OFF} characteristics because of a sufficiently wide LAC doping profile. However, for the type A device, the LAC doping impurity was confined close to the source junction. That is why the type A device had a slightly higher I_{OFF} characteristic, as shown in Fig. 4.

Fig. 5 shows the substrate currents (I_{SUB}) versus the gate voltages of the fabricated devices under an identical bias condition (V_{DS} = 5.6 V). From this figure, the I_{SUB} peak of the conventional device was higher than the peaks of the other LAC devices. This is because the conventional device had an abrupt electric field distribution at the drain junction edge; the two-dimensional device simulation results shown in Fig. 2(c) confirmed this. For the three LAC devices in Fig. 5, type A and type C devices showed the highest and lowest I_{SUB} , respectively. This I_{SUB} tendency can be explained by the drain current under the saturation regime. From Fig. 3(b), the type A device showed higher drain current driving characteristics than did the other LAC devices. Usually, a larger

drain current generates more hot carriers under a saturation regime. That is why the type A device had a higher I_{SUB} than those of the other LAC devices.

Figure 6 shows hot-carrier degradation characteristics of the four fabricated devices. Degradations of V_T, the drain current at the triode ($I_{D,LIN}$), and the drain current at saturation ($I_{D,SAT}$) regimes are shown in Figs. 6(a)-(c), respectively. The devices were subjected to electrical stress for 10,230 seconds, with measurements being taken at ten different points. The drain and gate stress voltages were chosen as 85% of the breakdown voltage and the maximum I_{SUB} of the given drain stress voltages, respectively. In Fig. 6, the conventional device shows the worst characteristics for the three parameters among the four fabricated devices. The hot carrier degradation of the conventional device can be explained by a lateral electric field distribution and the I_{SUB} characteristics in the previous figures. For the three LAC devices, the type A and C devices had the weakest and strongest resistances of hot carrier degradation, respectively. This tendency is clearly shown in Figs. 6(b) and (c), the degradation characteristics of $I_{D,LIN}$ and $I_{D,SAT}$, respectively. These results can be explained by the substrate currents shown in Fig. 5. In Fig. 5, the peak substrate current of the type A device is higher than those of the type B or C devices. It is apparent that hot carrier reliability, as well as DC characteristics, must be taken into account for optimal device design. From these experiments, we find that hot carrier degradation characteristics of an LAC device can be affected by the gate to LAC doping overlap length. Therefore, the gate to LAC doping overlap length must be carefully considered for an optimum device lifetime. It is possible that designing an LAC device with a shorter gate to LAC doping overlap length will enhance the DC electrical characteristics. For a hot carrier lifetime, however, the LAC device with a longer gate to LAC doping overlap length needs to be considered.

4. CONCLUSIONS

We discussed device optimization of LAC devices with various doping profiles. N–channel MOSFETs with a LAC doping profile were fabricated using the 0.35 μm standard CMOS process. The gate and LAC doping overlap lengths of the fabricated devices were varied from 0.5 to 1.5 μm, while maintaining other physical parameters as constant. All of the fabricated LAC devices showed improved DC and hot carrier degradation characteristics as compared to those of the conventional device. Among the LAC devices, the device with a shorter gate to LAC doping overlap length showed better g_m and I_{ON} characteristics. The devices with longer LAC doping overlap lengths showed improved I_{OFF}, I_{SUB}, and hot carrier degradation characteristics. This study demonstrates that the optimization of LAC devices accounts for hot carrier degradation as well as the DC characteristics.

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