VLSI Implementation of Auto-Correlation Architecture for Synchronization of MIMO-OFDM WLAN Systems

Jongmin Cho*, Jinsang Kim, and Won-Kyung Cho****

Abstract—**This paper presents a hardware-efficient auto-correlation scheme for the synchronization of MIMO-OFDM based wireless local area network (WLAN) systems, such as IEEE 802.11n. Carrier frequency offset (CFO) estimation for the frequency synchronization requires high complexity auto-correlation operations of many training symbols. In order to reduce the hardware complexity of the MIMO-OFDM synchronization, we propose an efficient correlation scheme based on time-multiplexing technique and the use of reduced samples while preserving the performance. Compared to a conventional architecture, the proposed architecture requires only 27% logic gates and 22% power consumption with acceptable BER performance loss.**

Index Terms—**CFO, OFDM, MIMO, VLSI**

I. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) is an effective transmission technique for various wireless communications such as wireless local area network (WLAN), for IEEE 802.11a/g/n standards, since it is robust in multi-path propagation. Also, MIMO-OFDM techniques have been considered the most promising technique for next generation communications, since it provides high data rates and spectral efficiency in multi-path fading channels. However, OFDM and MIMO-OFDM systems are known to be sensitive to synchronization errors, which may introduce inter-carrier-interference (ICI) and inter-symbol-interference (ISI) [1].

The hardware complexity of MIMO-OFDM based synchronization subsystem is linearly increased by the number of antennas [2]. Therefore, the development of an efficient synchronization scheme is one of the main issues for a practical MIMO-OFDM transceiver design. However, to our knowledge, researches of the hardware oriented MIMO-OFDM synchronization scheme have not been done actively. Although, in [2], simple MIMO extension of single-input single-output (SISO) based OFDM synchronization for IEEE 802.11n is presented, it does not provide the significant improvement of the synchronization performance and the complex multipliers and delay registers for auto-correlation are increased by the number of receiving antennas. We have reviewed previous researches of synchronization-related hardware designs for SISO based OFDM [3-5]. For all the subsystems of the synchronizations, an efficient correlation scheme is commonly required. In order to develop lower complex correlation schemes, the samples and their bit-width reduction techniques for the correlation can be employed [3, 4]. However, these techniques are not suitable to the auto-correlation of CFO estimation, since the CFO estimation requires precise correlation value while timing synchronization requires only the argument of a maximum correlation value [3]. In addition, since OFDM system is more sensitive to CFO than timing synchronization error, we may not use the sample reduction technique in SISO-OFDM WLAN system without sacrificing CFO performance. In contrast, for MIMO-OFDM based WLAN system, since the receiver diversity is improved by the multiple antennas, the sample reduction technique can be employed.

In this paper, we propose a hardware-efficient auto-

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correlation scheme for the CFO estimation of MIMO-OFDM based WLAN systems. In order to reduce the complexity of the system, we propose a scheme to use sample-reduced auto-correlation and time-multiplexing technique. While preserving the performance, the proposed scheme only requires 27% gate counts and 22% power consumption over a conventional scheme. Also, by using the time-multiplexing technique, the hardware utilization of complex multiplier in auto-correlation scheme is reached to 100%.

This paper is organized as follows. In Section II, we describe the system model, and the hardware-efficient auto-correlation scheme is presented in Section III. In Section IV, we evaluate the VLSI implementation results and finally, we conclude the paper in Section V.

II. SYSTEM MODEL

To provide both backward compatibility and high throughput in IEEE 802.11n, three preamble formats are defined [6]: Non-HT (high throughput) mode (legacy mode), HT mixed mode that consist of legacy and HT preamble, and HT Greenfield mode for high data rates. In this paper, we only consider legacy preamble of IEEE 802.11n standard for the proposed architecture. It is almost same as a physical layer convergence procedure (PLCP) preamble of IEEE 802.11a as shown in Fig. 1.

In general, the latter parts of 10 repeated short training symbols (STS) are used for symbol timing synchronization and coarse CFO estimation, and two long training symbols (LTS) with guard interval (GI2) are used for fine CFO estimation and channel estimation. For simulations, the proposed scheme is set to 4 × 4 space-time block code (STBC)-OFDM, and the multi-path channel models is TGn channel model 'D' in [7] which is typical office environment with 50 ns delay spread.

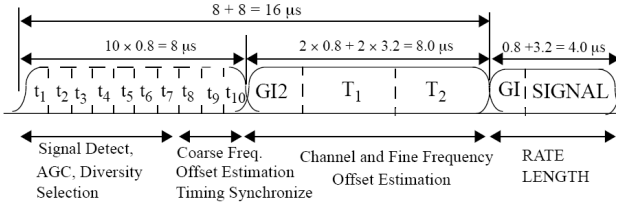

Fig. 1. PLCP preamble of IEEE 802.11a.

III. HARDWARE-EFFICIENT AUTO-CORRELATION SCHEME

1. Related Works

The synchronization block in packet mode OFDM system such as WLAN performs frame detection, CFO estimation, symbol timing synchronization. Although numerous synchronization algorithms for OFDM and MIMO-OFDM have been investigated, auto-correlation based synchronization is the most promising method, since it can be commonly used for frame detection, symbol timing synchronization and CFO estimation with moderate hardware complexity [1-5]. Therefore, a hardware efficient auto-correlation scheme needs to be developed for the CFO estimation of MIMO-OFDM systems. The main issue of the auto-correlation is the optimization of the scheme while reducing the number of samples and their bit-widths [3, 4]. The key idea of these techniques is that the frame detection and timing synchronization only require the argument of the maximum correlation value, whereas CFO estimation requires precise correlation value itself. Therefore, frame detection and coarse timing synchronization can use the sample and bit-width reduction technique with acceptable performance degradation. In contrast, as mentioned in [3], the above sample and bit-width reduction techniques cannot be used in auto-correlation for CFO estimation. This is because the CFO estimation needs precise correlation value, not the argument, and the effect of CFO in OFDM systems is more sensitive than that of timing synchronization error. Therefore, for CFO estimation, full bit-width operation and the data shifting of delay register are usually required for every clock cycle in order to avoid performance degradation. In [4], only system PER of the sample reduction technique based scheme is discussed. However, the performance degradation of CFO estimation may be greater than timing synchronization error. We should consider the performance degradation when we apply the sample reduction technique to CFO estimation. Thus, the target application in [4] is limited to ultra-wideband (UWB) which only considers QPSK modulation. WLAN systems require 16-QAM and 64-QAM modulation to achieve high data rate. Therefore, the performance loss should be taken into account when various modulation modes are

used. From VLSI implementation point of view for the CFO estimation block, we need to develop a low complex auto-correlation scheme, since first-in first-out (FIFO) based delay registers for the auto-correlation takes high complexity in MIMO OFDM systems.

2. Sample Reduction Technique and Analysis for MIMO-OFDM based WLAN

In OFDM system, the auto-correlation is used to calculate the phase difference between two successive training symbols to estimate CFO value [1-5]. For MIMO system, these auto-correlation values can be simply combined using a maximal-ratio combining (MRC) which provides better performance because of improved receiver diversity [1]. In MIMO-OFDM WLAN system, the auto-correlation and the CFO estimation are defined as expressed in (1) and (2), respectively.

$$A(n)=\sum_{j=1}^{N_r}\sum_{k=0}^{L_x-1} r_j(n+k)r_j^*(n+k-L_x) \tag{1}$$

$$\varepsilon=\frac{N}{2\pi L_x}\tan^{-1}\left(\frac{\mathrm{Im}\{A(n)\}}{\mathrm{Re}\{A(n)\}}\right) \tag{2}$$

where N_r is the number of receive antenna, L_x is the length of short and long training symbol, 16 and 64, respectively. N is an FFT size, ε is normalized CFO value. In [5], even though the delay registers for coarse CFO estimation (16 samples) and fine CFO estimation (64 samples) are shared for efficient design of a conventional SISO based WLAN, IEEE 802.11a, at least 64 delay registers are required for real and imaginary part, respectively. When the number of receiving antenna, N_r, is 4, 256 delay registers are required for IEEE 802.11n legacy preamble, extension of 802.11a preamble, in order to perform the auto-correlation in (1). An example of the straight-forward implementation of (1) without architectural transformation is shown in Fig. 2.

From the analysis of auto-correlation schemes, we can easily see that the high complexity block in auto-correlation is the FIFO based delay shift register. By increasing the number of receiving antennas in MIMO systems, the delay registers at each RX branch will be increased multiplicatively. To solve this problem, we propose a MIMO architecture requiring the almost same hardware complexity as SISO systems with reasonable performance loss. By keeping the system performance as SISO performance, the proposed architecture can use the fixed number of the delay registers regardless of the number of the receiving antennas. The proposed method is expressed as follows.

$$A(n)=\sum_{j=1}^{N_r}\sum_{k=0}^{\lfloor L_x/N_r\rfloor-1} r_j(n+k)r_j^*(n+k-L_x). \tag{3}$$

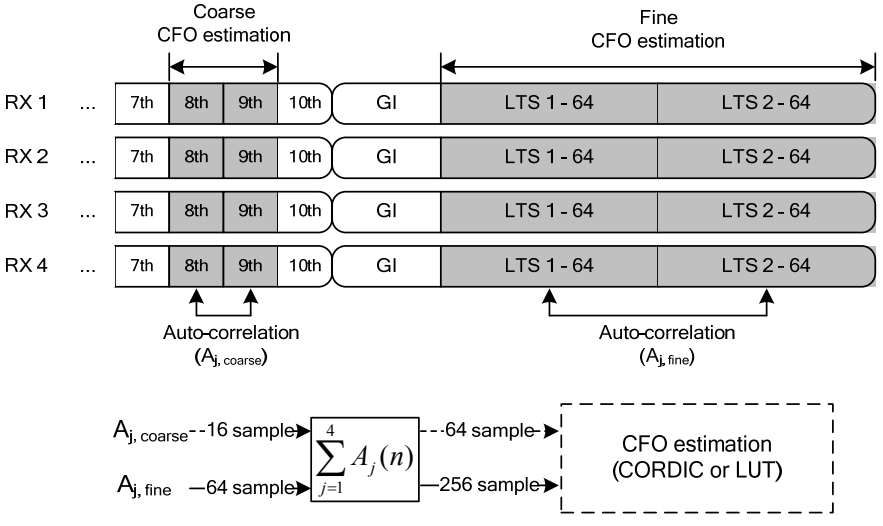

Fig. 2. Auto-correlation method of 256 sample-based scheme in (2).

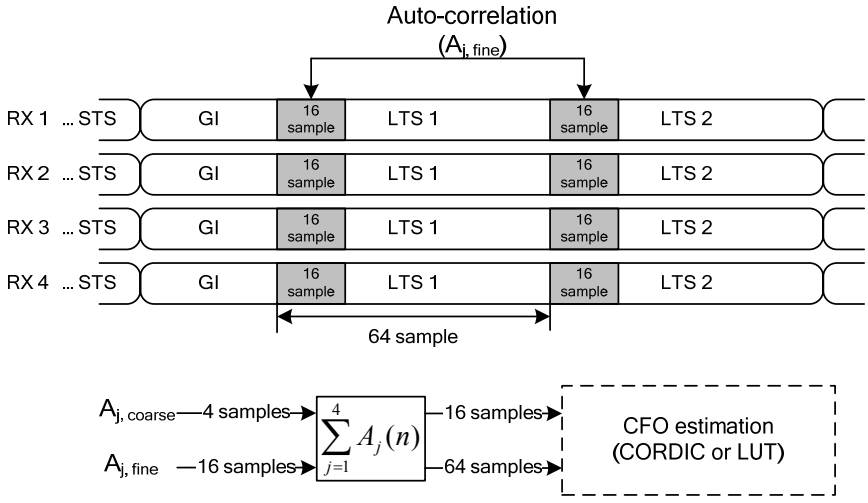

Fig. 3. Auto-correlation method of sample reduction technique in (4).

In (3), we can easily see that the number of the multiplications and delay registers are reduced by 75% when N_r is 4. Compared to the architecture of (1), the number of delay registers is reduced to be $1/N_r$. The proposed auto-correlation block diagram for fine CFO estimation is shown in Fig. 3. The auto-correlation for coarse process is the same as the fine process except the number of samples.

For the performance evaluation of the 64 sample-based proposed scheme in (3) and the 256 sample-based scheme in (1), we simulate and compare the two schemes in terms of mean square error (MSE) and bit error rate (BER) parameters as shown in Fig. 4 and Fig. 5, respectively. As shown in Fig. 4, the conventional scheme outperforms the proposed scheme in terms of MSE performance since it is robust to noises. This is because more samples are used in the auto-correlation, which means the improvement of the receiver diversity by MIMO antennas. However, the performance loss of the proposed scheme in terms of BER is not large as shown in Fig. 5. It is less than 1 dB for all modulation modes, QPSK, 16-QAM and 64-QAM. This is because even though the MSE performance of the proposed 64 sample-based scheme is worse than the 256 sample-based scheme in (1), the proposed scheme provides the same performance as SISO system and it is enough to

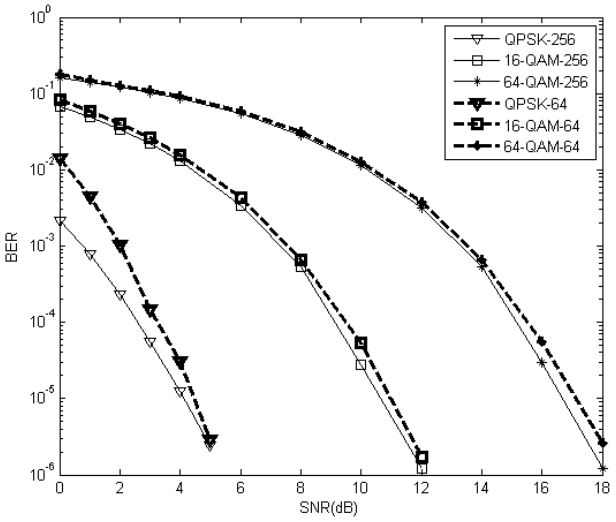

Fig. 4. BER performance of STBC-OFDM with 256- and 64-smaple based CFO estimation.

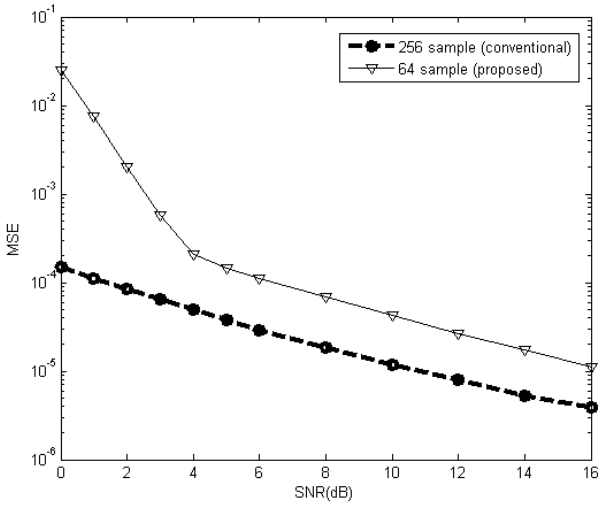

Fig. 5. MSE performance of CFO estimation for MIMO-OFDM.

achieve similar performance in terms of BER. It means that if we use more samples for the CFO estimation of MIMO systems, we cannot expect much performance improvement.

3. Time-Multiplexing Architecture

Fig. 3, we can see that only first 16 samples are correlated at each RX branch even if the LTS is 64 samples long. It means that the hardware utilization efficiency of the complex multiplier in auto-correlation scheme is only 25%. For more efficient implementation, we propose a folding method, a time-multiplexing architecture with which we can achieve the hardware utilization of 100% by sharing the complex multiplier. The details are shown in Fig. 6 and Fig. 8. From T1 to T4 in Fig. 6, auto-correlation is performed for coarse CFO estimation by using STS, and from T5 to T8 is done for fine CFO estimation. As mentioned above, each RX branch has different timing duration for auto-correlation, hence AC block in Fig. 8 that consists of complex multiplier, pipeline adder and conjugating block will be occupied sequentially. Therefore, AC block can be shared with all RX branches. The proposed algorithm with time-multiplexing technique is expressed as

$$A(n)=\sum_{j=1}^{N_r}\sum_{k=\left((j-1)\cdot\left\lfloor\frac{L_x}{N_r}\right\rfloor\right)}^{\left(\left\lfloor\frac{L_x}{N_r}\right\rfloor\cdot j-1\right)}\left(r_j(n+k)r_j^*(n+k-L_x)\right). \quad (4)$$

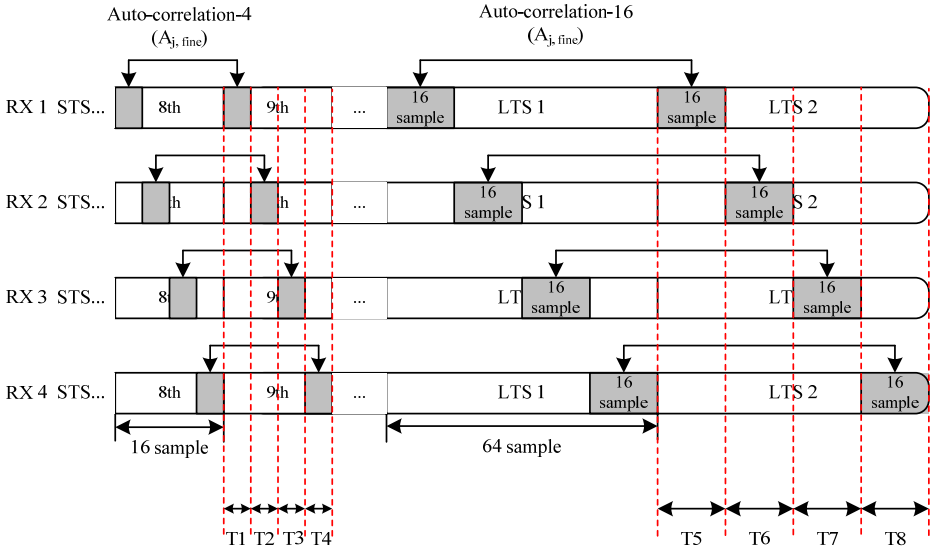

Fig. 6. The proposed time-multiplexing based auto-correlation diagram.

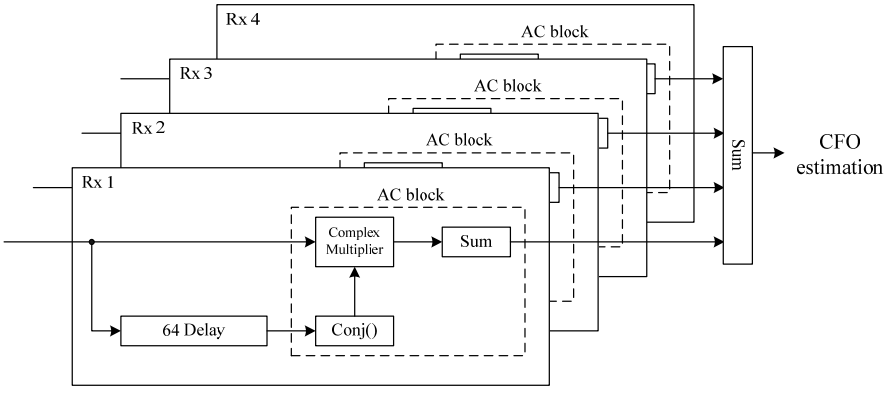

Fig. 7. Implementation example of (2) with 4 RX.

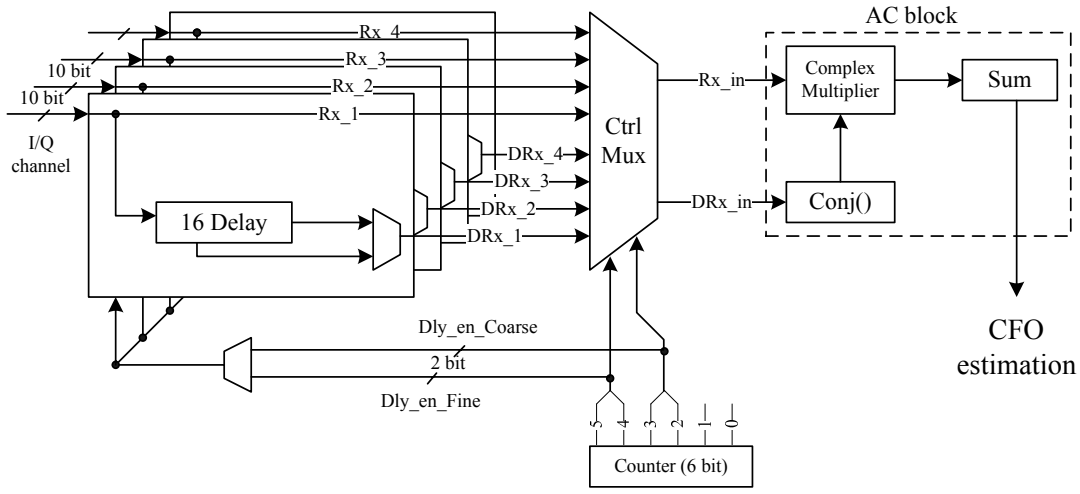

Fig. 8. Proposed time-multiplexing architecture with 4 RX.

The correlation timing depends on receiving antenna index *j* and the number of sample for correlation is the same for all RX branches. Regardless of the number of receiving antenna, the hardware complexity of the proposed architecture is almost equivalent to SISO case. In Fig. 7, each RX branch has an auto-correlation scheme consisting of 64 delay registers and an AC block. The proposed architecture in Fig. 8 has four 16 delay registers and only one AC block. Even though the proposed architecture has some control blocks, i.e. MUXs and a counter, these overheads are not high. As shown in Fig. 8, the proposed architecture controls time-multiplexing by the 6 bit counter with several control signals. I/Q channel signals are 10 bit. The delay enable signals, Dly_en_Coarse and Dly_en_Fine, are activated depending upon the tasks: fine CFO estimation and coarse CFO estimation.

IV. VLSI IMPLEMENTATION RESULTS

The complexity of the synchronization scheme depends on several factors such as synchronization algorithm, preamble size and I/O bit-width. Also, it depends on target applications or standards. Therefore, it is difficult to compare our scheme to other research works. In this paper, we compare our architecture with 4 × 4 MIMO architecture in Fig. 7. The proposed architecture is modeled using the VHDL and synthesized and manufactured using 0.18 um CMOS technology. For the synthesis and P&R, Synopsys Design Vision and Astro are used. The proposed architecture significantly reduces the gate counts around 73%. Also, the power consumption of the proposed architecture is reduced by 78%. Fig. 9 shows the layout of the synchronization scheme of 4×4 MIMO-OFDM WLAN system which employs the proposed auto-correlation algorithm. The chip implementation results are shown in Table I. The maximum clock frequency is 77 MHz. The gate count is 104K and the auto-correlation module takes 71.1% area and 81.4% power consumption.

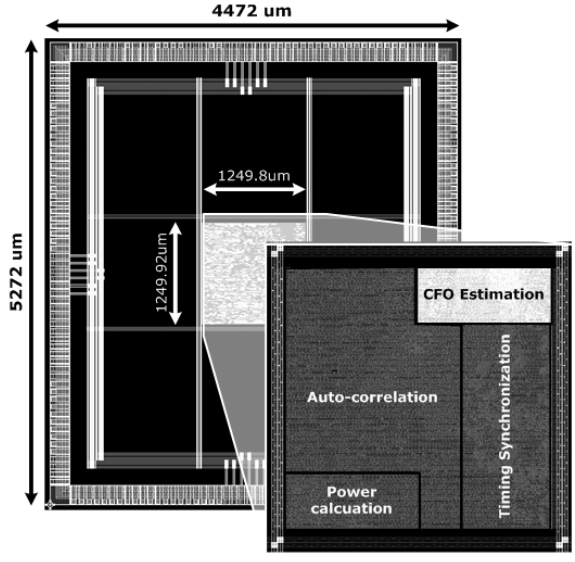

Fig. 9. Layout of synchronization scheme for MIMO OFDM-based WLAN.

Table 1. Chip imeplementation of synchronization module of MIMO-OFDM system using the proposed auto-correlation architecture

Process	0.18 um CMOS 1P5M
Package	208 MQFP
Die size	4.95×5.75 (mm^2)
Core size	1.25×1.25 (mm^2)
Max. Clock Freq.	77 MHz
Power consumption	55 mW
Gate counts	104K

V. CONCLUSIONS

In this paper, the hardware-efficient synchronization scheme for MIMO-OFDM wireless LAN standard, IEEE 802.11n, is proposed. The features of the proposed architecture are the use of sample reduction and time multiplexing techniques which utilize the diversity gain for the MIMO system. Experimental results show that our scheme provides smaller area and less power dissipation compared to the conventional architecture. Also, the proposed architecture was embedded and implemented for the synchronization module of WLAN.

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