Fabrication of Transimpedance Amplifier Module and Post-Amplifier Module for 40 Gb/s Optical Communication Systems

Jong-Min Lee, Byoung-Gue Min, Seong-Il Kim, Kyung Ho Lee, and Hae Cheon Kim

The design and performance of an InGaAs/InP transimpedance amplifier and post amplifier for 40 Gb/s receiver applications are presented. We fabricated the 40 Gb/s transimpedance amplifier and post amplifier using InGaAs/InP heterojunction bipolar transistor (HBT) technology. The developed InGaAs/InP HBTs show a cut-off frequency (f_T) of 129 GHz and a maximum oscillation frequency (f_{max}) of 175 GHz. The developed transimpedance amplifier provides a bandwidth of 33.5 GHz and a gain of 40.1 dBΩ. A 40 Gb/s data clean eye with 146 mV amplitude of the transimpedance amplifier module is achieved. The fabricated post amplifier demonstrates a very wide bandwidth of 36 GHz and a gain of 20.2 dB. The post-amplifier module was fabricated using a Teflon PCB substrate and shows a good eye opening and an output voltage swing above 520 mV.

Keywords: InGaAs/InP HBT, 40 Gb/s, transimpedance amplifier, post amplifier, module, package.

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I. Introduction

For 40 Gb/s optical communication systems, high-gain and high-bandwidth optical receivers are required [1], which inevitably require optical component modules and electrical component modules. The electrical component modules include a 40 Gb/s transimpedance amplifier and a post amplifier. A preamplifier is typically used as the input stage of the receiver in order to convert the small current from the photodiode into a voltage signal for amplification by the subsequent post amplifier [2], [3]. This stage is one of the key circuits in the optical link since it largely sets the sensitivity and maximum bit rate of the receiver. Transimpedance feedback amplifiers are commonly used as preamplifiers with low-input impedance and flat-gain characteristics. To achieve high-quality voltage signals, wideband transimpedance amplifiers have been implemented using InP/InGaAs heterojunction bipolar transistors (HBTs) technology. Because the InGaAs/InP transimpedance amplifiers allow monolithic integration with a p-i-n photo detector, these amplifiers have been widely investigated and have demonstrated excellent device and circuit performance.

A broadband amplifier is used as the post amplifier in 40 Gb/s optical fiber links; a post amplifier is needed for optical transmission systems to amplify the relatively small voltage signals into a large voltage sufficient to drive the succeeding digital circuits [4]-[6]. As the intermediate stage between a transimpedance amplifier and a clock and data recovery circuit, a post amplifier requires a high product of gain and bandwidth. A high gain is needed to make a reliable decision in the

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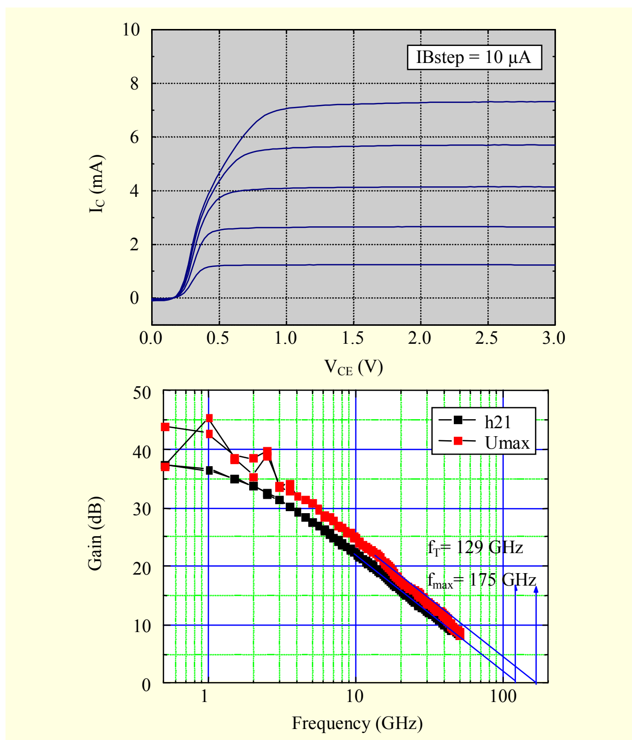

Fig. 1. Typical DC and RF characteristics of an InGaAs/InP HBT with an emitter area of 6 μm^2.

presence of system noise, and a high bandwidth is needed to pass the higher order harmonics of the rise and fall times. A post amplifier was also fabricated using InP/InGaAs HBTs and designed as general purpose gain blocks for use in 40 Gb/s optical transmission systems.

In this study, we describe the design, fabrication, and performance of a packaged 40 Gb/s transimpedance amplifier and post amplifier. The transimpedance and post amplifiers were designed and manufactured using our InP/InGaAs HBT library with an emitter width of 1 μm. The basic transistor has an area of 6 μm^2 and was fabricated using the usual triple-mesa process.

II. Fabrication of InGaAs/InP HBT and Amplifiers

The devices used in this work were grown by molecular beam epitaxy on a semi-insulating (100) InP substrate and fabricated using a triple-mesa isolation structure. Si and C were used as the *n*- and *p*-type dopants, respectively. The epi-structure was composed of an InP emitter on an InGaAs base layer with an abrupt junction. The epitaxial layer mainly consists of a 500 Å thick *n*-InP (n = 5×10^{17} cm^{-3}) emitter layer, a 500 Å thick *p*-InGaAs (p = 4×10^{19} cm^{-3}) uniform base layer, a 500 Å thick n-InGaAs/InAlAs chirp superlattice, a 3000 Å thick *n*-InP (n = 2×10^{16}cm^{-3}) collector layer, and a 4000 Å thick *n*-InGaAs (n = 2×10^{19} cm^{-3}) sub-collector layer. In this device, the passivated surfaces were the side walls of an InP emitter mesa and a highly doped *p*-type extrinsic InGaAs base layer. A silicon-nitride film was deposited using plasma-enhanced chemical-vapor deposition. The NiCr resistor and metal-insulator-metal capacitor were also integrated with InGaAs/InP HBTs. We did not adopt air-bridge or backside processing, such as wafer thinning and back-via-hole dry etching.

We measured the DC and RF characteristics using an HP semiconductor parameter analyzer, an HP 8510C network analyzer, and a cascade probe station. The eye patterns for the finally packaged broadband amplifier were measured using an Anritsu 4-channel 10-Gb/s pulse pattern generator (PPG), a digital sampling oscilloscope, and a 40 Gb/s multiplexing system. The typical DC and RF characteristics of InGaAs/InP HBTs are shown in Fig. 1. As Fig. 1 shows, the developed HBTs showed a cut-off frequency (f_T) of 129 GHz and a maximum oscillation frequency (f_{max}) of 175 GHz with a collector current of 7 mA. The extracted device parameters were modeled to fit the measured characteristics using simulators over the bias conditions of the HBT in the circuit.

III. Characteristics of Transimpedance Amplifier Module

We designed a common-base transimpedance amplifier composed of four stages: an input stage, gain stage, emitter-follower buffer stages, and a 50 ohm impedance matching stage. Figure 2 shows a schematic of the fabricated transimpedance amplifier. To exploit the high responsivity performance of the photodiode-transimpedance amplifier optical receiver, a common-base transimpedance amplifier was fabricated. The common-base transimpedance amplifier buffers the transimpedance amplifier from the high-impedance photo detector and improves the bandwidth [7]. The input signal current is amplified by the common emitter gain stage. The feedback network, which consists of a resistor, stabilizes the transimpedance gain. The feedback resistance is 700 ohm, and the single supply voltage is 3.3 V. The overall chip layout was designed to minimize the signal path from the input pad to the output pad. The chip size, including electrode pads for on-wafer measurement and packaging wire bond, is 0.675 mm × 0.525 mm for the transimpedance amplifier. RF signal pads for single input and output are configured into a ground-signal-ground (GSG) type with 150 μm pitch on the left and right sides, respectively, for RF on-wafer probing.

The transimpedance gain extracted from simulated S-parameters is about 40.1 dBΩ, and a 3 dB bandwidth of 33.5 GHz is achieved by using a capacitance peaking technique [8]. A peaking capacitor is used to increase the

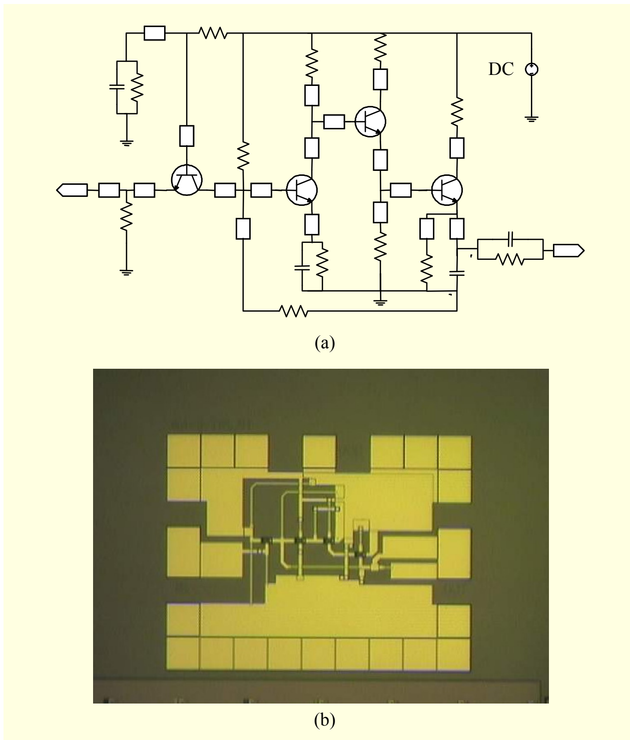

Fig. 2. Schematic diagram and photograph of a transimpedance amplifier.

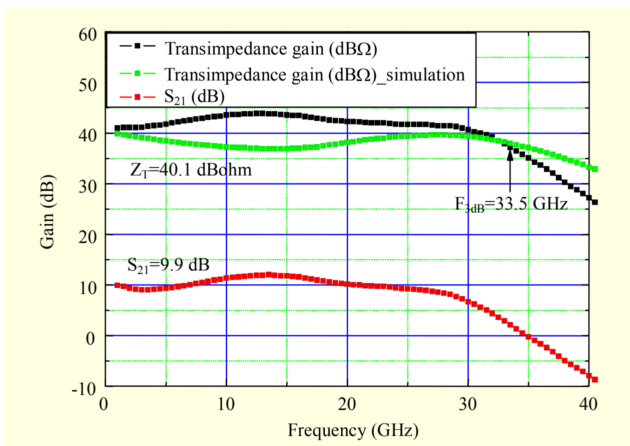

Fig. 3. Measured transmission coefficient S_{21} and tramsimpedance gain of a transimpedance amplifier.

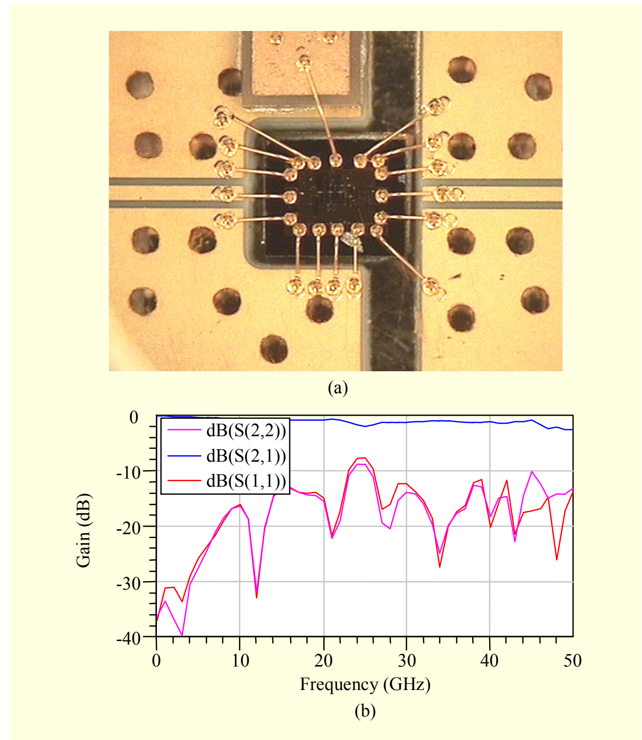

Fig. 4. (a) Photograph of wire-bonded transimpedance amplifier mounted on a ceramic substrate and (b) measured small signal response of the packaging components.

overall bandwidth transimpedance amplifier. In this work, we carried out a circuit simulation including loss by transmission lines in the circuit. When we considered the line effect, the transimpedance gain of the transimpedance amplifier was reduced as the frequency was increased. The effective transimpedance gain without a photo detector was measured on-wafer using coplanar probes.

The transimpedance amplifier exhibited an S_{21} gain of 9.9 dB, and S_{22} was less than –5 dB over a frequency range of less than 40 GHz. The transimpedance gain ripple was about 3.7 dB, and measured group delay was about 44 ps. The power dissipation was 82.5 mW with a single voltage supply of 3.3 V. These characteristics make the transimpedance amplifier suitable for use in a high-speed optical receiver.

For packaging processes, the whole wafer was sliced into separate chips. Each chip was mounted on a patterned ceramic substrate and wire bonded and assembled in an Au-plated metal case with SMA connectors for input and output ports. Figure 4(a) shows the assembled transimpedance amplifier module and Fig. 4(b) shows the small signal response of the packaging components, including the ceramic substrate, housing, connector, and wire-bonding. A low electrical return loss over a wide frequency range and an insertion loss of 1.5 dB at 40 GHz were achieved. To reduce the parasitic loss, the ceramic substrate had a hole and slot. By mounting the transimpedance amplifier in the hole, the wire length was minimized, and by adopting a substrate slot structure, the in-out coupling was suppressed. We fabricated transimpedance amplifier modules as shown in Fig. 5(a). To measure the eye-diagram, we made a 40 Gb/s NRZ signal by multiplexing 4-channel 10 Gb/s PPG signals (pseudorandom binary sequence 2^{31}–1). As shown in Fig. 5(b), the 40 Gb/s NRZ eye diagrams of the finally packaged transimpedance amplifier show a clear eye with a pattern of 146 mV for an input of 50 mV with rise and fall times of less than 10 ps.

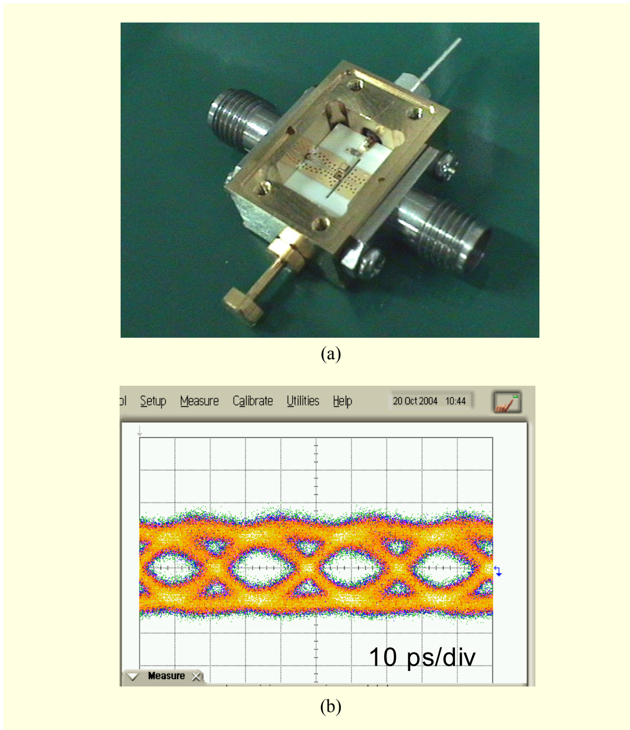

Fig. 5. (a) Photograph of a fabricated transimpedance amplifier module and (b) measured 40 Gb/s NRZ eye diagrams.

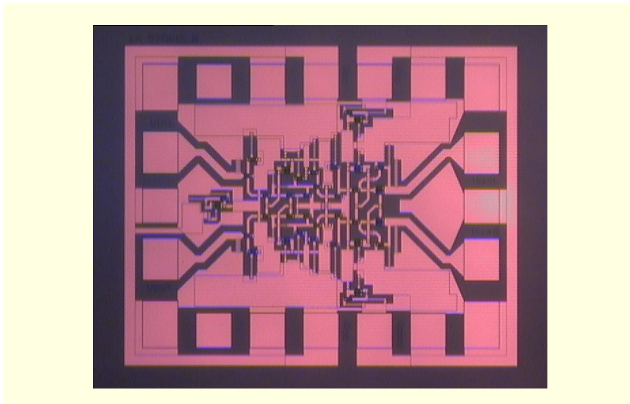

Fig. 6. Photograph of a post amplifier.

IV. Characteristics of Post-Amplifier Module

The post amplifier had a two-stage differential design. The two differential stages were coupled with emitter followers to transform the impedance and to shift the DC level. A differential operation was applied to reduce the time jitter and crosstalk. The overall chip layout was designed to keep the symmetry between differential signals to reduce the offset.

The chip size, including electrode pads for on-wafer measurement and the packaging wire bond, was 1.0 mm × 0.9 mm. Figure 6 shows a photograph of the post amplifier. RF signal pads for the differential input and output were configured into a

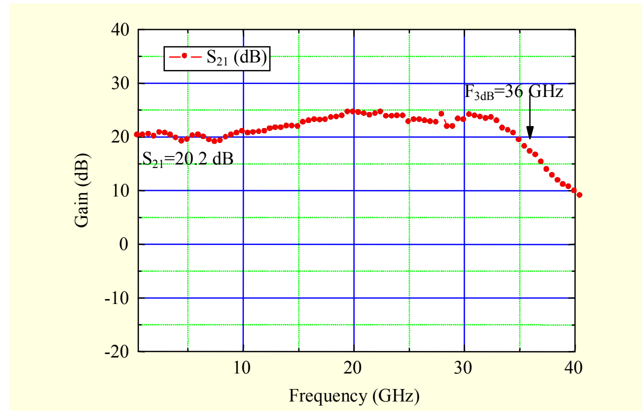

Fig. 7. Measured transmission coefficient S_{21} of a post amplifier.

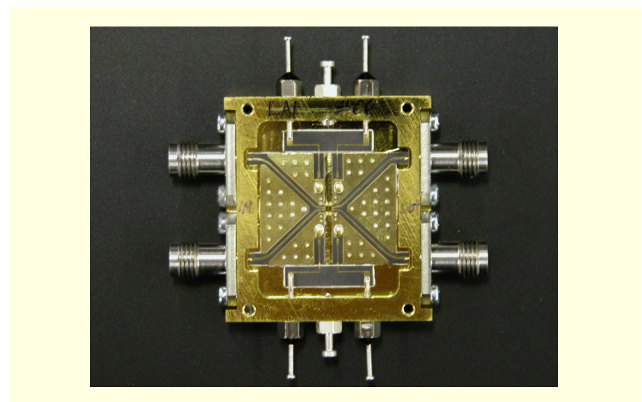

Fig. 8. Photograph of a fabricated post-amplifier module.

signal-ground-signal type with a 150 µm pitch on both the left and right sides. Large ground and power supply areas were used to obtain a low impedance and large capacitance. The circuit is composed of an input buffer, a two-stage amplifier, and an output buffer. The output buffer supplies constant differential voltages above 500 mV through a 50 ohm output resistor.

Figure 7 shows the gain bandwidth characteristics for the post amplifier. The fabricated amplifier exhibited a 36 GHz bandwidth with a single-ended 20.2 dB small-signal gain and an overall differential gain above 25 dB when the bias voltage was –4.9 V.

For packaging processes, the entire wafers were lapped, Au was evaporated onto the back side, and the wafers were sliced into separate chips. The chips were mounted onto a patterned board, wire bonded, and assembled in an Au-plated metal case with V-connectors. We adopted a Teflon PCB substrate for low cost application. The Teflon PCB substrate was 5 mils thick and was patterned using 0.5 ounce copper.

The GSG coplanar line between the post amplifier pad and V-connector was a patterned coplanar waveguide transmission line with 50 ohm characteristic impedance. Ground vias of

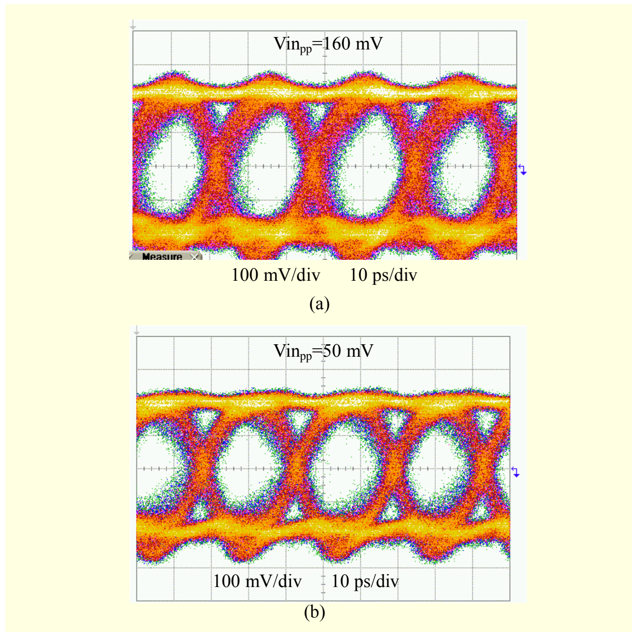

Fig. 9. 40 Gb/s NRZ eye diagrams of a post amplifier with input voltage swings of (a) 160 mV and (b) 50 mV.

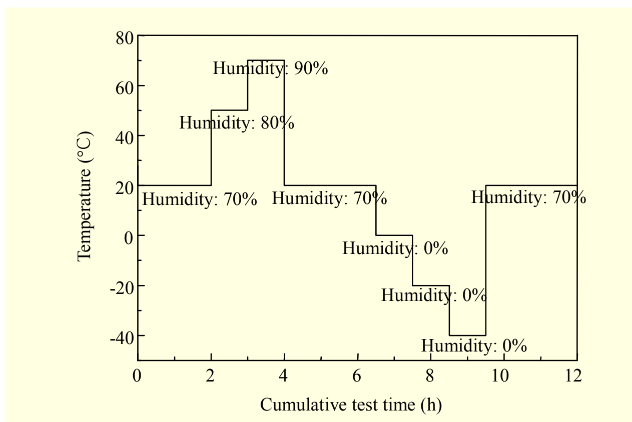

Fig. 10. Temperature and humidity test cycle for a post-amplifier module.

3 mm in diameter were designed to connect the top grounds to the back metallization. We used 100 pF single-layer capacitors and 10 nF multi-layer capacitors to bypass RF signals in the DC bias line. Figure 8 shows the assembled post-amplifier module.

Figure 9 shows the eye patterns for a post-amplifier module measured using a single-ended input voltage swing of 160 mV and a 50 mV input signal. As seen in Fig. 9, the 40 Gb/s NRZ eye diagrams of the finally packaged post amplifier show open 40 Gb/s eyes with an output magnitude above 520 mV with rise and fall times of less than 10 ps.

We conducted temperature and humidity tests of the post-amplifier module. Figure 10 shows the temperature and humidity test cycle. As seen in Table 1, there is no remarkable gain variation or abnormal current flooding during the test cycle, which confirms the reliability of the fabricated post-amplifier module.

Table 1. Gain variation of a post amplifier during temperature and humidity tests.

Stage	Temperature (°C)	Humidity (%)	Cumulative test time (h)	S_{21} (40 MHz)
1	28	66	0	19.09
2	20	70	2	19.16
3	50	80	3	19
4	70	90	4	18.8
5	20	70	6.5	18.5
6	0	0	7.5	19.13
7	-20	0	8.5	19.18
8	-40	0	9.5	18.65
9	20	70	12	19.2

V. Conclusion

In conclusion, we have successfully developed a wideband transimpedance amplifier and post amplifier using InGaAs/InP HBT technology. InGaAs/InP technology is preferred for the design and fabrication of 40 Gb/s electrical components. Experimental results demonstrate a transimpedance of 40.1 dBΩ and 33.5 GHz bandwidth with S-parameters measured. The power consumption of the amplifier is 82.5 mW and the chip size is 0.354 mm^2. Transimpedance amplifier modules were fabricated using ceramic substrates and wire bonding. We applied the hole and slot structure to the substrate design to reduce parasitic loss and coupling. Eye diagram measurements for transimpedance amplifier modules were carried out at a data rate of 40 Gb/s. Clear open eye diagrams at 40 Gb/s data rates were achieved.

A post amplifier was also fabricated using InGaAs/InP HBT technology. The fabricated circuit had an S_{21} gain of 20.2 dB and a –3 dB bandwidth of 36 GHz, with an excellent eye opening for a 40 Gb/s random pattern signal. Clear 40 Gb/s eye diagrams demonstrated the good system applicability of this module. The broadband transimpedance amplifier module and post-amplifier module are adequate for 40 Gb/s optical transport network systems.

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