A Highly Efficient GaAs HBT MMIC Balanced Power Amplifier for W-CDMA Handset Applications

Unha Kim, Junghyun Kim, and Youngwoo Kwon

ABSTRACT—A highly efficient and compactly integrated balanced power amplifier (PA) for W-CDMA handset applications is presented. To overcome the size limit of a typical balanced PA, a bulky input divider is integrated into a PA MMIC, and a complex output network is replaced with simple lumped-element networks. For efficiency improvement at the low output power level, one of the two amplifiers in parallel is deactivated and the other is partially operated with corresponding load impedance optimization. The implemented PA shows excellent average current consumption of 34.5 mA in urban and 56.3 mA in suburban environments, while exhibiting very good load-insensitivity under condition of VSWR=4:1.

Keywords—Balanced power amplifier, efficiency, MMIC, small form-factor, W-CDMA.

I. Introduction

For wideband code-division multiple access (W-CDMA) systems, the efficiency of power amplifiers (PAs) operating at low output power levels has been an important issue in maximizing battery lifetime because most mobile handsets operate at output power levels below 10 dBm in urban environments [1], [2]. Moreover, PAs have recently been required to be insensitive to antenna mismatch because handsets do not include isolators due to their bulky size and cost. Of the load-insensitive PAs reported, the balanced-type PA has been preferred due to its excellent performance [3]-[5]. However, bulky components in the balanced PA, such as the input divider, input phase compensator, 3-dB output combiner, and two output-matching networks, have prevented the PA from being widely adopted for handset applications.

A highly efficient balanced PA with a simple structure for easy implementation is proposed. A highly integrated monolithic microwave integrated circuit (MMIC) and output network help the PA to be miniaturized. Programmable biasing and simple diode switches are also used to enhance efficiency at a low output power level. For comparison, a 1 W level conventional class-AB PA is also fabricated and measured.

II. Design and Implementation

Figure 1 shows a schematic of the proposed balanced PA. A phase splitter of a simple T-network is used as the input power divider and phase compensator, and it is fully integrated into the PA MMIC, including the input matching circuits except a shunt stub l_x. Four $\lambda/4$ transformers of the output 3-dB coupler can be readily replaced by lumped elements with π-networks. Note that careful design enables integration of two output-matching circuits into the output 3-dB coupler because they can all be implemented by π-networks.

Because the power-added efficiency (PAE) of the PA in low output power operation is very important, a selective biasing corresponding to the output power level can be adopted in the PA [6]. In this work, all transistors (Q1 to Q4 in Fig. 1) are activated for high output power operation above 20 dBm (high-power mode), but Q1 and just a half of Q2 of the upper amplifier are used for low output power operation below 20 dBm (low-power mode), which makes the PA programmable and more efficient. Simultaneously, load impedance adjustment is implemented with two simple PIN diode switches (D1 and D2 in Fig. 1). When the PA operates in

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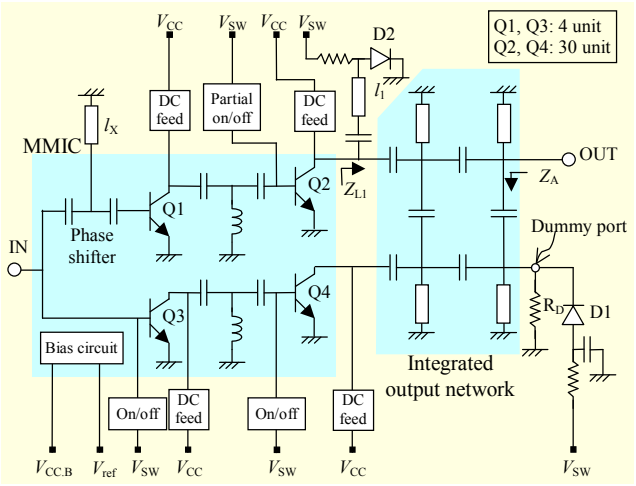

Fig. 1. Schematic of the proposed balanced PA.

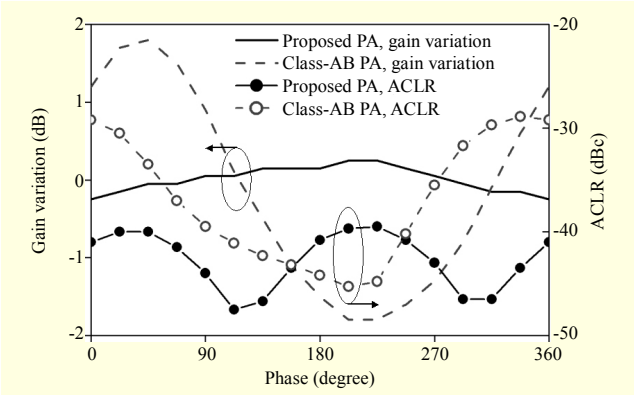

Fig. 2. Calculated gain variation and ACLR at P_{out}=24 dBm and VSWR=4:1.

low-power mode, on-state D1 brings Z_A, seen in Fig. 1, to high impedance for reducing power leakage into the dummy port, and on-state D2 modulates the load impedance (Z_{L1} in Fig. 1) to the PAE optimum impedance so as to maximize efficiency in low-power mode. On the other hand, D1 and D2 are both off in high-power mode.

To verify the load-insensitivity of the proposed PA structure, the 3GPP adjacent channel leakage ratio (ACLR) was solved using MATLAB from the simulated AM-AM and AM-PM distortion data [7]. Figure 2 shows the calculated gain variation and ACLR under a VSWR of 4:1. The output power of 24 dBm was assumed as the delivered power, and an ACLR of better than -40 dBc was observed over all phases. From the calculated data, it is expected that the proposed PA preserves its balance despite its simplified structure, and it can show good load-insensitivity under antenna mismatch.

III. Fabrication and Measurement

The MMIC was fabricated using a commercial 2-μm InGaP/GaAs heterojunction bipolar transistor (HBT) process with a size of 1.1 mm×1.08 mm. The MMIC contains two identical 2-stage amplifiers in parallel, each main-stage having an emitter area of 2,400 μm^2. The input matching network and the phase splitter except a shunt stub (l_x) were all integrated into the MMIC. Photos of the MMIC and the developed 4 mm×4 mm module are shown in Fig. 3.

For measurement, the 3GPP uplink W-CDMA signal was used with a 3.5 V supply voltage at an operating frequency of 1,950 MHz. Figure 4 shows the measured gain and ACLR. An output power of 20 dBm was selected as the switching point for two separate power operation modes. The proposed PA has power gains of around 25 dB in the high-power mode and 17 dB in the low-power mode, showing a good ACLR of better than -40 dBc up to a rated maximum power level of 27.5 dBm. Also, the circuit showed good measured results over all V_{CC} and Tx frequency range, and the PA still met the linearity requirement. As a reference, a conventional class-AB PA was also fabricated and measured. It should be noted that, as seen in Fig. 5, the PAE at 10 dBm in the low-power mode increased from 3.3% to 7.3% due to the selective biasing, maintaining the peak PAE of the proposed PA very close to that of the class-AB PA (37% at 27.5 dBm). The idle current, which has a great impact on the overall talk time, was also reduced from 65 mA to 23 mA by

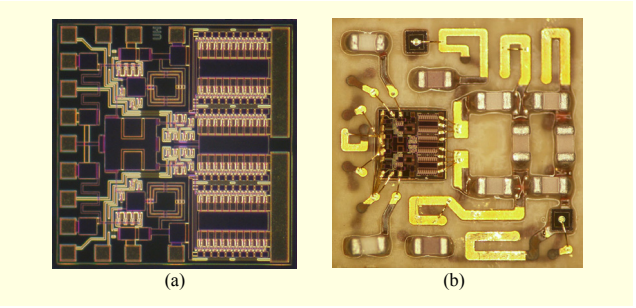

Fig. 3. Photos of (a) the fabricated MMIC and (b) the test module.

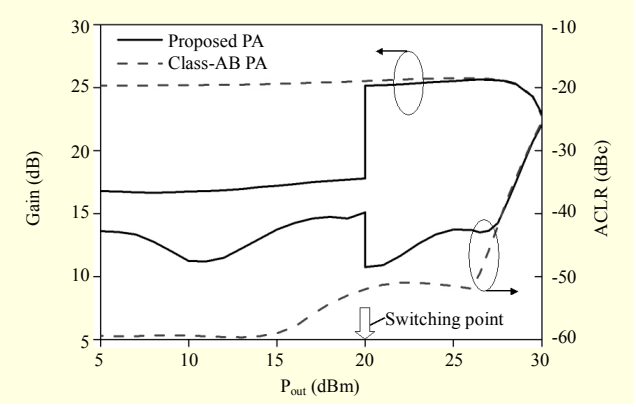

Fig. 4. Measured gain and ACLR.

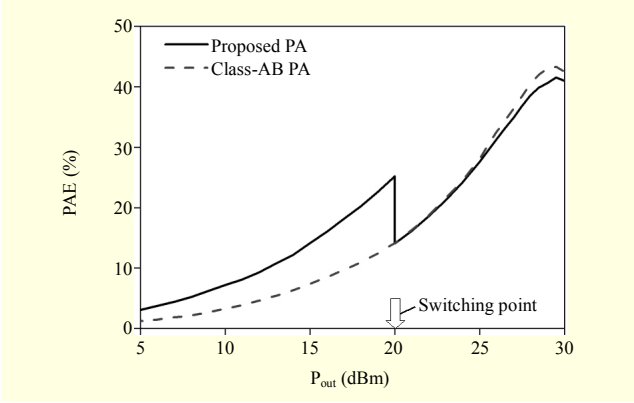

Fig. 5. Measured PAE.

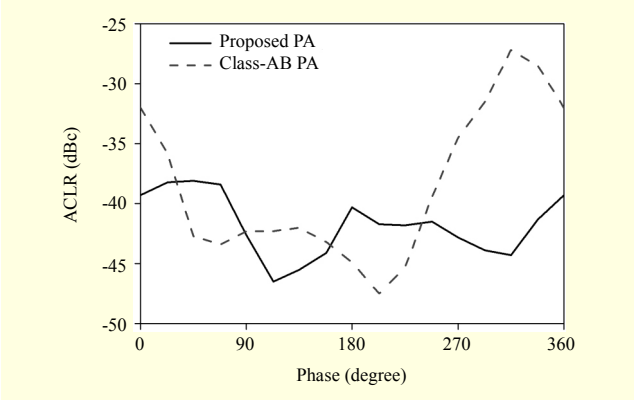

Fig. 7. Measured ACLR at P_{out}=24 dBm and VSWR=4:1.

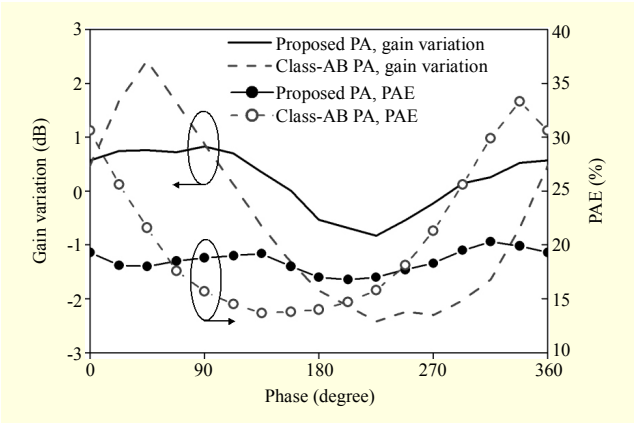

Fig. 6. Measured gain variation and PAE at P_{out}=24 dBm and VSWR=4:1.

employing the bias-switching at a specific output power, P_{out}=20 dBm. Thanks to the low idle current and high efficiency in the low-power mode, the average currents of the proposed PA were as low as 34.5 mA in urban and 56.3 mA in suburban environments [1]. This means that the average current can be reduced by 55% in urban and 41% in suburban environments as compared to that of the conventional class-AB PA.

To verify the load-insensitivity of the proposed PA, gain variation, PAE, and ACLR were measured under a VSWR of 4:1 and delivered power of 24 dBm as shown in Figs. 6 and 7. As expected from the calculated results in Fig. 2, the proposed PA exhibited excellent load-insensitivity with a gain variation of less than 1.6 dB and an ACLR better than -38 dBc over all phases, whereas the class-AB PA showed the worst ACLR of -27 dBc at a specific phase as well as a poor gain variation of 4.8 dB. It was also found in Fig. 6 that the proposed PA showed a PAE higher than 17% constantly over all phases.

IV. Conclusion

A highly efficient and load-insensitive PA module with small form-factor was developed for W-CDMA handset applications. The main obstacle to the application of the balanced PA in handset applications is overcome by employing highly integrated MMIC and lumped-element circuits with a simple structure. The selective biasing and programmable load impedance adjustment enables the proposed PA to operate in two separate power modes, resulting in very low average current consumption reduced by 55% in urban and 41% in suburban environments as compared to a conventional class-AB PA. The proposed PA showed good load-insensitivity, maintaining an ACLR of better than -38 dBc over all phases of a VSWR of 4:1. It can also be applied to other types of wireless applications requiring high efficiency and compact size.

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