Elimination of Idle Tones by a 2-Bit Adaptive Sigma-Delta Modulation System

Evangelos Prosalentis and George S. Tombras

The operation of a first-order 2-bit adaptive sigma-delta modulation system is described and discussed in this paper. The system operation is based on the combination of both "memory" and "look-ahead" estimation in the employed step-size adaptation algorithm of the basic quantizer. In comparison to simple systems and other adaptive sigma-delta systems, computer simulation results show that these features of the described system are responsible for the high SNR values and the extended dynamic range achieved for AC signals as well as the noise power reduction of almost 10 dB and the complete elimination of the idle tones for DC signals. However, such an advantageous performance requires the least possible multiplicative error accumulation, and this cannot be achieved without analog circuits of the highest possible accuracy.

Keywords: Adaptive sigma-delta modulation, idle tones, sigma-delta modulation.

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Evangelos Prosalentis (email: eprosaled@phys.uoa.gr) and George S. Tombras (phone: +302107276985, email: gtombras@phys.uoa.gr) are with the Department of Electronics, Computers, Telecommunications and Control, Faculty of Physics, University of Athens, Panepistimiopolis, Athens, Greece.

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I. Introduction

Among various analog-to-digital conversion (ADC) techniques, sigma-delta modulation (SDM) is one of the most popular due to its high resolution and relatively simple implementation. In its typical operation for AC input signals, the quantization noise from such a 1-bit quantizer is not white, while for DC input signals it appears as a periodic noise pattern due to the inherent generation of so-called idle tones. Various dithering techniques have been employed to whiten the noise pattern, causing dynamic range degradation [1], [2].

In adaptive SDM (ASDM), the step-size of the employed quantizer varies according to a pre-decided rule. Such a rule may include "memory" (estimation from the modulator output) and/or "look ahead" (estimation from the input signal itself or the quantizer input) features in the step-size estimation process. Thus, ASDM offers increased dynamic range and reduced quantization noise at the expense of some added complexity. Among several adaptation schemes that have been investigated in the literature so far [3], [4], a good example is the 2-bit ASDM system proposed by Aldajani and Sayed [5], which offers enhanced overall performance by adopting exponential step-size variability but does not solve the problem of idle tone generation.

Recently, we presented a new 2-bit ASDM system that incorporates both "memory" and "look ahead" characteristics in its instantaneous step-size adaptation algorithm [6]. The system does not generate idle tones despite dithering, and it offers high signal-to-noise ratio (SNR) values and extended dynamic range, although its practical performance is dependent on multiplicative error accumulation, as in one-bit and multi-bit SDM schemes [7], [8]. Moreover, in contrast to what is normally meant by multi-bit sigma-delta quantizers, the system generates 2-bit output codewords that convey source coding information rather than signal coding information since its operation is based on an adaptive 1-bit quantizer. As a consequence, the complete system must be seen as a hybrid system employing an almost analog process which cannot be equivalently replaced by a multi-bit quantizer.

In this paper, we mainly discuss the relation between the number of step-sizes generated and used during the coding process of our new system and the elimination of idle tones in comparison to ordinary SDM and the considered 2-bit ASDM system by Aldajani and Sayed, which we will refer to hereafter as "conventional 2-bit ASDM." Both these systems are briefly described in section II, while the proposed 2-bit ASDM system is presented in section III. Computer simulation results for the operation of all systems with and without dithering are finally given and discussed in sections IV and V.

II. Description of SDM and 2-Bit ASDM Systems

In an SDM system, the quantization noise is shaped towards higher frequencies according to the *noise transfer function* and the band-limited input signal passes through the modulator with minimum changes according to the *signal transfer function* [1]. In this respect, an oversampling 1-bit quantizer is incorporated within a feedback loop and an output binary signal $y(n)=L(n)=\mathrm{sgn}[p(n)]\cdot\Delta$ is generated, where Δ is the fixed quantizer's step-size, $L(n)$ is the 1-bit output codeword, and $p(n)$ is the output of a noise shaping filter $H(z)$. Clearly, if $H(z)$ is a simple integrator, then

$$p(n) = p(n-1) + e(n), \tag{1}$$

where $p(0)=0$, and $e(n)$ is the error between the encoded signal $y(n)$ and the input sample $x(n)$.

The quantizer step-size $\Delta(n)$ of the 2-bit ASDM system described in [5] takes values within a region $[\Delta_{\min}, \Delta_{\max}]$ according to the general form

$$\Delta(n) = M(n) \cdot \Delta(n-1), \tag{2}$$

common to all instantaneous step-size adaptation algorithms [5], [6], while $M(n)$ is the step-size multiplier at each sampling instant n, defined as

$$M(n) = \begin{cases} \alpha & \text{if } |p(n)| > \Delta(n-1), \\ \dfrac{1}{\alpha} & \text{otherwise,} \end{cases} \tag{3}$$

where $\alpha > 1$ [5], and $p(n)$ is the output of the noise shaping filter $H(z)$. Following that, the encoded output signal is written as

$$y(n)=\mathrm{sgn}[p(n)]\cdot\Delta(n), \tag{4}$$

while the 2-bit output codewords convey information about the sign and the quantizer step-size $\Delta(n)$ at instant n and consist of a first bit, $L_1(n)=\mathrm{sgn}[p(n)]$, and a second bit, $L_2(n)$, defined as

$$L_2(n) = \begin{cases} +1 & \text{if } |p(n)| > \Delta(n-1), \\ -1 & \text{otherwise.} \end{cases} \tag{5}$$

Hence, although the system operation is based on a 1-bit quantizer, it is (4) and the step-size adaptation rule

$$\Delta(n) = \alpha^{L_2(n)} \Delta(n-1) \tag{6}$$

that requires the generation of the 2-bit output codewords.

III. Description of the Proposed 2-Bit ASDM System

A block diagram of the proposed 2-bit ASDM system recently presented in [6] is shown in Fig. 1. The input signal $x(n)$ is fed to the modulator which consists of a basic SDM unit that generates the first output bit $L_1(n)$ and a set of circuit units that compose the step-size adaptation module and generate the second output bit $L_2(n)$. The two output bits are then transmitted to the demodulator which, by using a similar step-size adaptation module, produces the decoded signal $y(n)$ prior to the final low pass filtering (LPF).

The step-size estimation circuit (step-size estimator) is of major importance for the complete system operation. It is used in both the modulator and the demodulator, but is shown separately in Fig. 2. Its function is to derive the appropriate step-size $\Delta(n)$ locally required by the modulator according to the employed step-size adaptation algorithm and the values of the generated output bits $L_1(n)$ and $L_2(n)$. In particular, at each time instant n, the step-size $\Delta(n)$ can take values within $[\Delta_{\min}, \Delta_{\max}]$, following the general rule

$$\Delta(n) = M'(n) \cdot \Delta(n-1), \tag{7}$$

where $M'(n)$ is the step-size multiplier given by

$$M'(n) = M(n) \cdot \gamma(n), \tag{8}$$

where $\gamma(n)$ is defined as

$$\gamma(n) = \begin{cases} \gamma & \text{if } L_2(n) = L_2(n-1) = \text{-}1, \\ 1 & \text{otherwise,} \end{cases} \tag{9}$$

where $\gamma > 1$, and $M(n)$ is determined by

$$M(n) = \begin{cases} N(n)\beta & \text{if } |p(n)| \geq \dfrac{1}{2}(\beta + \dfrac{1}{\beta})N(n)\Delta(n-1), \\ \dfrac{N(n)}{\beta} & \text{otherwise,} \end{cases} \tag{10}$$

where $\beta > 1$, and

$$N(n) = \begin{cases} \alpha & \text{if } L_1(n) = L_1(n-1), \\ \dfrac{1}{\alpha} & \text{if } L_1(n) \neq L_1(n-1), \end{cases} \tag{11}$$

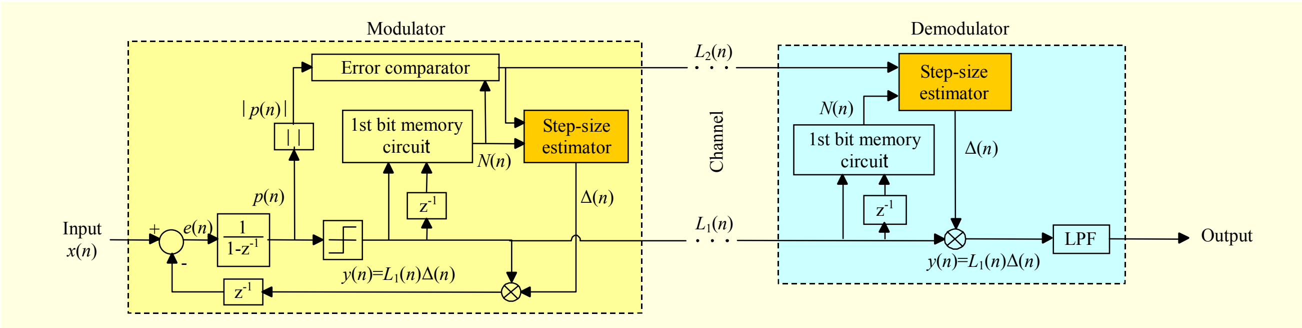

Fig. 1. Block diagram of the proposed 2-bit ASDM system.

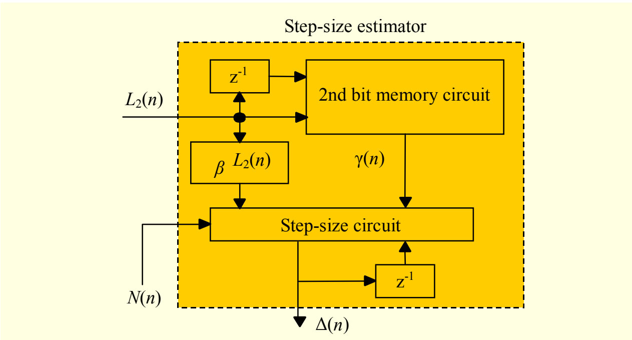

Fig. 2. Block diagram of the step-size estimation circuit of the proposed 2-bit ASDM system of Fig. 1.

where $\alpha > 1$.

In this respect, the proposed 2-bit ASDM system uses both look-ahead (forward) and memory (backward) estimation, in contrast to the conventional 2-bit ASDM. Clearly, the step-size multiplier $M'(n)$ in (7) does not depend only on the relation between the output $p(n)$ of the noise-shaping filter $H(z)$ and $\Delta(n-1)$, which is the look-ahead feature in its step-size adaptation. It also depends on the relation between the present and previous output codewords $L_w(n)$ and $L_w(n-1)$, which represents an additional double-memory feature of the employed step-size adaptation process shown in the step-size estimator of Fig. 2.

Following this and referring to Figs. 1 and 2, each output codeword consists of a first bit, $L_1(n)=\text{sgn}[p(n)]$, which is the output bit of the basic SDM unit of the modulator, and a second bit, $L_2(n)$, determined by the absolute value block for $p(n)$, the error comparator, and the value of $N(n)$, which is the output of the first bit memory circuit according to (11) and defined as

$$L_2(n) = \begin{cases} +1 & \text{if } |p(n)| \ge \frac{1}{2}(\beta + \frac{1}{\beta})N(n)\Delta(n-1), \\ -1 & \text{otherwise.} \end{cases} \qquad (12)$$

Then, $L_2(n)$ and $N(n)$ are used by the step-size estimator to determine the step-size value $\Delta(n)$ at each time instant n. It is obvious that this step-size estimation circuit must be exactly the same in both modulation and demodulation, since the so generated 2-bit output codewords convey information about the sign of the encoded signal $y(n)$ and one out of six possible values for the multiplier $M'(n)$ [6]. Then, $y(n)$ is written in compact form as

$$y(n) = L_1(n) \cdot \alpha^{L_1(n)L_1(n-1)} \beta^{L_2(n)} \gamma(n) \Delta(n-1), \qquad (13)$$

where the values of α, β, and γ are chosen to be $1 < \alpha \le 2$, $\beta \ge \alpha^2$, and $1 < \gamma < \beta$ [4].

IV. Comparison Results

In this section, we present the results of computer simulations we carried out in order to compare the performance of the proposed 2-bit ASDM system to that of SDM and the considered conventional 2-bit ASDM system using *Matlab* and *Simulink*. For both ASDM systems, we set the initial step-size to 1 mV within a range of values [0.5 mV, 5 V] with a variation range of 80 dB, while for SDM the quantization levels were set to ±1 V. In addition, the constants

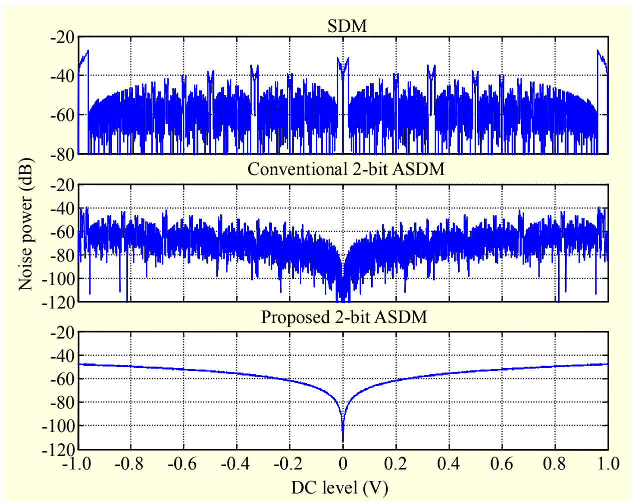

Fig. 3. Noise power vs. DC input level for the three systems.

of the proposed 2-bit ASDM system were set to α = 1.1, β = 1.75, and γ = 1.15, while for the conventional 2-bit ASDM system α = 1.45. These values are considered optimum for both AC and DC input signals [5], [6], although here we are concerned only with DC signals and the generation of idle tones.

The first comparison was carried out in terms of baseband (0 kHz to 20 kHz) modulation noise as estimated for various levels of a DC input signal sampled at 1.024 MHz. We used a binary output sequence of 2^{17} samples and applied a time domain Blackman-squared window prior to Fourier transform. The obtained results are shown in Fig. 3. SDM generates noise peaks (noise pattern) with magnitude up to almost -27 dB adjacent to integer divisions of the space between the quantization levels [1]. A noise pattern also exists at the output of the conventional 2-bit ASDM system with magnitude up to almost -40 dB. Clearly, the output of the proposed 2-bit ASDM system is free of any noise pattern, that is, it operates without generating idle tones.

In a second comparison, we estimated the power spectrum and the short-term autocorrelation of the quantization error of each system without dithering, since a simple spectral analysis alone is not sufficient to reveal the idle tones that are short-term periodic in the time domain [1]. We used a DC input signal with an amplitude of 1/128 volts (-42.14 dB) sampled again at 1.024 MHz and a Blackman-squared window applied to a binary output sequence of 2^{20} samples. The obtained results are shown in Fig. 4. In particular, the SDM's power spectrum which is shown in the upper graph of Fig. 4(a) contains detectable lines at discrete multiples of 4 kHz, while it reveals a tonal behaviour with a noise pattern repeated at every 128 samples as shown in the upper graph of Fig. 4(b). Similarly, the conventional 2-bit ASDM's power spectrum, shown in the middle graph of Fig. 4(a), contains detectable lines at discrete multiples of 69 Hz and 15 kHz, with a noise pattern repeated at every 14,754 and 68 samples, respectively, as shown in the middle graph of Fig. 4(b). However, as shown in the lower graph of Fig. 4(a), the proposed system generates a white-noise-like power spectrum that simply follows the spectrum envelope of the conventional 2-bit ASDM, except the impulses at the discrete multiples of 15 kHz (the first is at -85 dB). Furthermore, there is no output noise pattern as seen in the lower graph of Fig. 4(b).

A possible explanation for the noise pattern that appears in the output spectrum of the considered systems may be the number of different step-size values used during the coding process of the DC input signal and the distribution of the resulting quantization error values. Indeed, for an SDM system, it is obvious that only two step values are used, namely $+\Delta$ and $-\Delta$. However, for the two 2-bit ASDM systems, this has to be investigated, since variation of the step-size results in various

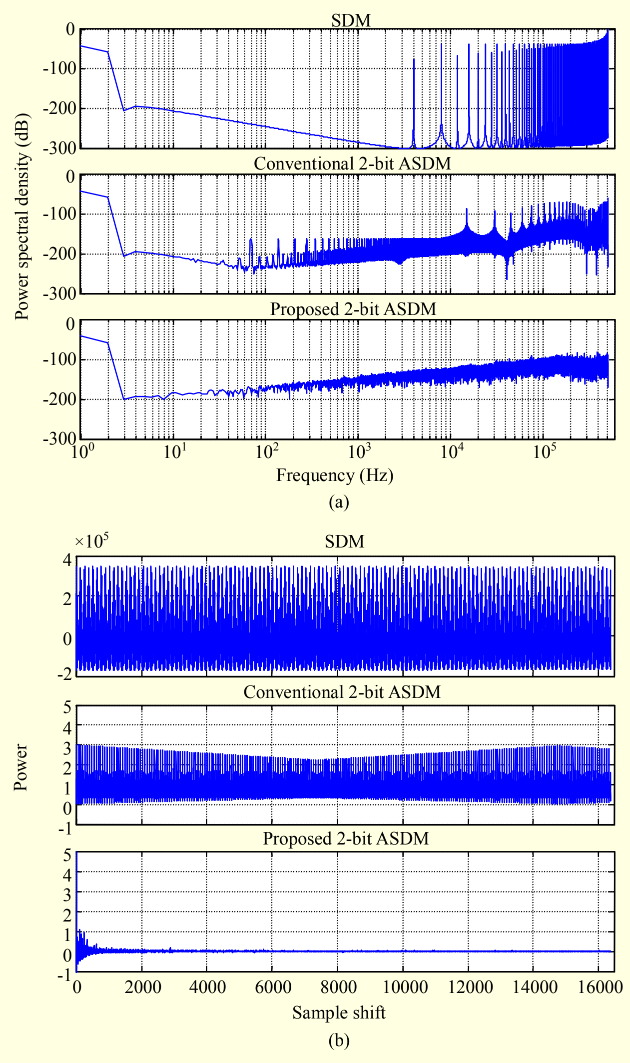

Fig. 4. Performance comparison of the three systems without dithering: (a) full-band power spectrum estimation and (b) autocorrelation estimation.

quantization error values which may follow a pattern of periodicity. This can be seen in Fig. 5, where histograms of step-size and quantization error values of both the considered ASDM systems are shown in Figs. 5(a) and 5(b), respectively, for the same DC input and the same binary output sequence of 2^{15} samples. Clearly, more step-sizes are used by the proposed 2-bit ASDM system than the conventional 2-bit ASDM. Hence, it is practically impossible to assume that there is (or even may appear to be) a pattern of step-sizes used by the proposed system, as appears to be the case for the conventional system with a limited number of step-sizes. Moreover, as shown in the lower graph of Fig. 5(b), a smooth and normal-like distribution for the quantization error values is revealed. We consider this a strong indication that the more step-sizes used, the smoother and closer to normal the quantization error distribution is; thus,

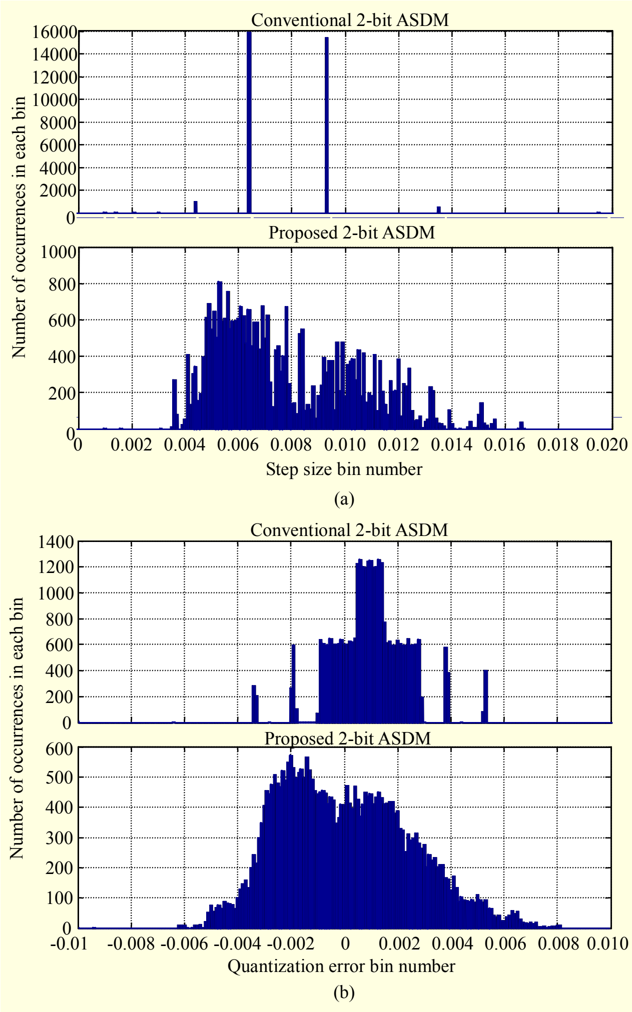

Fig. 5. Histograms for the two ASDM systems: (a) step size and (b) quantization error.

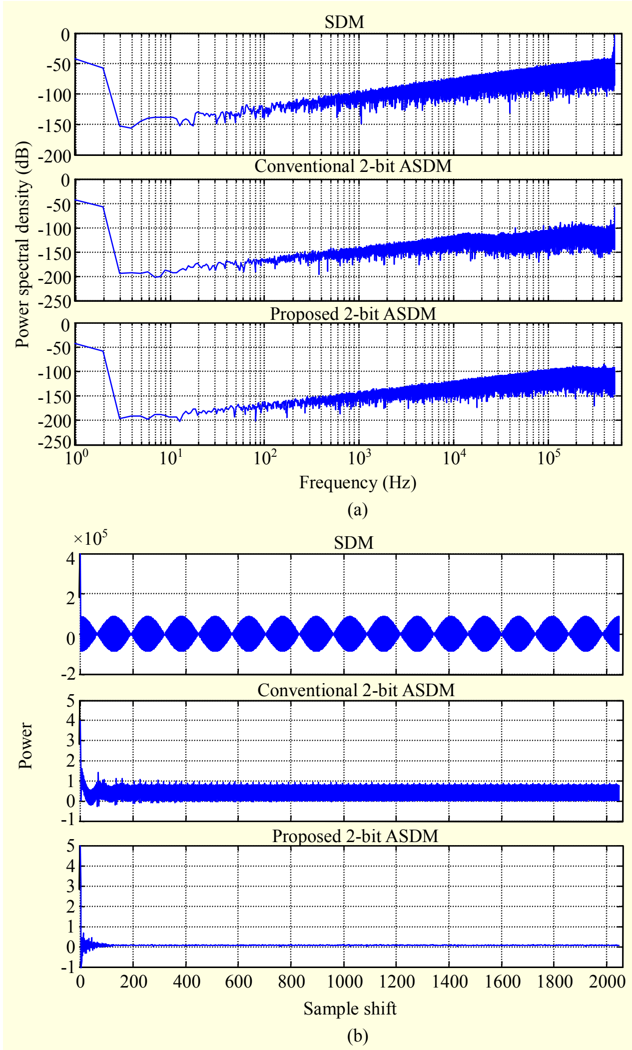

Fig. 6. Performance comparison of the three systems with dithering: (a) full-band power spectrum estimation and (b) autocorrelation estimation.

a white-noise-like output spectrum results.

Finally, we compare the three systems for the same DC input signal using dithering. The obtained results can be seen in Fig. 6. Specifically, by adding a pseudorandom signal with rectangular probability density function to the SDM input spanning one half the quantizer interval, that is, $\delta/\Delta = 0.5$, the SDM's power spectrum appears free of idle tones as shown in the upper graph of Fig. 6(a). However, its autocorrelation, shown in the upper graph of Fig. 6(b), reveals a noise pattern repeated at every 128 samples. Next, for both the considered 2-bit ASDM systems, we use a dither level of $\delta/\Delta=0.01$. In addition, for the conventional 2-bit ASDM system, we must increase the dither level from $\delta/\Delta = 0.005$ up to $\delta/\Delta=0.01$ [4] to eliminate the periodic modulation effect from its autocorrelation shown in the middle graph of Fig. 6(b), while any increase of the DC input signal requires further increase of the dither level. Furthermore, as shown in the middle graphs of Figs. 4(a) and 6(a), the base-band noise is almost 50 dB higher than that without dithering, justifying a trade off between dithering and dynamic range. Again, the proposed 2-bit ASDM appears superior because its power spectrum remains almost unchanged and there is a small improvement in its autocorrelation estimation as shown in the lower graphs of Figs. 4(b) and 6(b), respectively.

V. Conclusion

In this paper, we described and discussed the operation of a recently presented 2-bit ASDM system. The large number of step sizes used by the proposed 2-bit ASDM system is the outcome of an almost analog process (due to the memory and look-ahead features of its step-size adaptation algorithm). Hence, the complete system shown in Figs. 1 and 2 must be seen as a dynamically self-controlled hybrid system which generates 2-bit output codewords that convey information about the sign and step size of an adaptive 1-bit SDM quantizer, rather than information about the encoded signal itself. In this respect, the elimination of idle tones for DC input signals and the high SNR values and extended dynamic range for AC signals [6] require the least possible multiplicative error accumulation, and this cannot be achieved without analog circuits of the highest possible accuracy. Moreover, the step-size estimation circuit must be identical in both the modulator and demodulator. Hence, what appears to be a highly advantageous feature may very easily turn out to be a serious deficiency. Surely, there must be a trade-off between the number of step sizes that can be efficiently used in order to minimize idle tone generation in the output power spectrum, but investigating this is beyond the scope of this work.

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Evangelos Prosalentis received the BS degree in physics and the MS degree in electronics from the University of Athens, in 1989 and 1993, respectively. Since 1997, he has been a professor of electronics in post-compulsory secondary education. From 2001 to 2004, he was associated with the Department of Electronics in the Technological Educational Institute (TEI) of Athens, where he was responsible for the laboratory course in radar and radio systems. He is currently a PhD candidate with the Laboratory of Electronics, Department of Physics, University of Athens.

George S. Tombras received the BSc degree in physics from Aristotelian University of Thessaloniki, Greece, the MSc degree in electronics from University of Southampton, UK, and the PhD from Aristotelian University of Thessaloniki, in 1979, 1981, and 1988, respectively. From 1981 to 1989 he was a teaching and research assistant, and from 1989 to 1991, he was a lecturer with the Laboratory of Electronics, Physics Department, Aristotelian University of Thessaloniki. Since 1991, he has been with the Laboratory of Electronics, Faculty of Physics, University of Athens, where currently is an associate professor of electronics and director of the Department of Electronics, Computers, Telecommunications, and Control. His research interests include mobile communications, analog and digital circuits and systems, as well as instrumentation, measurements, and audio engineering. Professor Tombras is the author of the textbook *Introduction to Electronics* (in Greek) and has authored or co-authored more than 90 journal and conference refereed papers and many technical reports.