Ku-Band Power Amplifier MMIC Chipset with On-Chip Active Gate Bias Circuit

Younsub Noh, Dongpil Chang, and In-Bok Yom

We propose a Ku-band driver and high-power amplifier monolithic microwave integrated circuits (MMICs) employing a compensating gate bias circuit using a commercial 0.5 μm GaAs pHEMT technology. The integrated gate bias circuit provides compensation for the threshold voltage and temperature variations as well as independence of the supply voltage variations. A fabricated two-stage Ku-band driver amplifier MMIC exhibits a typical output power of 30.5 dBm and power-added efficiency (PAE) of 37% over a 13.5 GHz to 15.0 GHz frequency band, while a fabricated three-stage Ku-band high-power amplifier MMIC exhibits a maximum saturated output power of 39.25 dBm (8.4 W) and PAE of 22.7% at 14.5 GHz.

Keywords: Bias circuit, compensation, driver amplifier, Ku-band, pHEMT, MMIC, power amplifier, supply voltage, temperature, threshold voltage.

I. Introduction

Recently, Ku-band driver amplifier monolithic microwave integrated circuits (MMICs) have been demonstrated for local multipoint distribution service, point-to-point wireless communications systems, and very small aperture terminal (VSAT) applications with high gain [1], low cost [2], and single-supply [3] characteristics. High-power amplifiers (HPAs) are critical components for wireless communication systems. The previously reported Ku-band HPAs were developed by using a 0.25 μm GaAs pHEMT process exhibiting a saturated output power ranging from 6 to 8 W [4]-[7] without any compensation mechanism, such as process, temperature, or supply voltage variations. However, pHEMT MMICs are sensitive to threshold voltage and temperature variations. The threshold voltage of the transistor, which is typically varied by ± 0.3 V in fabricated chips, mainly determines the yield of an MMIC amplifier, and pHEMT amplifiers are seriously affected by temperature variations. Moreover MMICs designed without an on-chip gate bias circuit require external components for biasing, resulting in a high cost for module assembly. Thus, on-chip gate bias circuits built on MMICs are strongly required to achieve low cost and ease of use for modules. The compensation of temperature variations and partial compensation of threshold variations were introduced for a Ku-band low-noise amplifier [8]. However, it mainly focuses on compensation of temperature variations by increasing the drain current as the temperature increases.

In this work, we propose an on-chip gate bias circuit for compensating the threshold voltage and temperature variations, and an independent bias of supply voltage variations. The bias scheme is applied to a Ku-band driver amplifier and HPA

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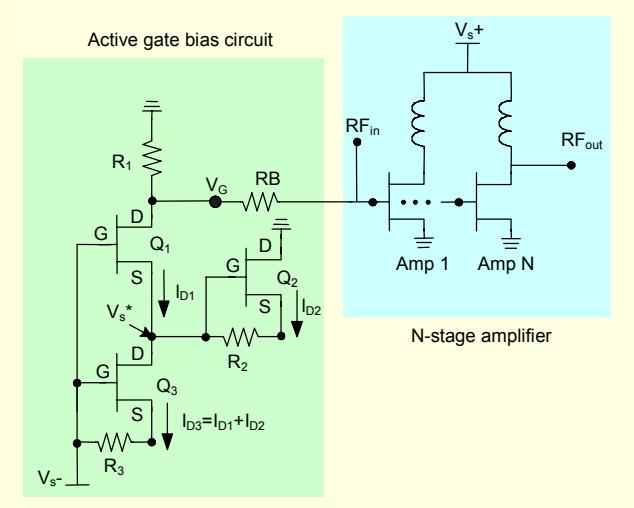

Fig. 1. Proposed active gate bias circuit.

MMICs, which are designed using a commercial 0.5 μm GaAs pHEMT process. Measurements show good agreement with the theoretical predictions of the proposed bias circuit. The design and measurement of the compensating gate bias circuit, driver amplifier MMIC, and HPA MMIC will be discussed in the next sections.

II. Active Gate Bias Circuit Design

The functions of an active gate bias circuit are setting the DC gate bias of the amplifiers, compensating the threshold voltage and temperature variations, providing independence of the supply voltage variations, and reducing the cost of assembly by integrating the amplifiers within MMICs.

An on-chip compensating gate bias circuit (Fig. 1) for MMIC amplifiers is proposed. The bias circuit is composed of resistors (R_1, R_2, and R_3) and transistors (Q_1, Q_2, and Q_3). The resistor RB is used for blocking RF leakage to the bias circuit. A gate bias voltage of V_G is simultaneously applied to the amplifiers from Amp 1 to Amp *N*. The proposed active gate bias circuit operates with a negative supply voltage (V_s-) and the *N*-stage amplifier operates with a positive supply voltage (V_s+).

The drain current of transistor Q_3 (I_{D3}) is determined by the summation of the drain currents of Q_1 (I_{D1}) and Q_2 (I_{D2}).

$$I_{D3} = I_{D1} + I_{D2}. \quad (1)$$

1. Setting of DC Gate Bias

For the Ku-band driver and power amplifiers, we select the class-AB bias to simultaneously obtain high gain, high output power, high linearity, and high efficiency characteristics. The resistance value of R_1 and the drain current of transistor Q_1 (I_{D1}) determine the gate bias of V_G.

2. Compensation of Threshold Voltage Variation

In general, the drain current of the amplifier decreases as the threshold voltage denoted by V_{th} increases in the positive direction in the case of a fixed gate bias. When the threshold voltage (V_{th}) increases in the positive direction, the drain current of the amplifier decreases. To compensate the reduction of the drain current, the gate bias V_G of the amplifier should be increased in the positive direction. When V_{th} slightly shifts to a larger value due to the process variation, the drain currents of Q_1, Q_2, and Q_3 decrease. Then, a voltage drop through resistor R_1 generates a higher value of V_G. Thus, the drain current of the amplifier can be kept constant with a variation of V_{th}.

3. Compensation of Temperature Variation

In the case of temperature variation by ΔT, the drain current variation of I_{D1} is expressed as

$$\Delta I_{D1}(\Delta T) = \Delta I_{D3}(\Delta T) - \Delta I_{D2}(\Delta T). \quad (2)$$

The amount of drain current variation of Q_3 (ΔI_{D3}) according to temperature variation is the largest among all transistors. Therefore, the drain current variation of Q_1 (ΔI_{D1}) by temperature variation depends on the drain current variations of Q_3. When the temperature decreases, the drain currents of both Q_1 (I_{D1}) and Q_3 (I_{D3}) increase, and an additional voltage drop through resistor R_1 then occurs, which makes gate voltage V_G lower. Therefore, the drain current of the amplifier decreases as the temperature decreases. In general, the gains of MMIC amplifiers increase as the temperature decreases, and they decrease as the drain current decreases. Thus, the proposed active gate bias circuit provides a compensated gate bias of temperature variations.

Figure 2 shows simulated drain currents of an amplifier (8F150, total gate width W_g=1,200 μm) with a proposed gate bias V_s- of -5 V and a direct bias V_G of -0.8 V as functions of a threshold voltage of ± 0.3 V and a temperature variation from -20°C to 80°C.

When the direct bias V_G is -0.8 V, the drain currents of the amplifier exhibit severe changes of ± 29% variation (25°C, current range = 94.7 mA to 165.8 mA) with a V_{th} variation of ± 0.3 V. The drain current of the RF amplifier decreases with an increase of temperature, resulting in RF performance degradation with increasing temperature.

With the proposed compensating gate bias circuit, the drain currents of the RF amplifier range from 131.3 mA to 137.7 mA with a V_{th} variation of ± 0.3 V and temperature variation of 100°C. The peak variation of the drain current with respect to the threshold voltage variations is only 3.2 mA (± 1.4%) at a

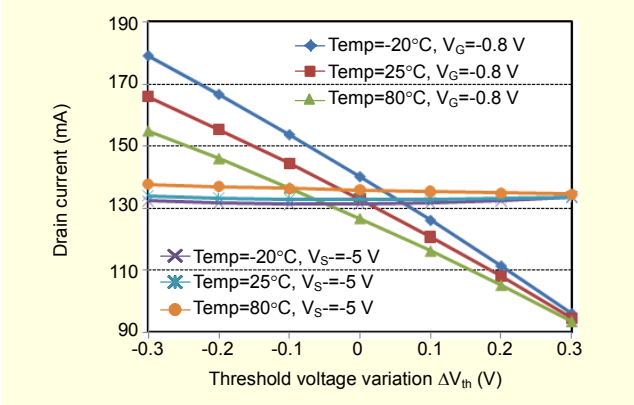

Fig. 2. Simulated drain currents of amplifier (W_g=1.2 mm) as functions of threshold voltage and temperature variations with the proposed active bias and direct bias.

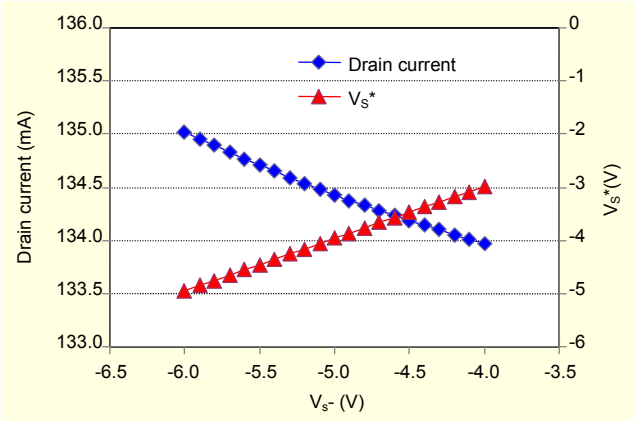

Fig. 3. Simulated drain currents of an amplifier (W_g = 1.2 mm) and the drain voltage of Q_3 (V_s*) in Fig. 1 as a function of negative supply voltage (V_s-).

temperature of 80°C, which proves an excellent compensation of the threshold voltage variation. In addition, the simulated drain current of the RF transistor at a temperature of 80°C reveals a 4.6 mA higher value than that at -20°C, which provides compensation of temperature variations.

4. Independence of the Supply Voltage

An active gate bias circuit insensitive to negative supply voltage (V_s-) variations is strongly required in a real system design. The drain voltage of Q_3 (V_s*) in Fig.1 is proportional to the negative supply voltage of V_s-. The voltage difference between V_s* and V_s- is about 1.0 V, which is the voltage drop through transistor Q_3 and resistor R_3. The simulated drain current variation of the amplifier (W_g = 1.2 mm) is as small as 1.1 mA over a negative supply voltage (V_s-) from -6.0 V to -4.0 V.

The periphery of 0.15 mm (2F75) is used for the bias

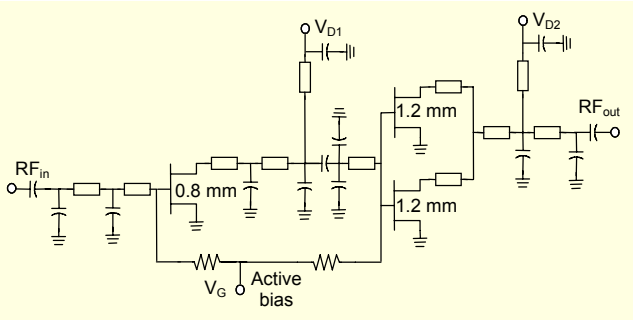

Fig. 4. Schematic diagram of the Ku-band driver amplifier MMIC.

transistors (Q_1, Q_2, and Q_3), and the resistor R_1 of 100 Ω generates V_G of -0.8 V with I_{D1} of 8 mA. The simulated optimum bias condition to satisfy the above requirements of the active gate bias circuit simultaneously is revealed as

$$I_{D2} = 2I_{D1}\,. \tag{3}$$

The determined resistance values are 50 Ω for R_2 and 19.2 Ω for R_3 to meet (1) and (3).

5. Reducing Assembly Cost

Previously reported pHEMT amplifiers [1]-[7] have no on-chip gate bias; therefore, these amplifiers require external components for biasing with compensation mechanisms, which results in a higher cost for assembly. We integrate the proposed bias circuit within MMICs to overcome these problems.

III. Ku-Band Driver Amplifier MMIC Design and Measurement

The two-stage cascaded driver amplifier was designed and fabricated using a commercial 0.5 μm pHEMT process. The periphery of the pHEMTs is 0.8 mm (8F100 × 1) and 2.4 mm (8F150 × 2) for the first stage and the power stage, respectively (Fig. 4). The input, inter-stage, and output matching networks were optimized to simultaneously obtain a larger output power and PAE based on a load/source-pull simulation. All microstrip lines were optimized by EM simulation.

Shunt RC networks were added to all gates of amplifying HEMTs to enhance the electrical stability for all frequency bands. For gate biasing, the proposed on-chip compensating gate bias circuit of Fig. 1 was used for the two amplifying stages shown in Fig. 5. The fabricated Ku-band driver amplifier MMIC with the proposed bias circuit is also shown in Fig. 5. The size of the MMIC is 2.85 mm × 1.35 mm with a thickness of 0.1 mm.

The drain current of the driver amplifier MMIC was measured with a direct gate bias V_G of -0.8 V and the proposed on-chip gate bias circuit with three different values of V_s- (-4.5 V,

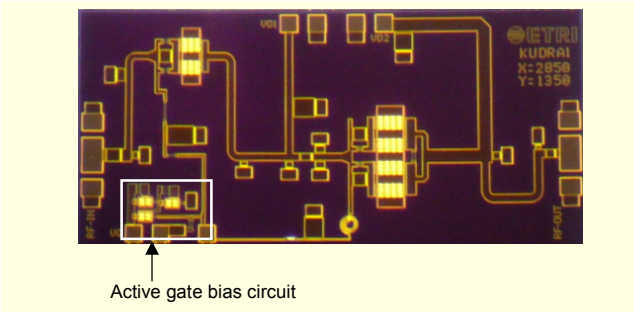

Fig. 5. Photograph of the fabricated Ku-band driver amplifier MMIC.

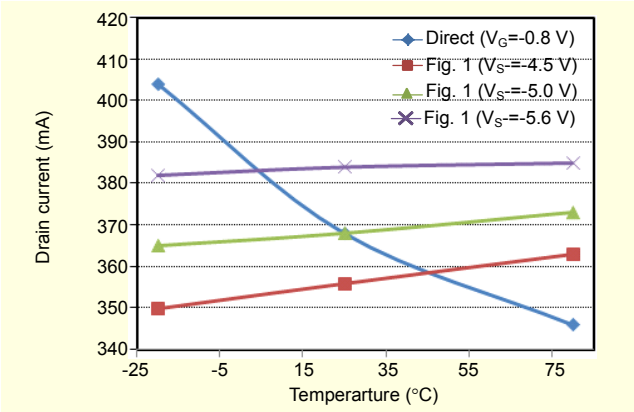

Fig. 6. Measured drain current of Ku-band driver amplifier for direct bias and proposed on-chip gate biases of Fig. 1.

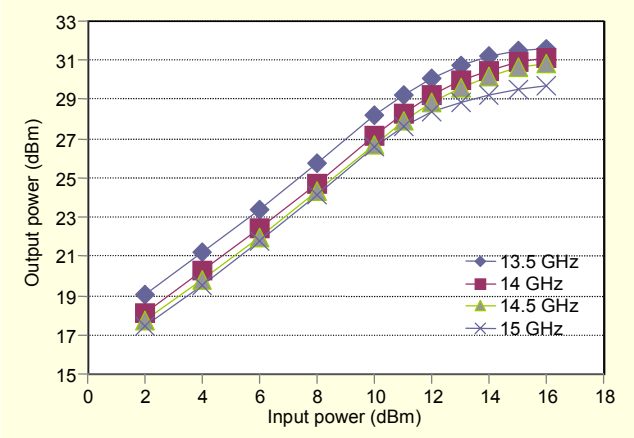

Fig. 7. Measured output power as a function of input power.

-5.0 V, and -5.5 V) as shown in Fig. 6. For a direct bias case of V_G = -0.8 V, the drain current decreases as the temperature increases, operating as a general MMIC without compensation of temperature.

With the proposed bias circuit, the drain current increases as the temperature increases, compensating the effect of temperature variations. Furthermore, the proposed bias circuit exhibits stable drain currents over a negative supply

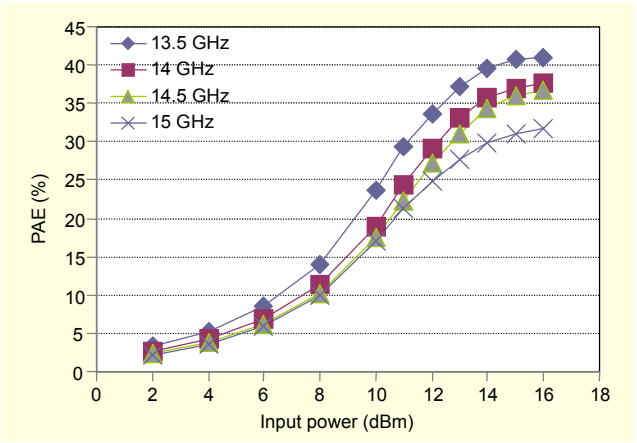

Fig. 8. Measured PAE as a function of input power.

voltage (V_s-) variation of ± 0.5 V, exhibiting a 4.3% deviation at a temperature of 25°C.

The fabricated two-stage driver amplifier MMIC was measured under a positive supply voltage (V_s+) of 7.0 V and a negative supply voltage (V_s-) of -5.0 V. The quiescent current was 368 mA with the configuration shown in Fig. 1. Figure 7 shows the measured output power at frequencies of 13.5 GHz, 14 GHz, 14.5 GHz, and 15 GHz. The 1 dB compression output power (P_{1dB}) ranges from 29.7 dBm to 31.6 dBm. The measured PAEs with the same condition as the output power are shown in Fig. 8. The measured peak PAE is 41% at 13.5 GHz.

IV. Ku-Band High-Power Amplifier MMIC Design and Measurement

A three-stage cascaded HPA was fabricated using a commercial 0.5 μm pHEMT process. The peripheries of the pHEMTs are 3.2 mm (4 × 8F100), 9.6 mm (8 × 8F150), and 19.2 mm (16 × 8F150) for the first, second, and power stages, respectively (Fig. 9). At 14 GHz, the load/source-pull simulation revealed a maximum output power of 31.1 dBm with a 2 × 8F150 (periphery of 2.4 mm) device, which is used for the unit device of the second and power stages, under a drain voltage of 7.0 V and a gate voltage of -0.8 V. The input-matching network is optimized for high gain, and the output matching networks and two inter-stages were optimized to simultaneously obtain a larger output power and PAE based on the load/source-pull simulation. All microstrip lines were fully optimized by EM simulation as in the driver amplifier design.

A fabricated Ku-band HPA MMIC with the proposed active gate bias circuit is shown in Fig. 10. The MMIC is as small as 4.3 mm × 4.65 mm with a thickness of 0.1 mm.

The fabricated three-stage Ku-band HPA MMIC was measured under a positive supply voltage (V_s+) of 7.0 V and

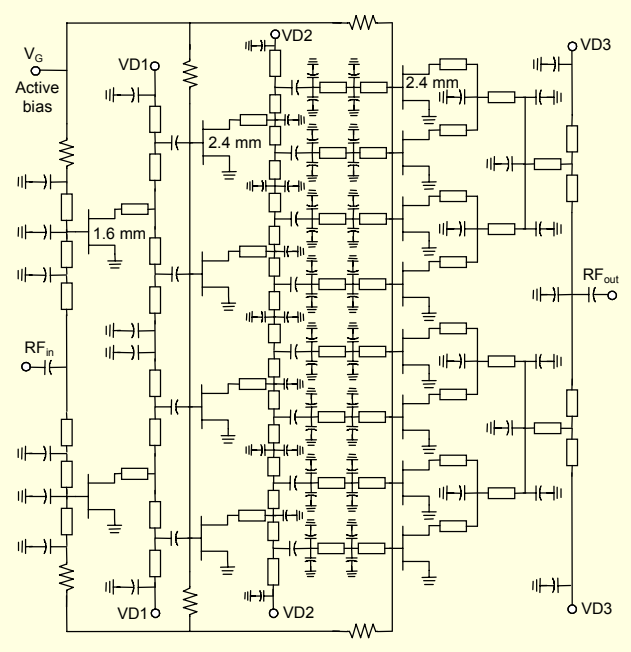

Fig. 9. Schematic diagram of the Ku-band HPA MMIC.

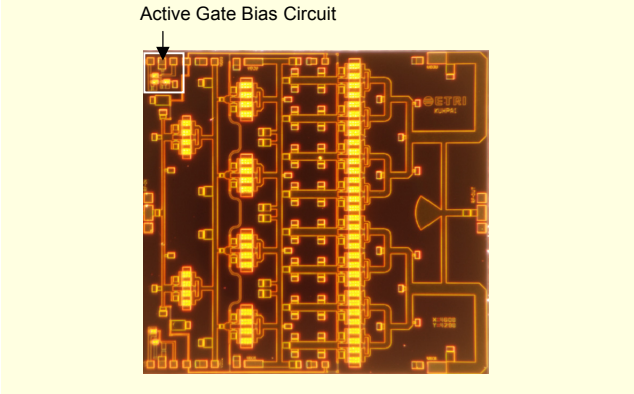

Fig. 10. Photograph of the fabricated Ku-band HPA MMIC.

negative supply voltage (V_s-) of -5.0 V, and the quiescent current was 3.5 A with the configuration shown in Fig. 1.

The small signal gain of the three-stage HPA is greater than 17.2 dB, from 12 GHz to 15 GHz, and the input and output return losses are 10 dB, typically in the same frequency range (Fig. 11).

The measured output power, associated power gain, and PAE as a function of input power at 14.0 GHz are shown in Fig. 12. The measured 1 dB compression output power (P1dB) is 38.5 dBm with a PAE of 20.4%. The saturated output power (P_{sat}) was measured with an input power of 22 dBm, and P_{sat} is 39.25 dBm (8.4 W) at 14.5 GHz with a PAE of 22.7% (Fig. 13). The measured and simulated results show good agreement.

Figure 14 shows the measured temperature dependence of P_{sat} with the proposed and direct biases. At the temperature of-

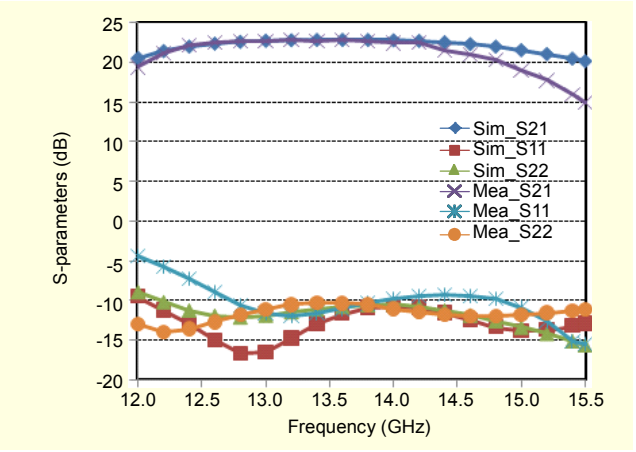

Fig. 11. Measured and simulated small signal S-parameters of the three-stage HPA.

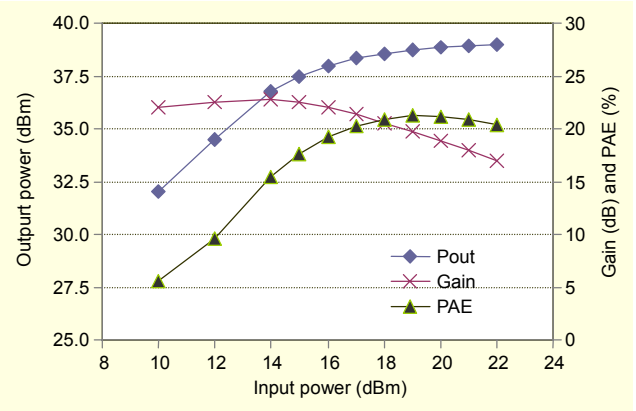

Fig. 12. Measured output power, gain, and PAE as functions of input power at 14 GHz.

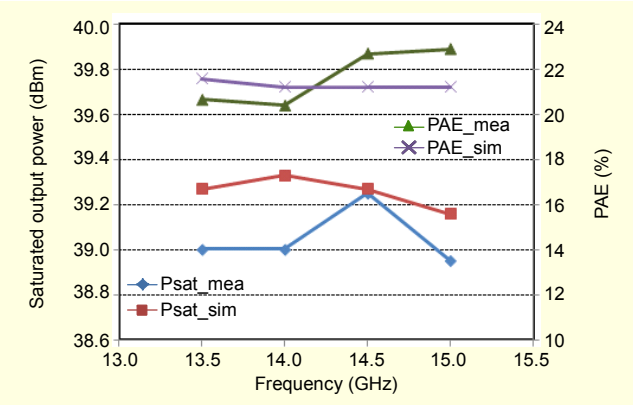

Fig. 13. Measured and simulated saturated output power and PAE as functions of frequency.

20°C, P_{sat} with the direct bias is slightly higher than that with the proposed bias. However, P_{sat} with the proposed bias exhibits about 0.3 dB higher value than that with the direct bias. This is mainly because of the drain current increasing

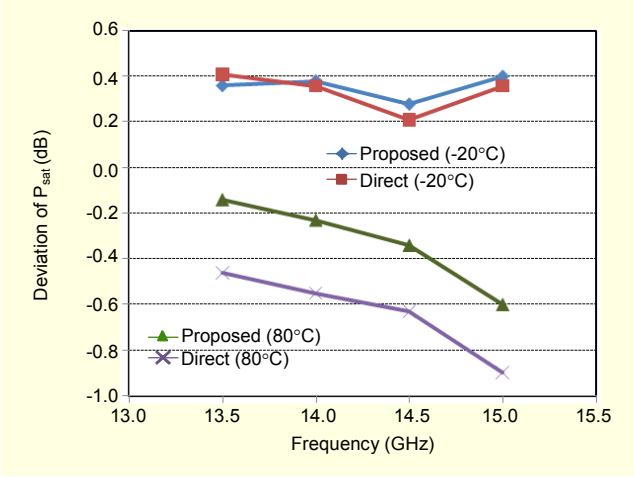

Fig. 14. Measured P_{sat} deviations of HPA from the P_{sat} value at 25°C with the proposed and direct biases.

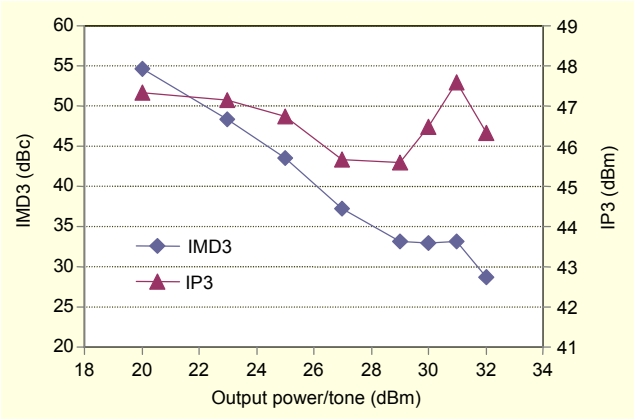

Fig. 15. Measured IMD3 and IP3 at 14 GHz as functions of output power/tone.

mechanism as the temperature increases.

The third-order intermodulation distortion (IMD3) and third-order intercept point (IP3) were measured at a frequency of 14.0 GHz as a function of output power/tone under the condition of 10 MHz input signal separation (Fig. 15). The measured IMD3 is 33 dBc for a single-tone output power of 30 dBm. The measured IP3 of the HPA is greater than 45.6 dBm, generating a 7.1 to 9.0 dB higher value than the 1 dB compression output power.

V. Conclusion

We proposed a new active gate bias circuit compensating the threshold voltage and temperature variations, providing independence of the supply voltage variations. The proposed bias circuit was applied to a Ku-band driver amplifier and HPA MMICs successfully. A two-stage driver amplifier MMIC delivered an output power of up to 31.6 dBm with a PAE of 41%, while a three-stage HPA MMIC delivered an output power of up to 39.25 dBm with a PAE of 22.7% at 14.5 GHz. We believe that these MMICs with the proposed gate bias circuit will be good candidates for Ku-band applications.

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