Test-Generation-Based Fault Detection in Analog VLSI Circuits Using Neural Networks

Palanisamy Kalpana and Kandasamy Gunavathi

In this paper, we propose a novel test methodology for the detection of catastrophic and parametric faults present in analog very large scale integration circuits. An automatic test pattern generation algorithm is proposed to generate piece-wise linear (PWL) stimulus using wavelets and a genetic algorithm. The PWL stimulus generated by the test algorithm is used as a test stimulus to the circuit under test. Faults are injected to the circuit under test and the wavelet coefficients obtained from the output response of the circuit. These coefficients are used to train the neural network for fault detection. The proposed method is validated with two IEEE benchmark circuits, namely, an operational amplifier and a state variable filter. This method gives 100% fault coverage for both catastrophic and parametric faults in these circuits.

Keywords: ATPG, genetic algorithm, catastrophic fault, parametric fault, wavelet, probabilistic neural network.

I. Introduction

Testing of analog very large scale integration (VLSI) circuits has become a challenge and has gained more interest in recent years for several reasons, such as increase in the applications of analog circuits, integration of whole systems on single chips, and the high cost of analog testing. Increased analog circuit applications are due to the analog nature of signals in the real world.

The high analog test cost results from many factors, such as expensive test equipment, long test development time, and long test production time. The development and production test time costs constitute a part of the development and production costs of the integrated circuits, respectively. The challenge faced by test engineers is to develop a test methodology to reduce the test cost and to accelerate the time-to-market without sacrificing integrated circuit (IC) quality. Consequently, the generation and evaluation of an effective test methodology is a very important issue in the production of an IC and has direct consequences on the price and the quality of the final product.

II. Faults in Analog Circuits

During the manufacture of ICs, an enormous number of various failures could be present, and it is totally infeasible to analyze them individually. Thus, failures are grouped together according to their logical fault effect on the functionality of the circuit, and this leads to the construction of logical fault models.

Faults present in ICs can be divided into three classes: permanent faults, which are faults in existence long enough to be observed at test time; temporary faults (transient or intermittent), which appear and disappear in short intervals of time; and delay faults, which affect the operating speed of the

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circuit.

Permanent faults are further classified into catastrophic faults (open and short) and parametric faults (due to disturbance in the process parameters). When a catastrophic fault occurs, the topology of the circuit is changed. Due to parametric faults, the performance parameters of each manufactured circuit deviate from the nominal one and therefore correspond to a different point in each parameter space. If each parameter of the circuit is within a fault free space, then the circuit is treated as fault free; otherwise, it is considered a faulty circuit.

In this paper, catastrophic and parametric faults are taken as fault models for analog circuits, which are designed with resistors, capacitors, MOSFETs, and bipolar junction transistors. The testing issues related to these faults are addressed in this study.

III. Test Pattern Generation

Since the cost of testing a VLSI chip is a significant fraction of the manufacturing cost, the time required to test a chip should be minimized, and there should be significant fault coverage. The objective of the automatic test pattern generator is to find an optimal set of test stimuli which detects all modeled faults, that is, a set of test stimuli which when applied to the circuit can distinguish between the correct circuit and any circuit with a modeled fault.

The goal of the proposed approach is to compute a set of test stimuli that maximizes the fault coverage while minimizing test access. Therefore, the problem of test signal generation is an optimization problem in principle. Test vector generation using deterministic techniques is highly complex and time consuming because of the extremely large search spaces involved. Therefore, artificial intelligence methods have gained much attention [1], [2].

Genetic algorithms are search optimization algorithms based on the mechanics of natural genetics that attempt to use similar methods for selection and reproduction to solve various optimization problems. Genetic algorithms have proven to be effective in VLSI applications, including circuit layout and partitioning, cell placement, routing, and automatic test generation. The proposed method uses a genetic algorithm for the generation of the test stimulus which detects both catastrophic and parametric faults present in the circuit under test (CUT).

In the literature, a genetic algorithm is used as a test pattern generator [1], [2] to generate a piece-wise linear (PWL) stimulus. In [1] and [2], multiple node points in the circuits are considered for detecting faults in the CUT. However, in complex systems all nodes in the circuit may not be accessible. Therefore, in this work only the output node is considered for measurements and the output response is analyzed using wavelets.

1. PWL Signal Generation

By exciting the CUT with pulses and ramps whose frequency spectrum stretches over a wide range of frequencies, all faults can be made visible in the measurement space. Thus, a transient PWL signal is generated for detection of both catastrophic and parametric faults present in the circuits. To generate the PWL test signal, a genetic algorithm is used. Each test vector is a transient stimulus.

Figure 1 shows an example test vector. The amplitude limit for each test vector is fixed based on the allowable range of input signal for the circuit, and the frequency of the stimulus is fixed based on the allowable operating frequency of the circuits. For example, if a circuit has a supply voltage of 2.5 V, a gain of 2, and a 1 MHz bandwidth, then the amplitude range for the PWL stimulus is fixed from -1 to +1 and the frequency is fixed from 1 Hz to 1 MHz. The length of the PWL signal is fixed based on the amplitude level and frequency of operation of the CUT. Initial random vectors (PWL test signals) are selected such that all amplitude levels are covered.

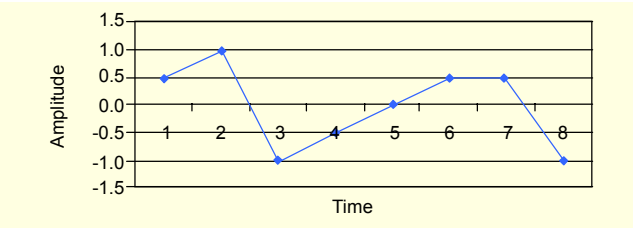

Fig. 1. PWL test vector.

2. Bounds for Parameters

For the given CUT, the bounds of the parameters are found as follows.

In general, a circuit is bounded by n specifications, $S = [s_1, s_2, \cdots, s_n]$. For designing the circuit, m parameters, $P = [p_1, p_2, \cdots, p_m]$ are used. Each specification is dependent on one or more parameters. Under single parametric (p_i) fault assumption, upper and lower bounds of the parameters are fixed for each specification. Given an acceptable range of s_j (upper bound s_j^u, lower bound s_j^l), the accepted tolerance range of p_i (upper bound p_i^u, lower bound p_i^l) can be found as shown in Fig. 2.

The final upper and lower bounds of the accepted range for p_i are found as follows:

$$p_i^u = \min(p_{i1}^u, p_{i2}^u, \cdots, p_{in}^u), \quad (1)$$

$$p_i^l = \max(p_{i1}^l, p_{i2}^l, \cdots, p_{in}^l). \quad (2)$$

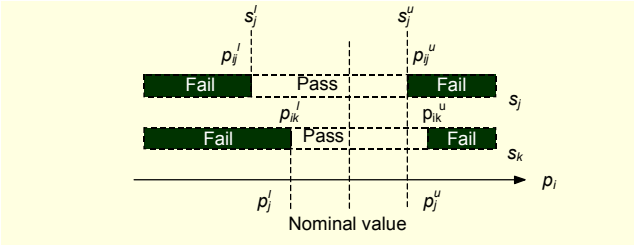

Fig. 2. Bounds for parameters.

After setting the bounds for parameters, the circuit is simulated under fault-free and faulty conditions.

3. Feature Extraction Using Wavelets

Wavelet transform (WT) is capable of providing the time and frequency resolution simultaneously and hence giving time-frequency representation of the signal. Deviation of any parameter alters the specifications of the circuit. These specifications may be represented as time domain or frequency domain units. If both time and frequency domain information are available, then all possible faults present in the circuit can be detected.

Generally, the presence of catastrophic faults changes the functioning of the circuit. Some of them do not change the circuit functioning fully and affect only the specifications of the circuit. In such cases, it is necessary to obtain both time and frequency domain information about the signal; therefore, wavelet decomposition is performed on the output signal.

The output voltage response of the signal is captured and is sampled with the sampling frequency of 5f, where f is the basic frequency of the signal. When this signal passes through the filter bank, the multiresolution decomposition of the signal takes place. Two filters are present at each stage of resolution. The first filter is the mother wavelet, which is high pass in nature. The second filter is low pass in nature. The downsampled output of the high pass filter provides the detail coefficients, and the low pass filter provides the approximation coefficients. The detail and approximation coefficients reflect the high and low frequency contents of the signal.

The frequency components at different levels in the decomposed signal for the signal of frequency 5f are shown in Table 1. Since the approximation coefficients give the basic structure of the signal, approximation coefficients are used for analysis. For the selection of a suitable wavelet, analysis is performed using different wavelets and one which shows maximum classification efficiency is chosen for classification of faulty circuits. Since the sampling frequency is 5f, the signal is decomposed into five levels. The wavelet coefficients from level one to level three contain most of the information about the signal.

Table 1. Frequency components at different levels in the decomposed signal.

	Detail coefficient	Approximation coefficient
Level 1	2.5f –5f	0f –2.5f
Level 2	1.25f –2.5f	0f –1.25f
Level 3	0.625f –1.25f	0f –0.625f
Level 4	0.3125f –0.625f	0f –0.3125f
Level 5	0.15625f –0.3125f	0f –0.15625f

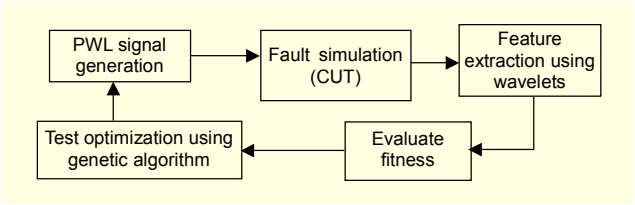

Fig. 3. Test pattern generation using genetic algorithm and wavelets.

4. Proposed Specification Driven Test Pattern Generation Method

An overview of the proposed test generation methodology is shown in Fig. 3. The input to the proposed test generator consists of the circuit description and the specifications of the circuit. The output of the test generator consists of test stimuli. The nominal specifications (gain and BW) for the CUT are found. The acceptable deviation for each parameter (internal and external) is decided based on the given lower and upper bound of the circuit specifications as discussed in section III.2. After the bounds for the parameters are set, the circuit is simulated under fault-free and faulty conditions.

A genetic algorithm is used to find the optimal test stimulus. The initial population is generated randomly. All the parameters in the circuit are varied within their acceptable range of values and Monte Carlo analysis is performed for each test pattern. The same test patterns are applied to the fault-free circuit and the nominal results are observed. The output signal is sampled and wavelet decomposition is performed for every Monte Carlo result as well as the nominal result. The root mean square error (RMSE) is calculated between the wavelet coefficients of the nominal result and the wavelet coefficients of each Monte Carlo result. From this array of MSE values, the minimum and maximum values are chosen. These values determine the acceptable (threshold) range for the fault free circuit.

Then faults are introduced in the circuit one by one from the fault list, and faults are simulated for each test vector. The RMSE is calculated as before using wavelets. If this RMSE

Table 2. Opamp circuit results in one generation.

Test vector	PWL representation											Fault coverage (%)
	0.0u	0.5u	1.0u	1.5u	2.0u	2.5u	3.0u	3.5u	4.0u	4.5u	5.0u	
1	0.5	1.0	0.0	-1.0	1.0	1.0	-0.5	-0.5	0.5	0.5	-0.5	86.67
2	0.0	1.0	-1.0	-1.0	1.0	0.5	1.0	0.0	0.5	1.0	1.0	100
3	0.0	1.0	-0.5	-0.5	-1.0	1.0	0.5	0.5	-0.5	-1.0	-1.0	86.67
4	-0.5	-1.0	0.5	0.0	0.0	0.0	0.5	-1.0	0.0	-1.0	0.5	86.67

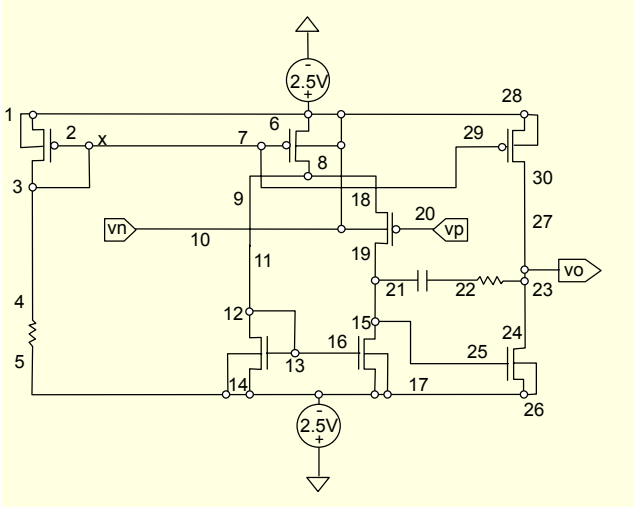

Fig. 4. Benchmark Opamp.

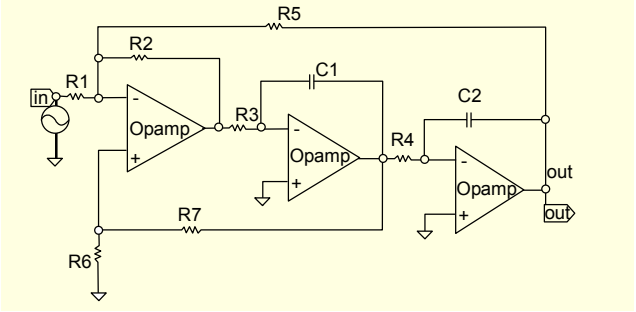

Fig. 5. Benchmark state variable filter.

value lies outside the threshold range, then the test signal is selected as a test signal detecting that particular fault. The number of faults detected by this particular pattern determines its fitness. The test pattern with the highest fitness value, that is, the pattern which detects the maximum number of faults, is the best pattern for the current generation. This pattern will be passed on to the next generation.

Crossover is performed between the best pattern and another pattern in the population. This results in two children. The fitness of each child is calculated as before. Of the two children, the one that is more fit is passed on to the next generation. Thus, the population for the next generation is obtained. This process continues until one of the stopping criteria is met.

The IEEE benchmark circuits, operational amplifier (Opamp) shown in Fig. 4 and state variable filter (SVF) shown in Fig. 5 are taken as CUTs for the proposed test pattern generation. The Opamp is used in non-inverting amplifier mode. The gain and bandwidth are taken as specifications for the operational amplifier circuit, and 10% deviation is fixed as the bound for each specification. The circuit is simulated with these bounds and the limits for the parameters are fixed. The results obtained for the Opamp in one generation are shown in Table 2.

IV. Proposed Fault Detection Method Using PWL Signal

The PWL stimulus generated by the genetic algorithm technique is used as a test stimulus and the circuits are tested. The IEEE benchmark circuits, Opamp, and SVF circuits are taken as CUTs. In the proposed method, the bounds for the parameters are initially fixed based on the satisfaction/violation of the specifications. Then, circuits are simulated based on these bounds. The circuits are simulated with parametric variations using Monte Carlo simulation. The output response is sampled and wavelet analysis is performed. Wavelet coefficients are obtained for fault-free and faulty responses.

1. Fault Detection Using Neural Networks

Artificial intelligence techniques are popularly used in many VLSI problems. In many studies neural networks are used in fault detection and classification problems. In previous works, a back propagation neural (BPN) net and a self organizing map are [4] used for fault classification. In [5], a probabilistic neural network (PNN) is used for the detection of catastrophic faults, but AC current, AC voltage, DC current, and DC voltage are the four measurements used for training the neural network. In [6] and [7], wavelet coefficients are used as preprocessors for the data before the neural network is trained. In these works, a BPN network is used for classification and fault detection is

Table 3. Classification results of operational amplifier using a PNN with catastrophic faults.

Minimum fraction variance (PCA)	Spread	PNN					
		Db1			Coif1		
		%C	%P	%Q	%C	%P	%Q
1%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100
2%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100
5%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100

%C: percentage of correct fault-free classifications
%P: percentage of correct faulty classifications
%Q: average of the percentages of correct fault-free and faulty classifications

Table 4. Classification results of SVF using a PNN with catastrophic faults.

Minimum fraction variance (PCA)	Spread	PNN					
		Db1			Coif1		
		%C	%P	%Q	%C	%P	%Q
1%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100
2%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100
5%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100

done only for parametric faults. In the pseudorandom signal based testing method [8], a PNN produces better results than a BPN network. Therefore, a PNN is used in this proposed testing method to detect both catastrophic and parametric faults.

V. Results and Discussion

1. Catastrophic Fault Detection

As discussed in section IV, the CUTs are tested for fault-free and faulty conditions. Two wavelets Db1 and Coif1 are used for catastrophic fault detection and the results are tabulated in Tables 3 and 4. The proposed test method used to detect catastrophic faults achieves 100% fault coverage in both circuits.

Table 5. Classification results of operational amplifier using a PNN with parametric faults.

Minimum fraction variance (PCA)	Spread	PNN					
		Db1			Coif1		
		%C	%P	%Q	%C	%P	%Q
1%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100
2%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100
5%	0.1	100	100	100	100	100	100
	0.2	100	100	100	100	100	100
	0.3	100	100	100	100	100	100

Table 6. Classification efficiency of various wavelets in SVF.

Wavelet	%C	%P	%Q
Db1	85	100	92.5
Db3	95	100	97.5
Coif1	85	100	92.5
Coif3	100	100	100

2. Parametric Fault Detection

The Opmp circuit and SVF are simulated with parametric faults. The wavelet coefficients obtained from the output response are used in neural networks for parametric fault detection. PNN is also used for parametric fault detection. The results for the operational amplifier using a PNN are tabulated in Table 5.

The classification efficiency of various wavelets for SVF is tabulated in Table 6, and the classification results for SVF are shown in Table 7.

The PWL-based method also achieves a classification efficiency of 100% for parametric fault detection.

The results obtained using the proposed PWL-based testing method are compared with the pseudorandom-based testing method [8]. The results are compared in Table 8. Both methods have 100% fault coverage for catastrophic faults; however, the proposed method has higher fault coverage for parametric faults than the pseudorandom method.

Table 7. Classification results of SVF using PNN with parametric faults.

Minimum fraction variance (PCA)	Spread	PNN		
		Coif3		
		%C	%P	%Q
1%	0.1	100	100	100
	0.2	100	100	100
	0.3	100	100	100
2%	0.1	100	100	100
	0.2	100	100	100
	0.3	100	100	100
5%	0.1	100	100	100
	0.2	100	100	100
	0.3	100	100	100

Table 8. Comparison of results obtained using the pseudorandom and PWL methods.

IEEE bench mark circuits	Catastrophic fault		Parametric fault	
	Pseudo random method	PWL method	Pseudo random method	PWL method
Operational amplifier	100%	100%	94.5%	100%
State variable filter	100%	100%	95%	100%

VI. Conclusion

In the proposed PWL-based testing method, specification driven PWL stimulus is generated using a genetic algorithm. The conventional PWL generation method uses measurements from multiple nodes in the circuit, whereas the proposed PWL generation method takes only the output node measurements. This is a very important feature of the proposed method. When the circuits were tested with generated PWL signal, it was found that the proposed method achieves 100% fault coverage for catastrophic faults and parametric faults present in Analog VLSI circuits.

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