Reliability Characteristics of La-doped High-k/Metal Gate nMOSFETs

C. Y. Kang*, R. Choi, B. H. Lee***, and R. Jammy***

Abstract—**The reliability of hafnium oxide gate dielectrics incorporating lanthanum (La) is investigated. nMOSFETs with metal/La-doped high-k dielectric stack show lower V_{th} and I_{gate}, which is attributed to the dipole formation at the high-k/SiO_2 interface. The reliability results well correlate with the dipole model. Due to lower trapping efficiency, the La-doping of the high-k gate stacks can provide better PBTI immunity, as well as lower charge trapping compared to the control HfSiO stacks. While the devices with La show better immunity to positive bias temperature instability (PBTI) under normal operating conditions, the threshold voltage shift (ΔV_{th}) at high field PBTI is significant. The results of a transconductance shift (ΔG_m) that traps are easily generated during high field stress because the La weakens atomic bonding in the interface layer.**

Index Terms—**La-doped high-k/metal gate nMOSFETs**

I. INTRODUCTION

High-k gate dielectrics have been studied as alternative gate dielectrics for the 45 nm technology nodes and beyond to replace conventional SiO_2 or silicon oxynitrides (SiO_xN_y) and have been successfully implemented in CMOS integrations [1, 2]. Hf-based oxides, including HfO_2 and $HfSiO_x$, have been regarded as promising candidates for high-k dielectrics because of their excellent thermal stability with Si. Furthermore, the mobility of HfSiON devices, which was underestimated due to transient charging during conventional characterrization, has improved significantly by dielectric stack optimization based on better understanding of transient charging behaviors in high-k [3-6].

In conjunction with high-k dielectrics, a band-edge metal solution for n- and pMOSFETs is being pursued because it is known that polySi/high-k stacks are limited by dopant penetration, inversion oxide thickness (T_{inv}) scalability, threshold voltage (V_{th}) controllability by Fermi-level pinning, and poor reliability [7-11]. Various attempts have been made in material screening to find proper band-edge electrode materials [8, 12, 13].

Besides pursuing a band-edge metal solution, a simple rare-earth metal doping technique has been proposed to modulate V_{th} [14-17]. Among various rare-earth metals, lanthanum has been demonstrated as a strong candidate for nMOSFETs because of its low V_{th}, good carrier mobility, good EOT scaling, and positive bias temperature instability (PBTI). During a high temperature dopant activation step, electropositive La that has diffused into the high-k/SiO_2 interface forms a dipole, which shifts the band offset and thereby the effective work function (EWF) of the electrode. To explain the V_{th}/flatband voltage (V_{fb}) modulation HfO_2 or HfSiO incorporaating La, various models were proposed, such as a positive charge by oxygen vacancy and interface dipoles [15-20]. Unlike the V_{th}/V_{fb} modulation caused by additional positive charge generation/increase in the dielectric, devices with La show excellent carrier mobility due to the short range of the dipole electric field [15, 16].

Manuscript received Jun. 1, 2009; revised Aug. 28, 2009.
* SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, USA
** Inha University, Inchon, Korea
*** Dept. of Nanobio Materials Electronics and Dept. of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangji, Korea
TEL: (512) 356-3527
E-mail:Chang.Yong.Kang@sematech.org

Thus, HfO_2 gate dielectric incorporating La seems to be a strong candidate for future nMOS dielectrics, but the effects of the La-induced dipole on device performance and dielectric reliability have not been studied thoroughly. Reliability studies of high-k dielectrics are focusing on understanding mechanisms of how and where defects are generated using various characterization methods [3, 21-27] and it is reported that interface trap generation rather than the bulk high-k layer is very crucial to dielectric reliability [28, 29]. In this work, therefore, we investigate the reliability of nMOSFETs with HfO_2 dielectrics that incorporate La, whose device performance and V_{th} are suitable for future technology node applications. We especially focus on how incorpo-rating La into the interfacial layer affects dielectric reliability.

II. EXPERIMENTAL

Transistors were fabricated using a gate-first integration flow. Hf-silicate films with different SiO_x concentrations were deposited by atomic layer deposition (ALD). A molecular beam deposition (MBD) process was employed to deposit an ultra thin LaO_x cap on the high-k film before depositing the metal gate electrode. Post high-k deposition treatments included a post-nitridation anneal. Mobility was extracted from 10 μm x 1 μm transistors using the NCSU CVC and mob2d models [30]. For comparison, control HfSiO devices were fabricated without the LaO_x cap. The equivalent oxide thicknesses (EOTs) for the sample devices were in the 0.85 ~ 1.02 nm range (Table 1).

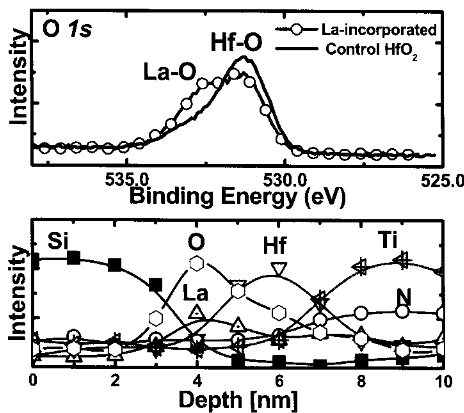


Fig. 1. XPS analysis shows that by incorporating La, LaOx segregation has occurred after high temperature anneal. La piled up near the HfO_2/SiO_2 interface from the EELS analysis [31].

Table 1. Split conditions of HfSiO & Electrical parameters.

SiO	La	PDA	EOT[nm]	V_{FB}[V]
10%	X	700°C, NH_3	0.89	-0.58
	O		0.95	-0.85
80%			1.02	-0.93

X-ray photoelectron spectroscopy (XPS) analysis shows that LaO/HfO phase segregation/separation occurs after the thermal process (Fig. 1). Electron energy-loss spectroscopy (EELS) analysis confirmed that La accumulates near the high-k/SiO_2 interface by the end of the device fabrication process [2].

III. RESULTS AND DISCUSSION

In the La-doped HfSiO samples with 10% SiO_x, V_{FB} and V_{th} are shifted to the negative direction by about 300 mV, which is due to the La-dipole formation as shown in Fig. 2. EELS analysis in Fig. 1 showed that the

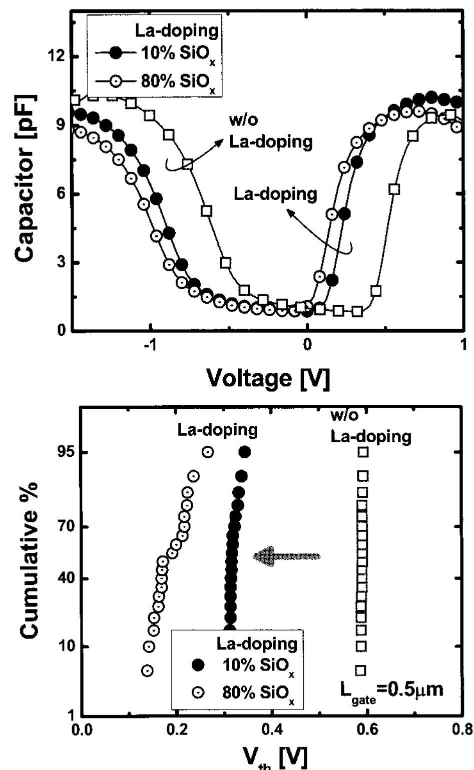
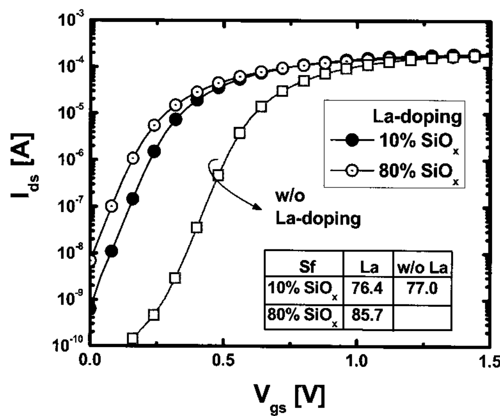


Fig. 2. Transistor CV curves for La-doped samples are shifted to negative direction due to La-dipole formation. For the 80% SiO_x, EOT was increased due to reduced dielectric constant. Vth for the 80% SiO_x shows lowest. It appears to be due to oxygen vacancy or more strong La-Si dipole formation [30].

La deposited on the high-k layer piled up at the interface between the SiO_x and high-k layer. To modulate V_{fb} and V_{th}, the location of La is known to be critical, i.e., no V_{th} shift was observed when the La was at the top of the high-k layer [18]. Once the La diffuses down to the interface layer, the La-O-Si configuration is formed resulting in an interface dipole formation by a charge transfer [15, 18].

In the 80% SiO_x samples, the V_{th} is further reduced in spite of an EOT increase due to reduced dielectric constant. The transistor subthreshold slopes (S_f) for the control (no La doping) and sample transistors (both have 10% SiO_2 HfSiO dielectric) exhibit similar value of 77 mV/dec. However, higher S_f is observed in the 80% SiO_x devices (Fig. 3). This increased subthreshold slope is attributed to the interface states density (N_{it}) increase confirmed by the charge pumping measurements (Fig. 4).



Sf	La	w/o La
10% SiOx	76.4	77.0
80% SiOx	85.7	

Fig. 3. For the 10% SiO_x devices, the both w and w/o La-doping show similar subthreshold slope (Sf). However, the increased Sf is observed for the 80% SiO_x [30].

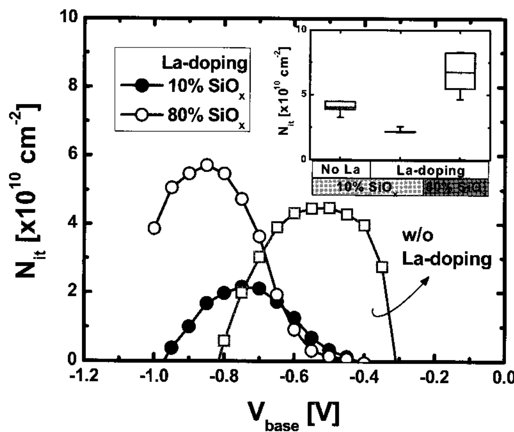


Fig. 4. By incorporating La, interface states density was decreased. By increasing SiO_x content, Nit was increased [30].

For the 10% SiO_x devices, the interface state density decreased slightly after La incorporation. The 10% SiO_x with La doping exhibits slightly reduced carrier mobility in the low and intermediate field regime compared to the control device (Fig. 5) because the dipole field induces additional carrier scattering even though 300 mV of the V_{th} was shifted in the device with La. This excellent low-field mobility cannot be explained by positive charge incorporation. In addition, the interface state densities from the devices incorporating La are even lower than the control samples. Therefore, interface dipole formation from adding La is believed to be the primary cause of the V_{th} and mobility characteristics. Previous reports proposed a dipole-induced band-offset model to explain the V_{th} shift [16, 18, 31]. Various material screening experiments in search of a band-edge solution have indicated that the interface dipole field is related to the electro-negativity of rare-earth metal elements [15, 16]. If this is true, this band-offset model will be proved by the gate leakage behavior. For the 80% SiO_x devices, mobility degraded significantly. The lower V_{th} and carrier mobility (higher N_{it} and S_f) for the 80% SiO_x sample appear to be due to ① the stronger La-Si dipole formation or ② positive charges [6].

A previous La-doped HfO_2 study reported that the La dipole led to an increase in the effective barrier height for the substrate injection, which resulted in reduced gate leakage currents. In this study, the gate leakage at V_{ox}=+1.2 V for the La-doped samples was also reduced due to an offset in barrier height (Fig. 6 and 7). However, the gate leakage difference for the different SiO_x content

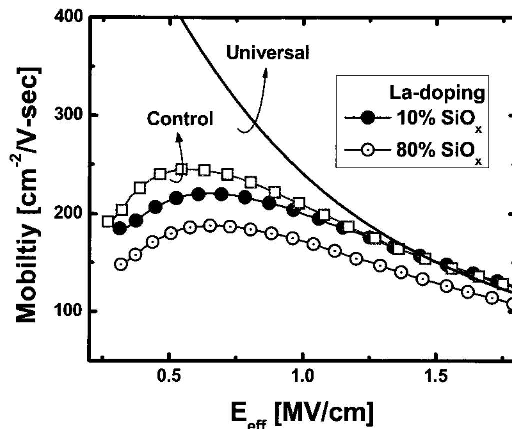


Fig. 5. For 10% SiO_x samples, the reason of reduced carrier mobility at low and intermediate field regime is dipole field even though lower N_{it} [30].

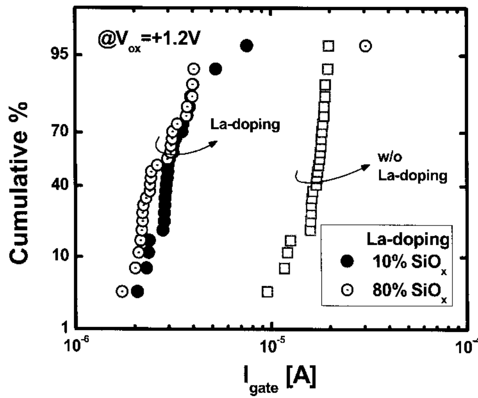


Fig. 6. At V_{ox}=+1.2 V, La-doping reduced gate leakage due to an offset of barrier height [30].

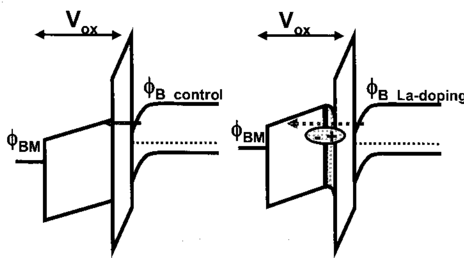


Fig. 7. The La-induced dipole formation between the interface and high-k retarded the injected charges [30].

was not significant. If the larger V_{th} shift for the 80% SiO_x was related to the greater dipole formation, the gate leakage would be lower than that of 10% SiO_x samples, which suggest that La doping results in a positive charge as well.

In previous studies of La-doped high-k dielectrics, the high-k dielectric stacks with La showed better PBTI reliabilities [14, 16]. Other studies reported that incurporating La provided better PBTI immunity at lower bias conditions but reliability under high gate stress field conditions became worse [31, 32]. In the positive bias temperature instabilities (PBTI) under the same gate overdrive stress conditions, both types of La-doped devices showed smaller V_{th} shifts. At lower V_{ox} (<1.4 V) condition, La-doping can result in less V_{th} shift because of reduced trapping efficiency, as shown Fig. 8 and 9. With increasing stress voltage (V_{ox}>1.8 V), however, all devices showed a similar ΔV_{th}. The similar ratio of $Q_{trapped}$ to Q_{inj} indicates that intrinsic charge trapping is similar regardless of La doping and SiO_2 concentration, as shown in Fig. 10. At a lower gate stress voltages, G_m degradation was similar. With increased gate stress voltage, however, G_m in both La-doped samples degraded more, indicating that the interface degradation becomes more significant and time-dependent dielectric breakdown (TDDB) characteristics may be worsen (See Fig. 11). From the TDDB test at a higher gate stress as shown in Fig. 12, La-doped samples show shorter time to breakdown, which are attributed to lower interface quality, most probably associated with the presence of

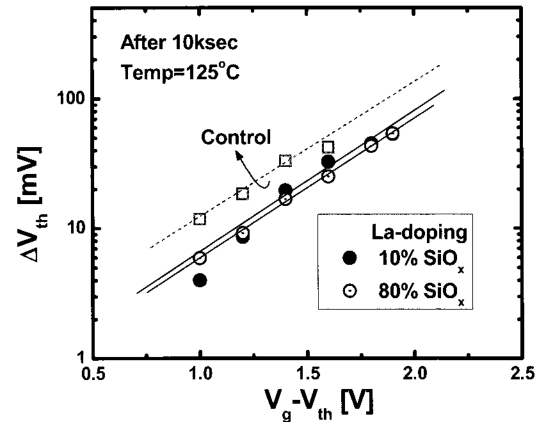


Fig. 8. At same gate overdrive stress conditions, La-doping showed less V_{th} shift. For the 80% SiO_x, lowest V_{th} was observed [30].

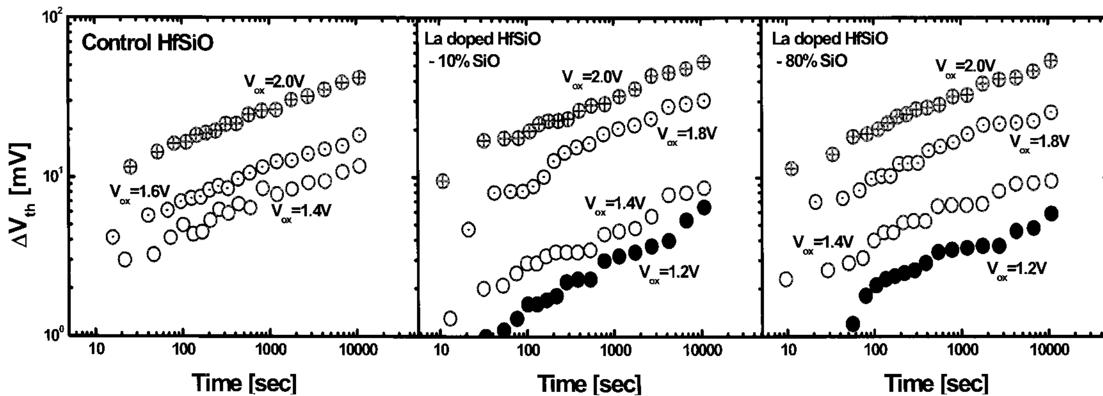


Fig. 9. At lower V_{ox} (<1.4 V) condition, La-doping can induce less V_{th} shift because of reduced trapping efficiency. With increasing stress voltage (V_{ox}>1. V), however, all devices showed similar V_{th} shift [30].

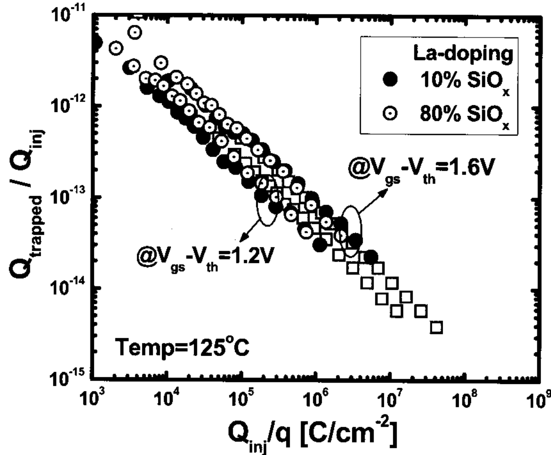


Fig. 10. Similar ratio of $Q_{trapped}$ to Q_{inj} indicates that intrinsic charge trapping are similar regardless of La-doping and SiO_x concentration [30].

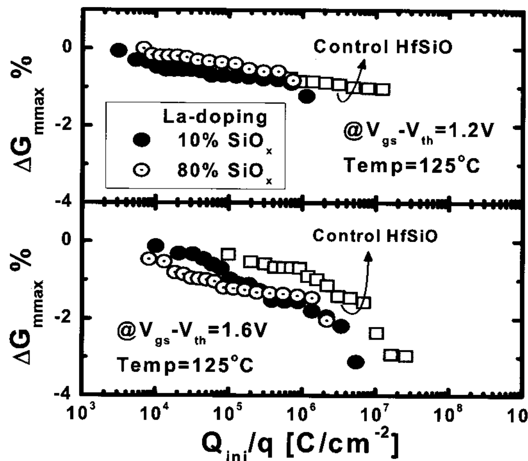


Fig. 11. At lower gate stress, G_m degradation was similar. With increasing the gate stress voltage, La-doped samples showed more G_m degradation, indicating that the interface degradation becomes more significant [30].

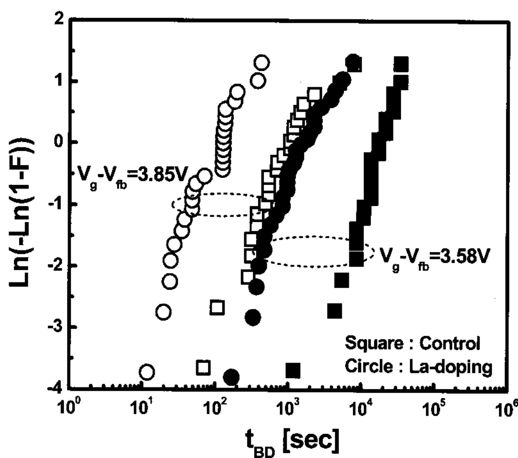


Fig. 12. La-doping can degrade TDDB characteristics due to more interface degradation at higher voltage stress conditions [31].

La atoms. Considering the operation conditions for the devices of the 32 nm technology node and below, however, the degradation of La-doped devices is expected to be less severe and it might be comparable to the control devices.

IV. CONCLUSIONS

La-doped HfSiO samples showed lower V_{th} and I_{gate}, which was attributed to the dipole formation at the high-k/SiO_2 interface. With increasing SiO_x content, significant mobility degradation was observed, most likely due to additional La-related charges in the interfacial layer. La-doped devices demonstrate better immunity in the PBTI test and low charge trapping efficiency compared to the control HfSiO.

From the results above, the key factor for improving high field reliability is to mitigate the accumulation of La in the bottom interface layer. However, this can increase the nMOSFET V_{th}. With a given condition for incorporating La while maintaining a target V_{th}, interface engineering to obtain a more robust interface will be a key factor in reliability.

REFERENCES

[1] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Rarade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2007, pp. 247-250.

[2] M. T. Bohr, R. S. Chau, T. Ghani, and K. Mistry, "The high-k solution," *IEEE Spectrum,* Vol. 44, pp. 29-35, 2007.

[3] B. H. Lee, C. D. Young, R. Choi, J. H. Sim, G. Bersuker, C. Y. Kang, R. Harris, G. A. Brown, K. Matthews, and S. C. Song, "Intrinsic characteristics of high-k devices and implications of fast transient charging effects (FTCE)," *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International,* pp. 859-862, 2004.

[4] C. Y. Kang, R. Choi, J. H. Sim, C. Young, B. H. Lee, G. Bersuker, and J. C. Lee, "Charge trapping effects in HfSiON dielectrics on the ring oscillator circuit and the single stage inverter operation," in *Technical Digest - International Electron Devices Meeting, IEDM,* San Francisco, CA, 2004, pp. 485-488.

[5] C. D. Young, G. Bersuker, D. Heh, A. Neugroschel, R. Choi, C. Y. Kang, J. Tun, and B. H. Lee, "Electrical characterization methodologies for the assessment of high-? gate dielectric stacks," in *ECS Transactions*, Washington, DC, 2007, pp. 335-346.

[6] A. Kerber, E. Cartier, R. Degraeve, P. J. Roussel, L. Pantisano, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Charge trapping and dielectric reliability of SiO2-Al2O3 gate stacks with TiN electrodes," *IEEE Transactions on Electron Devices,* Vol. 50, pp. 1261-1269, 2003.

[7] J. Lee, H. Park, H. Choi, M. Hasan, M. Jo, M. Chang, B. H. Lee, C. S. Park, C. Y. Kang, and H. Hwang, "Modulation of TiSiN effective work function using high-pressure postmetallization annealing in dilute oxygen ambient," *Applied Physics Letters,* Vol. 92, 2008.

[8] S. C. Song, Z. B. Zhang, M. M. Hussain, C. Huffman, J. Barnett, S. H. Bae, H. J. Li, P. Majhi, C. S. Park, and B. S. Ju, "Highly manufacturable 45 nm LSTP CMOSFETs using novel dual high-k and dual metal gate CMOS integration," *VLSI Symp. Tech. Dig,* 2006.

[9] S. Abermann, J. Efavi, G. Sjöblom, M. Lemme, J. Olsson, and E. Bertagnolli, "Impact of Al-, Ni-, TiN-, and Mo-metal gates on MOCVD-grown HfO2 and ZrO2 high-k dielectrics," *Microelectronics Reliability,* Vol. 47, pp. 536-539, 2007.

[10] Y. H. Kim, R. Choi, R. Jha, J. H. Lee, V. Misra, and J. C. Lee, "Effects of barrier height (ΦB) and the nature of Bi-layer structure on the reliability of high-k dielectrics with dual metal gate (Ru & Ru-Ta alloy) technology," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2004, pp.138-139.

[11] Y. T. Hou, T. Low, B. Xu, M. F. Li, G. Samudra, and D. L. Kwong, "Impact of metal gate work function on nano CMOS device performance," in *International Conference on Solid-State and Integrated Circuits Technology Proceedings, ICSICT,* 2004, pp. 57-60.

[12] M. M. Hussain, C. Smith, P. Kalra, J. W. Yang, G. Gebara, B. Sassman, P. Kirsch, P. Majhi, S. C. Song, R. Harris, H. H. Tseng, and R. Jammy, "Dual work function high-k/metal gate CMOS FinFETs," in *ESSDERC 2007 - Proceedings of the 37th European Solid-State Device Research Conference,* 2008, pp. 207-209.

[13] C. Y. Ren, H. Y. Kang, J. F. Wang, X. P. Ma, H. Chan, D. S. H. Li, and M. F. Kwong, "A dual-metal gate integration process for CMOS with sub-1-nm EOT HfO/sub 2/by using HfN replacement gate," *Electron Device Letters, IEEE,* Vol. 25, pp. 580-582, 2004.

[14] P. D. Kirsch, M. A. Quevedo-Lopez, S. A. Krishnan, C. Krug, H. AlShareef, C. S. Park, R. Harris, N. Moumen, A. Neugroschel, and G. Bersuker, "Band Edge n-MOSFETs with High-k/Metal Gate Stacks Scaled to EOT= 0.9 nm with Excellent Carrier Mobility and High Temperature Stability," *Electron Devices Meeting, 2006. IEDM'06. International,* pp. 1-4, 2006.

[15] P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker, H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H. H. Tseng, R. Jammy, T. S. Boscke, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, "Dipole model explaining high-k/metal gate field effect transistor threshold voltage tuning," *Applied Physics Letters,* Vol. 92, p. 092901, 2008.

[16] P. Sivasubramani, T. S. Böscke, J. Huang, C. D. Young, P. D. Kirsch, S. A. Krishnan, M. A. Quevedo-Lopez, S. Govindarajan, B. S. Ju, H. R. Harris, D. J. Lichtenwalner, J. S. Jur, A. I. Kingon, J. Kim, B. E. Gnade, R. M. Wallace, G. Bersuker, B. H. Lee, and R. Jammy, "Dipole moment model

explaining nFET vt tuning utilizing La. Sc, Er, and Sr doped HfSiON dielectrics," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2007, pp. 68-69.

[17] X. P. Wang, L. Ming-Fu, C. Ren, X. F. Yu, C. Shen, H. H. Ma, A. Chin, C. X. Zhu, N. Jiang, M. B. Yu, and K. Dim-Lee, "Tuning effective metal gate work function by a novel gate dielectric HfLaO for nMOSFETs," *Electron Device Letters, IEEE,* vol. 27, pp. 31-33, 2006.

[18] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, "Study of La-induced flat band voltage shift in metal/HfLaO x/SiO2/Si capacitors," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers,* Vol. 46, pp. 7251-7255, 2007.

[19] Y. Abe, N. Miyata, Y. Shiraki, and T. Yasuda, "Dipole formation at direct-contact Hf O2 Si interface," *Applied Physics Letters,* Vol. 90, 2007.

[20] B. J. O. Sullivan, R. Mitsuhashi, G. Pourtois, M. Aoulaiche, M. Houssa, N. V. d. Heyden, T. Schram, Y. Harada, G. Groeseneken, P. Absil, S. Biesemans, T. Nakabayashi, A. Ikeda, and M. Niwa, "Reliability study of La[sub 2]O[sub 3] capped HfSiON high-permittivity n-type metal-oxide-semiconductor field-effect transistor devices with tantalum-rich electrodes," *Journal of Applied Physics,* Vol. 104, p. 044512, 2008.

[21] B. H. Lee, C. Y. Kang, T. H. Lee, J. Barnett, R. Choi, S. C. Song, and R. Jammy, "Reliability of thich oxides integrated with HfSiO~ x gate dielectric," *SOLID STATE DEVICES AND MATERIALS,* Vol. 2006, p. 1122, 2006.

[22] K. Okada, H. Ota, W. Mizubayashi, H. Satake, A. Ogawa, K. Iwamoto, T. Horikawa, T. Nabatame, and A. Toriumi, "Quantitative analysis of contribution of initial traps to breakdown in HfAlOx/SiO2 stacked gate dielectrics," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2005, pp. 166-167.

[23] K. Okada, H. Ota, T. Nabatame, and A. Toriumi, "Dielectric breakdown in high-K gate dielectrics - Mechanism and lifetime assessment," in *Annual Proceedings - Reliability Physics (Symposium)*, 2007, pp. 36-43.

[24] G. Ribes, S. Bruye?re, M. Denais, F. Monsieur, D. Roy, E. Vincent, and Ghibaudo, "High-k dielectrics breakdown accurate lifetime assessment methodology," in *IEEE International Reliability Physics Symposium Proceedings*, 2005, pp. 61-66.

[25] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-k dielectrics reliability issues," *IEEE Transactions on Device and Materials Reliability,* Vol. 5, pp. 5-19, 2005.

[26] J. H. Sim, B. H. Lee, R. Choi, S. C. Song, and G. Bersuker, "Hot carrier degradation of HfSiON gate dielectrics with TiN electrode," *IEEE Transactions on Device and Materials Reliability,* Vol. 5, pp. 177-182, 2005.

[27] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Threshold voltage instabilities in high-? gate dielectric stacks," *IEEE Transactions on Device and Materials Reliability,* Vol. 5, pp. 45-64, 2005.

[28] A. Neugroschel, G. Bersuker, R. Choi, C. Cochrane, P. Lenahan, D. Heh, C. Young, C. Y. Kang, B. H. Lee, and R. Jammy, "An accurate lifetime analysis methodology incorporating governing NBTI mechanisms in high-k/SiO2 gate stacks," in *Technical Digest - International Electron Devices Meeting, IEDM,* 2006.

[29] G. Bersuker, J. H. Sim, C. S. Park, C. D. Young, S. Nadkarni, R. Choi, and B. H. Lee, "Intrinsic Threshold Voltage Instability of the HFO2 NMOS Transistors," *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International,* pp. 179-183, 2006.

[30] E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman, "Modeled tunnel currents for high dielectric constant dielectrics," *IEEE Transactions on Electron Devices,* Vol. 45, pp. 1350-1355, 1998.

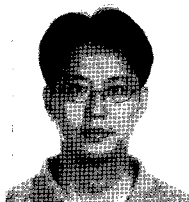
[31] C. Y. Kang, C. S. Park, D. Heh, C. Young, P. Kirsch, H. B. Park, R. Choi, G. Bersuker, J. W. Yang, B. H. Lee, J. Lichtenwalner, J. S. Jur, A. I. Kingon, and R. Jammy, "Performance and reliability characteristics of the band edge high-k/metal gate nMOSFETs with La-doped Hf-silicate gate dielectrics," in *IEEE International Reliability Physics Symposium Proceedings*, 2008, pp. 663-664.

[32] C. Y. Kang, C. D. Young, J. Huang, P. Kirsch, D. Heh, P. Sivasubramani, H. K. Park, B. G, B. H. Lee, H.S. Choi, K.T. Lee, Y-H. Jeong, J. Lichtenwalner, A. I. Kingon, H-H Tseng, and R. Jammy, "The Impact of La-doping on the Reliability of Low Vth High-k/Metal Gate nMOSFETs under Various Gate

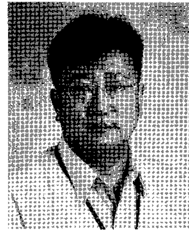
Stress Conditions," in *Technical Digest – International Electron Devices Meeting*, 2008, pp. p.115-118.

Chang Yong Kang received a B.S. (1993) and a M.S. (1995) from Hanyang University, Seoul, Korea and Ph.D (2005) in electrical and computer engineering from the University of Texas at Austin. He worked at Hynix, former LG Semicon (1995-2001), where he was involved in DRAM, high performance and low standby power logic devices design and he covered device characteri-zation, TCAD/Spice modeling and process integration. Since 2005, he is with SEMATECH as a senior technical staff. He has authored and co-authored over 100 peer-reviewed journal and conference papers in the various semiconductor research areas including gate oxide reliability, SOI FinFET device and process, strained silicon devices, alternative channel device, and high-k/ metal gate process and devices.

Dr. Kang is the recipient of the 2008 SSDM Best Paper Award. He is a senor member of IEEE and his name was listed on Marquis Who's Who in Science and Engineering and Marquis Who's Who in the World. Also, he serves as a reviewer for various technical journals such as TED, EDL, APL, JAP, Thin Solid Film, etc. Currently, he is a technical committee member of IEEE ICMTS.



Rino Choi received his Bachelor of Science and Master of Science degree in the Department of Inorganic Materials Engineering of the Seoul National University in 1992 and 1994, respectively. He received the Ph.D. in Materials Science and Engineering Program in 2004 from the University of Texas at Austin. He worked for Daewoo Motors Company from 1994 to 1999, where he worked as a development and test engineer. Since 1999, he studied various high-k dielectrics and published more than 100 journal and conference papers. After his completion of his Ph.D, he worked on the electrical characterization and reliability of advanced gate stacks at SEMATECH. Since September, 2007, he is with School of Materials Science and Engineering, Inha University, Korea. He is an IEEE senior member and serves as a guest editor and executive committee member in several major journals and conferences.



Byoung Hun Lee received a B.S. (1989) and a M.S. (1992) in Physics from Korea Advanced Institute of Science and Technology and Ph.D (2000) in electrical and computer engineering from the University of Texas at Austin. He worked at Samsung semiconductor (1992-1997) and has been with IBM since 2001. He has authored and co-authored more than 220 journal and conference papers in the various semiconductor research areas including gate oxide reliability, SOI device and process, strained silicon devices, and high-k/ metal gate process and devices. He is a senor member of IEEE and a member of the Electrochemical Society. He was on the assignment to SEMATECH as a manager of advanced gate stack program, managing high-k dielectric project, metal electrode project, material evaluation test structure project and electrical characterization project. Since 2008, he joined Gwangju Institute of Science and Technology, Korea as a faculty member.

Rajarao "Raj" Jammy graduated with a doctoral degree in Electrical Engineering from Northwestern University in November 1996. He then joined IBM's Semiconductor Research and Development Center in East Fishkill, NY, where he worked on development of ultra-thin dielectrics, advanced doping techniques and other front end of line technologies for deep trench DRAMs. In January 2001 he was appointed as Manager of the Thermal Processes, and Surface Preparation group with additional responsibilities in CMP, Thin Films and Metallization in the DRAM development organization. He moved to IBM T. J. Watson Research Center in Yorktown Heights, NY in June 2002 to manage IBM's efforts on high k gate dielectrics and metal gates. Between June 2005 and June 2008 he was an IBM assignee to SEMATECH as the Director of the Front End Processes Division in Austin, TX.

In June 2008 he joined SEMATECH staff after the completion of his assignment from IBM. As SEMATECH staff his responsibilities were expanded, and he currently serves as the Vice President of Emerging Technologies. He holds more than 50 patents and is an author/co-author of over 125 publications/presentations.