A CMOS Frequency Synthesizer for 5~6 GHz UNII-Band Sub-Harmonic Direct-Conversion Receiver

Chan-Young Jeong and Changsik Yoo

Abstract—**A CMOS frequency synthesizer for 5~6 GHz UNII-band sub-harmonic direct-conversion receiver has been developed. For quadrature down-conversion with sub-harmonic mixing, octa-phase local oscillator (LO) signals are generated by an integer-N type phase-locked loop (PLL) frequency synthesizer. The complex timing issue of feedback divider of the PLL with large division ratio is solved by using multi-modulus prescaler. Phase noise of the local oscillator signal is improved by employing the ring-type LC-tank oscillator and switching its tail current source. Implemented in a 0.18 μm CMOS technology, the phase noise of the LO signal is lower than -80 dBc/Hz and -113 dBc/Hz at 100 kHz and 1MHz offset, respectively. The measured reference spur is lower than -70 dBc and the power consumption is 40 mW from a 1.8 V supply voltage.**

Index Terms—**Frequency synthesizer, integer-n type, voltage controlled oscillator (VCO), multi-modulus prescaler, phase noise, reference spur**

I. INTRODUCTION

Among various kinds of wireless receiver architecture, direct-conversion receiver (DCR) offers the highest level of integration and low-power operation [1, 2]. However, DCR suffers the impairments due to the flicker noise, DC-offset, and second-order distortion. The DC-offset resulting from the self-mixing due to the LO leakage can be greatly reduced by generating the LO signal in smart ways. If the VCO oscillates at twice the LO frequency, the leakage of the VCO output does not produce any DC-offset [3]. But, the oscillation frequency of the VCO can be too high in some applications. Another way is to use a quadrature VCO oscillating at two-thirds of the required LO frequency and a divide-by-two circuit producing the one-third of the LO frequency [4]. If the two outputs of the VCO and divide-by-two circuit are mixed by a single-side-band mixer, we can generate the required quadrature LO signals. This method, however, can result in large power consumption because of the many building blocks operating at high frequency.

If the direct down-conversion is performed by sub-harmonic mixer in which the effective frequency mixing appears between input RF signal and harmonic of applied LO signal, the required LO frequency becomes the half the RF frequency of the normal DCR architecture [5, 6]. Therefore, there is no DC-offset due to the

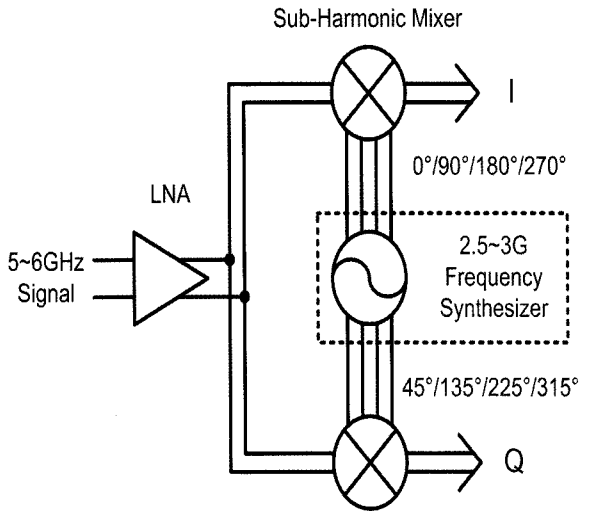

Fig. 1. Sub-harmonic direct-conversion receiver for 5~6GHz UNII-band.

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LO leakage by self-mixing. Fig. 1 shows the 5~6 GHz UNII-band DCR employing the sub-harmonic mixing. The required LO frequency is 2.5~3 GHz and octa-phase LO signals are required for quadrature down-conversion. This paper presents the design of an integer-N frequency synthesizer for the 5~6 GHz DCR with sub-harmonic down-conversion architecture.

Section II describes the architecture of the frequency synthesizer and Section III presents the design of each building block. The experimental results of the frequency synthesizer fabricated in a 0.18 μm CMOS technology is given in Section IV and the paper is concluded in Section V.

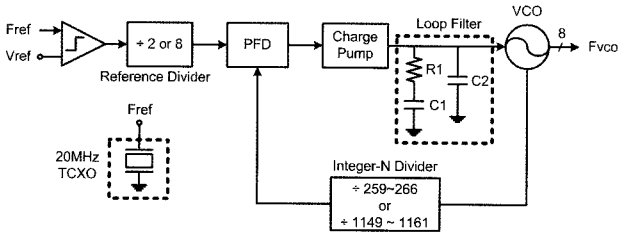


Fig. 2. Architecture of the frequency synthesizer.

II. Frequency Synthesizer Architecture

Because the channel spacing of the targeted 5~6 GHz UNII-band RF receiver is 20 MHz, there is no need to use fractional-N type phase locked loop (PLL) and the simple integer-N type PLL can provide sufficient performance. Fig. 2 shows the block diagram of the frequency synthesizer for the 5~6 GHz sub-harmonic DCR. Because the channel spacing is 20 MHz and the DCR has sub-harmonic down-conversion architecture, the frequency spacing of the frequency synthesizer output is 10MHz. The 5~6 GHz UNII-band is divided into lower (5.15~5.35 GHz) and upper band (5.725~5.825 GHz) and thus the reference frequency should be different for lower and upper bands. The external TCXO (temperature compensated crystal oscillator) output of 20 MHz is divided by an on-chip reference divider to generate 10 MHz and 2.5 MHz reference frequency, respectively for the lower and upper band. The VCO is of ring-type four-stage LC-tank oscillator to generate the octa-phase outputs [7, 8].

III. Circuit Implementation

1. Ring-type LC-VCO

Octa-phase LO signals can be generated by passing a single-phase signal through a passive poly-phase filter (PPF) but the phase noise performance will be degraded due to the power loss in the PPF. Also, QVCO usually shows poorer phase noise performance because the phase shift of the LO resonator of the QVCO is not zero at the oscillation condition and thus its quality factor is degraded [9]. In this work, a ring-type four-stage LC-VCO shown in Fig. 3 is used instead to have low phase noise. Because the VCO has four cascaded stages, cross-coupled pMOS differential pair with small bias current can provide enough gain ensuring oscillation.

For a single-phase LC-VCO, it has been shown the phase noise can be greatly improved if the tail current source is switched on and off because the trapped electrons causing the 1/f noise are released periodically [10, 11]. The same principle can also be applied to this ring-type LC-VCO. As is clear in Fig. 3, the biasing transistors of each stage are switched on and off by the input signals DN and DP. Of course, the biasing transistors of each stage can also be switched on and off by the output signals CN and CP. But, it is found the minima of the common-source node voltage Vc are aligned

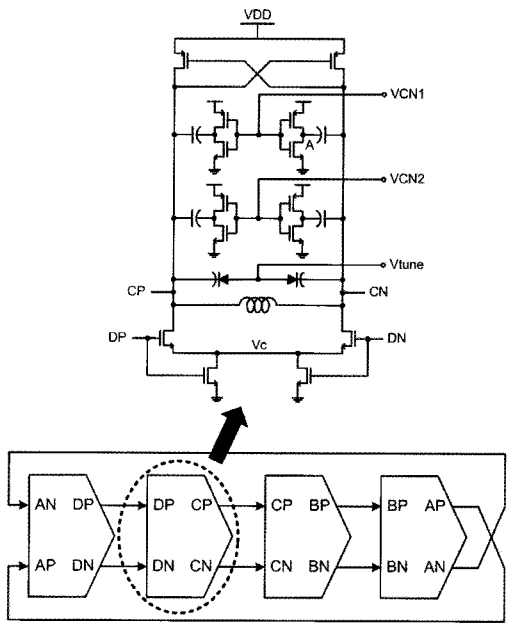


Fig. 3. Ring-type octa-phase LC-tank VCO.

with the minima of the outputs CN and CP if the biasing transistors are switched by the input signal DN and DP [12]. If the minima of the outputs are aligned with the minima of the common-source node, the output swing is maximized and therefore the phase noise is improved.

In order to have a wide frequency tuning range with small VCO gain (Kvco) for low phase noise, two bit digital input, VCN1 and VCN2, coarsely controls the oscillation frequency with capacitor bank. VCO used inverter type switches to control 2-bit capacitor bank. The capacitor bank can be controlled by an automatic frequency calibration (AFC) circuit before the PLL locks the VCO frequency to the reference clock [13].

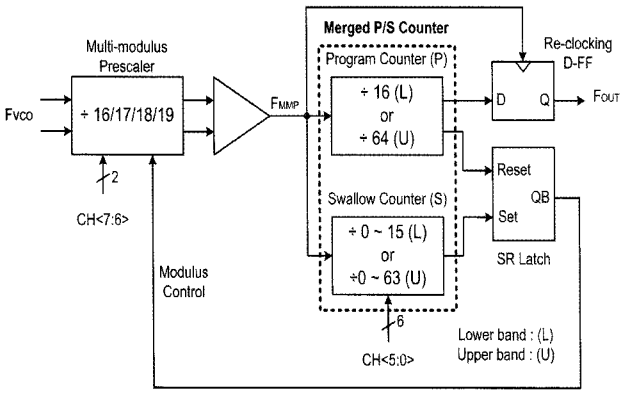


Fig. 4. Integer-N divider with the multi-modulus prescaler.

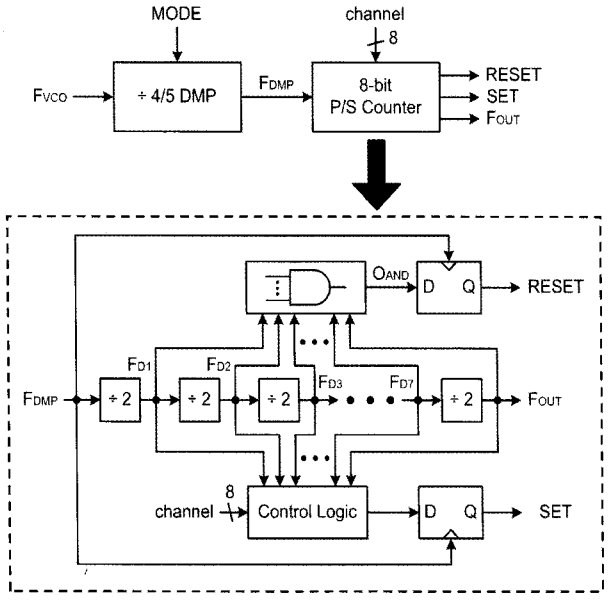


Fig. 5. Conventional implementation of divider with DMP and P/S counter for upper band.

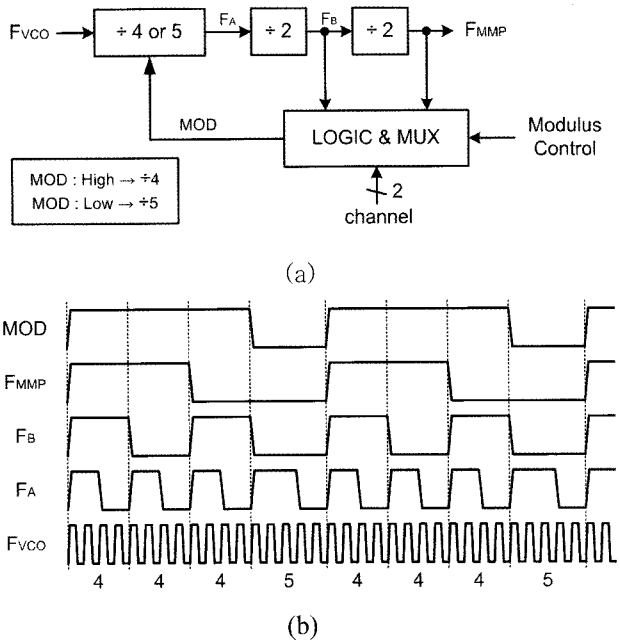


Fig. 6. (a) Block diagram of the MMP and (b) timing diagram of the MMP when the modulus is 17.

2. Integer-N Divider with Multi-Modulus Prescaler

Fig. 4 shows the block diagram of the proposed integer-N divider which employs the multi-modulus prescaler (MMP) instead of widely used dual-modulus prescaler (DMP) to simplify the timing issue in designing the divider with division ratio spanning a wide range. The ÷16/17/18/19 prescaler is followed by a ÷16/64 program counter and ÷0~15/63 swallow counter to provide the division ratio of 259~266 and 1149~1161 in the lower and upper band, respectively. A channel is selected by 8-bit digital input CH<7:0> where CH<7:6> and CH<5:0> control the modulus of the MMP and division ratio of the program & swallow (P/S) counter, respectively.

Of course, the integer-N divider can also be implemented with a DMP as shown in Fig. 5. The large division ratio, however, can result in large asynchronous delay of the P/S counter, which can lead to the incorrect operation of the divider. In Fig. 5, ÷4/5 DMP and ÷256 P/S counter are used to realize the required division ratio. If larger modulus number is used in the DMP, it is impossible to realize all the division ratios required in this work. Because the ÷256 P/S counter is implemented by a cascade of 8 asynchronous divide-by-two circuits, the delay from the input to the output of the P/S counter is very large and can be almost equal to or even larger

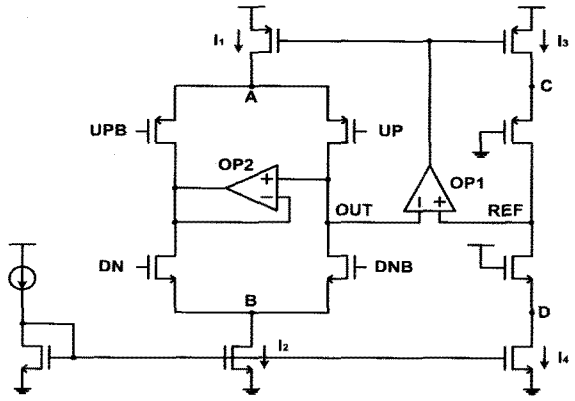


Fig. 7. Used charge pump ensuring equal up and down currents.

than the period of the input clock, F_{DMP}. Then, the P/S counter can generate incorrect pulse of SET or RESET signal, which results in wrong division ratio.

Due to the large delay from F_{DMP} to F_{OUT}, the AND-gated output, O_{AND} is temporarily set to high and O_{AND} is latched by the rising edge of F_{DMP}, which generates the incorrect pulse of RESET signal. To solve this problem, the delay from the input to the output of the P/S counter should be smaller than the period of F_{DMP}. For this, we have employed the ÷16/17/18/19 MMP [14, 15]. Because of the large modulus number, the period of the input clock of the P/S counter, F_{DMP}, is increased and the division ratio of P/S counter becomes smaller. Therefore, the delay from the input to the output of the P/S counter is now much smaller than the period of F_{MMP} and there is no incorrect pulse of SET and RESET signal.

The block diagram of the MMP is shown in Fig. 6 (a). Because the cycle time of F_{MMP} is four times larger than that of F_A which is the output of the divide-by-4/5 circuit, the division ratio of the divide-by-4/5 circuit can change four times per one cycle of F_{MMP}. Therefore, it is possible to realize the modulus number of 16/17/18/19 by controlling the signal MOD appropriately. For example, MOD is high for three periods of F_A and low for one period to have the modulus of 17 as shown in Fig. 6 (b).

3. Charge Pump

The mismatch in the magnitudes of up and low current of the charge pump (CP) results in reference spur in the LO signal, which severely degrades the performance of wireless transceiver. In the proposed CP shown in Fig. 7, the voltage of the node REF is kept equal to the voltage of OUT node of charge pump, and the voltage of the node A(B) is equal to that of the node C(D), which ensure equal up and down current. The feedback amplifier OP2 ensures the constant potential at the nodes,

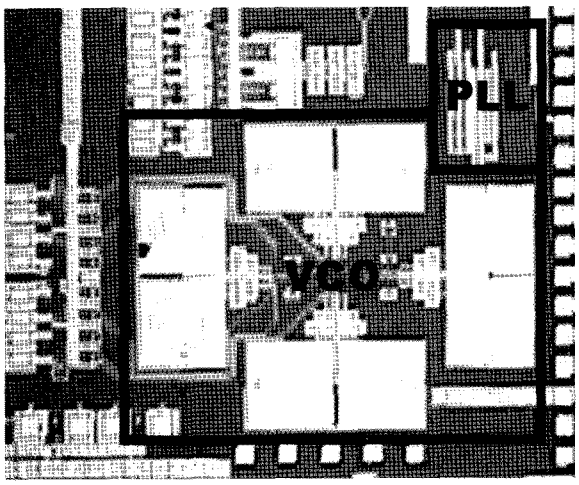


Fig. 8. Die photograph of synthesizer.

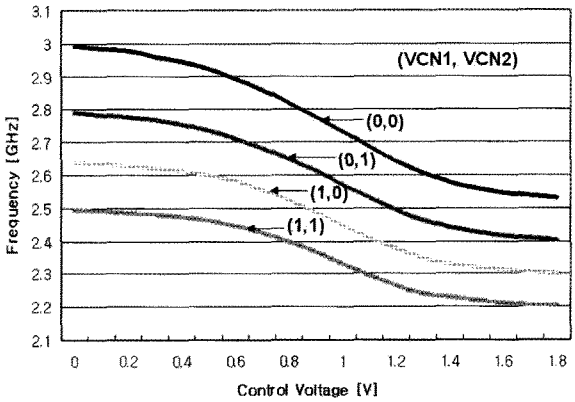


Fig. 9. Frequency tuning characteristic of the VCO.

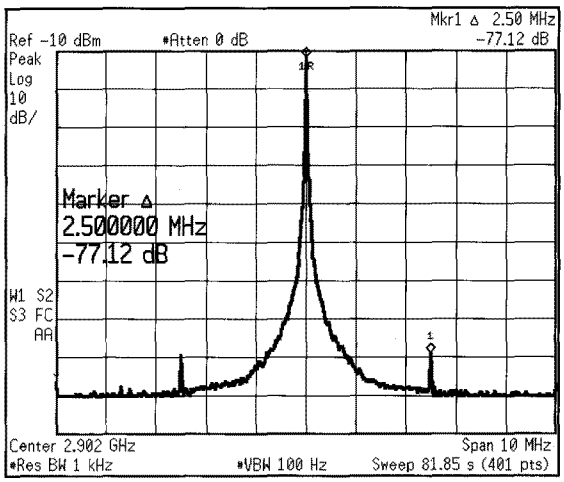


Fig. 10. Output spectrum of 2.5MHz reference clock.

A and B during the switching transients and the reference spur is further reduced.

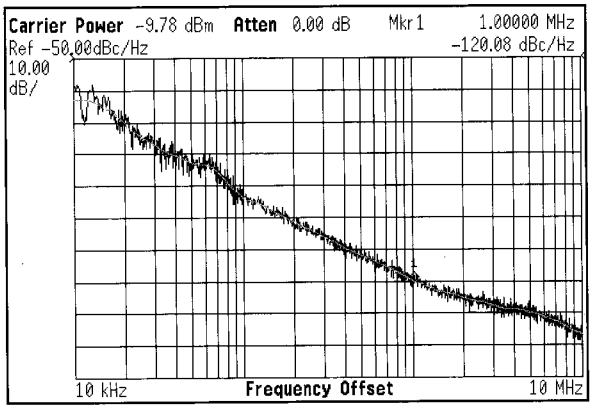
IV. MEASUREMENT RESULTS

The frequency synthesizer has been fabricated in a 0.18μm CMOS technology. Fig. 8 shows the die photograph of the chip which occupies the active area of 1.4 mm × 1.4 mm. The VCO and divider draw 9 and 10 mA from a 1.8-V supply, respectively, and the other blocks draw 3 mA, which amounts to 40 mW total power dissipation. The digital and the analog sections have been separated by n-well guard-ring to avoid the noise coupling through the substrate.

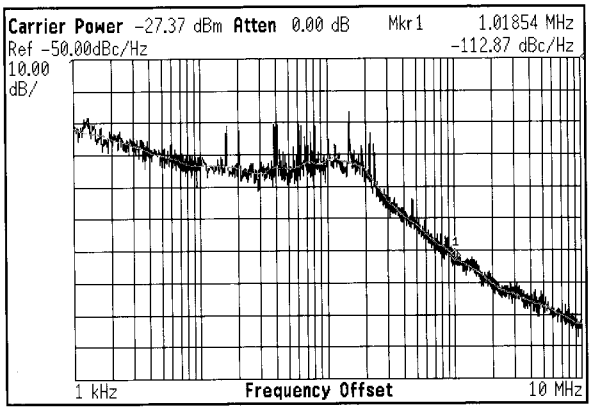
As shown in Fig. 9, the VCO can be tuned between 2.2 GHz and 3 GHz (30% tuning range). The conversion gain of the VCO is about 300 MHz/V. The phase error between octa-phase outputs is smaller than 1.2°. The spectrum of the LO signal is shown in Fig. 10 for upper band where the reference frequency is 2.5 MHz. The carrier power is about -10 dBm and the reference spurs are 70 dB smaller than the carrier power. The measured phase noise of the open-loop and closed-loop VCO output are -120 dBc/Hz and -113 dBc/Hz respectively, at 1 MHz offset from the carrier, as shown in Fig. 11. The higher closed loop phase nose at 1 MHz offset from the carrier is due to the high loop bandwidth. The performance of the proposed synthesizer is compared with previously reported works in Table 1. The proposed synthesizer has better or similar phase noise performance and the chip area while it shows similar power consumption.

V. CONCLUSIONS

A 2.5~3 GHz integer-N frequency synthesizer has been developed for 5~6 GHz UNII-band direct-conversion receiver. Octa-phase local oscillator signals are generated for quadrature down-conversion with sub-harmonic mixing. An integer-N divider consists of multi-modulus prescaler and merged program and swallow counter to solve the complicated timing issues. Phase noise of the VCO is improved by using the ring-type structure with the biasing transistor switched on and off.



(a)



(b)

Fig. 11. Measured phase noise of (a) open-loop VCO at 2.99 GHz and (b) clock-loop VCO at 2.9025 GHz.

Table 1. Comparison of Synthesizer's Performance for 5~6 GHz UNII Band Direct-Conversion Receiver

	VCO Freq. (tuning)	Process [um]	Area [mm2]	Power [mW]	P. N. [dBc/Hz @1MHz]
[16]	3.2~4GHz	0.25	1.7	93	-115
[17]	9.8~11.9GHz	0.18	2.5	39.6	-110
[18]	3.2 ~ 3.9GHz	0.18	> 5	> 40	-108
This work	2.2~3GHz	0.18	2	40	-113

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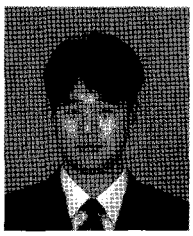

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