

Noise Analysis of Sub Quarter Micrometer AlGaIn/GaN Microwave Power HEMT

Rajesh K. Tyagi*, Anil Ahlawat*, Manoj Pandey**, and Sujata Pandey*

Abstract—An analytical 2-dimensional model to explain the small signal and noise properties of an AlGaIn/GaN modulation doped field effect transistor has been developed. The model is based on the solution of two-dimensional Poisson's equation. The developed model explains the influence of Noise in ohmic region (Johnson noise or Thermal noise) as well as in saturated region (spontaneous generation of dipole layers in the saturated region). Small signal parameters are obtained and are used to calculate the different noise parameters. All the results have been compared with the experimental data and show an excellent agreement and the validity of our model.

Index Terms—AlGaIn/GaN HEMT, polarization, two-dimensional model, drain circuit noise, gate circuit noise

I. INTRODUCTION

Noise in the channel is the internal generation of signals that cause degradation from the desired response. Fluctuations in signal phase, amplitude, and spectral content are forms of noise [1]. The physical properties of materials result in various classes or types of noises. Thermal noise originates because heat in the electrical device provides energy to the carriers causing random fluctuations in their movements. The noise is generated only in systems or circuit elements that dissipate power

(resistive).

A careful examination of the current reveals minute fluctuations, known as noise, which are present whether externally applied signals are present or not. Such fluctuations interfere with weak signals when the transistor is part of an analog circuit. For this reason, the high frequency noise in transistors has received importance. At microwave frequencies, the intrinsic and extrinsic noise sources are generally thermal [2].

The thermal noise within the channel gives rise to both drain channel noise and induced gate noise. As one increases the drain source voltage, the electric field within the channel increases. The increasing electric field causes more carriers to reach velocity saturation. It means there are more carriers present at the time of velocity saturation, therefore amount of diffusion noise near the drain increases. Analytical noise models are available, including the effect of gate inductance and fringing field effect which can predict noise performance based on the scattering parameters at microwave frequencies [3, 4]. It was also shown that as the device width is made to decrease; the noise model will give positive response.

Several theoretical models have been developed to study the noise properties of HEMT. These models could not explain the behavior and effect of noise. Klepser et al., [5] developed an analytical bias dependent noise model for InP HEMT. Their model is based on the two piece linear approximation using charge control and saturation velocity models. Combining large signal model and analytical expressions for the noise source parameter P, R & C an analytical bias dependent noise model was developed. A model for noise parameter of HEMT with resistor temperature noise sources was developed [6]. The model was used to extrapolate the noise parameter in frequency range and described the noise behavior over

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a wide range of bias points. The model was also applied to pseudomorphic structures. Also Hida et al., [7] developed a new low noise AlGaAs/GaAs HEMT which exhibited a 0.95 dB minimum noise figure with a 10.3 dB associated again at 12 GHz and of a 45 GHz cut-off frequency at room temperature. Hsu and Pavlidis [8] developed MODFET noise model and showed its correlation with gate leakage current. A numerical noise model for AlGa_{0.25}N/GaN HEMT was also developed [9]. Noise assessment of AlGa_{0.25}N/GaN HEMT on Si and SiC substrates were done by Jaeger et al., [10]. The HEMT presented very low noise properties with F_{min} and G_{ass} close to 1 dB and 13 dB at 12 GHz. Low frequency and microwave noise characteristics of GaN and GaAs based HEMT are reported in literature [11-17].

In this paper we propose an analytical model that accurately explains the calculations of noise parameters and noise characteristics of 120 nm AlGa_{0.25}N/GaN HEMT. The gate circuit noise and drain circuit noise of AlGa_{0.25}N/GaN HEMT, incorporating the effects of spontaneous and strain-dependent piezoelectric polarization fields have been analyzed. This model is based on the solution of 2-dimensional Poisson's equation. The present model is capable of explaining the influence of noise in ohmic region as well as in saturated region. The effects of important technological parameters such as aluminum concentration, gate length, barrier thickness, and doping of the AlGa_{0.25}N layer on device and noise characteristics have been analyzed in detail. Two dimensional analysis of the device has been carried out in linear as well as in the saturation region. Modified expressions of device transconductance, drain conductance, gate to source and source to drain capacitance has been developed which are used for calculating the important noise parameters. The results of the proposed model have been verified with the published experimental/simulated data and show close agreement.

II. MODEL FORMULATION

Fig. 1 shows a basic AlGa_{0.25}N/GaN HEMT structure. The structure is on a semi-insulating 4H-SiC substrate. The epilayer consists of a 100 nm AlN buffer, 2 μ m undoped GaN, a 5 nm undoped Al_{0.25}Ga_{0.75}N spacer a 10 nm Si-doped Al_{0.25}Ga_{0.75}N charge supply layer and a 10 nm undoped Al_{0.25}Ga_{0.75}N barrier layer. The device has a

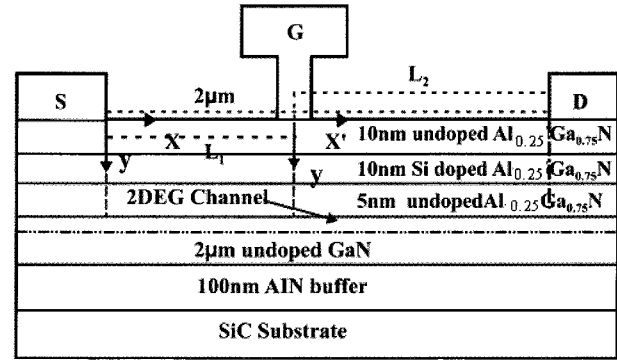


Fig. 1. AlGa_{0.25}N/GaN HEMT structure.

gate length of 120 nm, a gate width of 100 μ m and a source drain spacing of 2 μ m. As shown in the Fig. 1 the region between the gate and the channel is rectangular in shape. It is divided in two regions i.e., the low field region with $0 < x < L_1$ and high field region with $L_1 < x < L$. where L_1 is the length of the linear region (low field region) and L_2 is the length of the saturated region (high field region) and $L (= L_1 + L_2)$ is the total length.

The threshold voltage, including the effects of charge polarization, surface and buffer traps can be expressed as [7],

$$V_{th(m)} = \frac{\Phi_B(m)}{q} - \frac{d \cdot \sigma(m)}{\epsilon(m)} - \frac{\Delta E_c(m)}{q} + \frac{E_{f0}(m)}{q} - \left(\frac{q}{\epsilon(m)} \right) \int_0^d dx \int_0^x N_{si}(x,m) dx - \frac{q \cdot d \cdot N_{st}}{\epsilon(m)} - \frac{q \cdot N_b}{C_b} \quad (1)$$

Where Φ_B is metal-semiconductor Schotky barrier height, q is the electronic charge, σ is overall net (both spontaneous and piezoelectric) polarization charge at the barrier—AlGa_{0.25}N/GaN interface. ΔE_c is the conduction band discontinuity, d is AlGa_{0.25}N layer thickness, $N_{si}(x)$ is Si-doping concentration, E_{f0} is the difference between the intrinsic Fermi level and the conduction band edge of the GaN, ϵ is the dielectric constant of AlGa_{0.25}N, N_{st} is the net-charged surface traps per unit area, N_b effective net-charged buffer traps per unit area and C_b is the effective buffer-to-channel capacitance per unit area. The last two terms in equation (1) describe the effects of the surface traps and buffer traps, respectively.

One-dimensional Poisson's equation is solved in region 1 to obtain the potential in the low field region. With the help of two-dimensional Poisson equation, we obtain the potential in the velocity saturated region (high field). Proper boundary conditions are used to ensure continuity of potential across the interface of the two regions

The drain current (I_{ds}) is calculated from the current density equation

$$I_{ds}(m,x) = W q \mu(x,m) \left(n_s(m,x) \frac{dV_c(x)}{dx} + \frac{K_B T}{q} \frac{dn_s(m,x)}{dx} \right) \quad (2)$$

Where W is the gate width, $n_s(m,x)$ is the sheet carrier concentration, K_B is the Boltzmann constant, T is the absolute temperature and $\mu(m,x)$ is the Al composition (m) dependent mobility. The total drain source current is obtained iteratively by calculating the drain current in the two regions separately and verifying the continuity of potential at the interface of the two regions. The field dependent mobility is given as

$$\mu(x,m) = \frac{\mu_0(m)}{1 + \left\{ \left(\frac{\mu_0(m) E_c - v_{sat}}{E_c v_{sat}} \right) \frac{dV_c(x)}{dx} \right\}} \quad (3)$$

with $\mu_0(m)$ as low field mobility, E_c as the critical field and v_{sat} as the saturation velocity. The sheet carrier density (2DEG) is

$$n_s(m,x) = \frac{\epsilon(m)}{q(d_d + d_i + \Delta d)} (V_{gs} - V_{th} - V_c(x)) \quad (4)$$

Substituting equation (3) and (4) in equation (2) and integrating it using the boundary conditions

$$V_c(x) \Big|_{x=0} = I_{ds}(m,x) R_s \quad (5)$$

$$V_c(x) \Big|_{x=L} = V_{ds} - I_{ds}(m,x) (R_s + R_d) \quad (6)$$

The detailed analysis is given in [14]. It is very important to calculate the interface voltage in reducing potential field, which is very significant for calculating the device transconductance (g_m), and drain conductance (g_d). The following reduced potentials will be defined according to the analysis of Pucel et al. [12].

$$s = \frac{V_{gs} - V_{th}(m)}{V_{th}(m)} \quad (7A)$$

$$w = \frac{V_{gs} - V_{th}(m) - V_{ds}}{V_{th}(m)} \quad (7B)$$

$$p = \frac{V_{gs} - V_{th}(m) - V(x)}{V_{th}(m)} \quad (7C)$$

By using equations (2) to (7), we easily calculate the

value of drain source current.

$$I_{ds} = \frac{G_0}{L_1} \left\{ \left(\frac{(V_{th})^2 (s^2 - p^2)}{2} \right) - \frac{K_B T}{q} V_{L1} \right\} \quad (8)$$

Where V_{th} is threshold voltage, L_1 is linear region length, V_{L1} is the linear region voltage and G_0 is a constant and defined as

$$G_0 = \frac{W \mu_0 \epsilon(m)}{(d_d + d_i + \Delta d)}$$

After solving the current equation I_{ds} , we calculate the voltage (V_{L1}) at L_1 by using boundary conditions at $x = L_1$ $V_c(x) = V_{L1}$ $dV_c(x)/dx = E_c$ then

$$V_{L1} = \left(\frac{-K_B T}{q} + \frac{I_c}{E_c G_0} \right) + \left\{ \left(\frac{-K_B T}{q} + \frac{I_c}{E_c G_0} \right)^2 + (V_{th})^2 (s^2 - p^2) \right\}^{1/2} \quad (9)$$

For calculating the value of L_1 , we find out the current in a saturated region, the saturated current is the product of the number of charge carriers and their velocity, so

$$I_{ds} = \frac{\epsilon(m) V_{th} p W v_s}{d_d + d_i + \Delta d} \quad (10)$$

where v_s is the velocity of the charge carriers also $E_s = v_s / \mu(x)$

Calculating the value of L_1 from equations (7), (8) and (9), we get the following

$$L_1 = \left\{ \left(\frac{(V_{th}) (s^2 - p^2)}{2 p E_s} \right) - \frac{K_B T V_{L1}}{V_{th} p E_s q} \right\} \quad (11)$$

1. Calculation of the Potential in the saturated region

As it is evident from the experiments that in short channel devices the current in the saturation region is not constant but increases with the increase in drain voltage. To describe the characteristics of device in the saturation region accurately we have performed two dimensional analyses in this region. The length of the saturated region L_2 , is determined by both the gate and drain biases.

The potential distribution in the saturation region is obtained by solving two-dimensional Poisson's equation. It is assumed that the region is completely depleted under normal operating conditions and is rectangular in

shape. The analytical solution is obtained by the method developed in [18] and the boundary conditions similar to those of Chang and Fetterman [19]. For the calculation purpose, it is assumed that there is continuity of potential, there is discontinuity of transverse electric field at the interface due to the presence of two dimensional electron gas and the discontinuity of the surface electric field at the gate edges.

The potential distribution in the saturated region is obtained from

$$V(x',y) = \frac{2dE_s}{\pi} \sinh \frac{\pi x'}{2d} \sinh \frac{\pi y}{2d} + V_g + \frac{q}{\epsilon(m)} \left(\int_0^d N_d(y) dy - \frac{I_c}{qWV_{sat}} \right) y - \frac{q}{\epsilon(m)} \int_0^y N_d(y) dy \quad (12)$$

Where $x' = x - L_1$. Substituting $y = d$ in equation 12 we can calculate the potential along the 2DEG channel. Now,

$$V(x')_{x'=L} = V_L = V_d \text{ and } V(x')_{x'=L_1} = V_{L1} \quad (13)$$

So in the saturation region we can write

$$V_L - V_{L1} = \frac{2dE_s}{\pi} \sinh \frac{\pi L_2}{2d} \quad (14)$$

Where V_{L1} is given by equation (9).

The potential drop in the ohmic region channel is given by

$$V_p = - (V(L_1) - V(0)) = V_{th}(s-p) \quad (15)$$

The Potential in the channel by using equation (14) and (15). We get the following equation

$$L_2 = \frac{2d}{\pi} \sinh^{-1} \left(\frac{\pi}{2dE_s} (V_{ds} - V_{th}(s-p)) \right) \quad (16)$$

Now the total length $L = L_1 + L_2$. Substituting the values of L_1 (Linear region length) and L_2 (Saturated region length), we have

$$L = \left\{ \left(\frac{(V_{th})(s^2 - p^2)}{2pE_s} \right) - \frac{K_B T V_{L1}}{V_{th} p E_s q} \right\} + \frac{2d}{\pi} \sinh^{-1} \left(\frac{\pi}{2dE_s} (V_{ds} - V_{th}(s-p)) \right) \quad (17)$$

Equation (17) is used for calculating the small-signal parameters.

2. Calculation of the g_m and g_d

The current voltage characteristics in the saturation region can be obtained by rearranging the terms and replacing I_c by I_{ds} . After obtaining the current voltage characteristics one can easily derive the small signal parameters by differentiating the drain source current with respect to the gate and drain biases.

According to definition of g_m we get,

$$g_m = \frac{dI_d}{dV_g} = \frac{dI_c}{dV_g} = - \frac{\left(\frac{dF}{dV_g} \right)}{\left(\frac{dF}{dI_c} \right)} \quad (18)$$

where

$$F(I_c, V_{ds}, V_g) = L_1 + L_2 - L = 0$$

For converting L into the I_c function we multiply whole equation by I_c/G_0 and calculate g_m

$$g_m = \frac{(s-p) + \frac{2dE_s}{\pi V_{th}} \sinh^{-1} \left\{ \frac{\pi}{2dE_s} (V_{ds} - V_{th}(s-p)) \right\} - \frac{L E_s}{V_{th}}}{\frac{K_B T}{q V_{th}} \left\{ \frac{1}{E_c G_0} + \frac{1}{E_c G_0 (-K_B T/q + I_c/E_c G_0)^2 + (V_{th})^2 (s^2 - p^2)^{1/2}} \right\}} \quad (19)$$

Similarly drain conductance g_d can be obtained as

$$g_d = \frac{dI_c}{dV_{ds}} + \frac{1}{R_p} = - \frac{\left(\frac{dF}{dV_{ds}} \right)}{\left(\frac{dF}{dI_c} \right)} + \frac{1}{R_p} \quad (20)$$

$$g_d = \frac{p + \frac{p V_{th} K_B T}{q} \left[\left(\frac{-K_B T}{q} + \frac{I_c}{E_c G_0} \right)^2 + V_{th}^2 (s^2 - p^2) \right]^{-1/2} - \frac{2dE_s}{\pi V_{th}} \sinh^{-1} \left\{ \frac{\pi}{2dE_s} (V_{ds} - V_{th}(s-p)) \right\} + \frac{2L E_s}{V_{th}} + \frac{1}{R_p}}{\frac{K_B T}{q V_{th}} \left\{ \frac{1}{E_c G_0} - \frac{1}{E_c G_0 (-K_B T/q + I_c/E_c G_0)^2 + (V_{th})^2 (s^2 - p^2)^{1/2}} \right\}} \quad (21)$$

The unity gain cut off frequency f_T is an important figure of merit in determining the microwave application of the device. It is given by the ratio of the transconductance and the device capacitances. For simplicity, we have taken the capacitance to be a constant quantity. The intrinsic frequency f_T is given as

$$F_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (22)$$

C_{gs} and C_{gd} are calculated elsewhere [20].

III. NOISE ANALYSIS OF AN ALGAN/GAN BASED HEMT

The noise analysis is confined with the drain-circuit noise and gate circuit noise.

1. Drain Circuit Noise in an AlGaIn/GaN HEMT

Johnson noise at the interface of the saturated region assuming that our circuit is open circuit Johnson noise analysis is confined with the linear region and saturated region. According to Pucel, Haus and Statz [21] analysis, the channel is divided into two regions, a low field and a high field region. The drain circuit noise is caused by two phenomena firstly by thermal fluctuation and secondly by carriers traveling at their saturated velocity, which is interpreted as diffusion noise. These two effects are uncorrelated because they are produced by different mechanism.

The mean square noise voltage on the drain is given by

$$|\overline{v_{d1}^2}| = 4KT_0 \Delta f \frac{V_{th}}{I_d} \cosh^2\left(\frac{\pi L_2}{2d}\right) (P_0 + P_\delta) \quad (23)$$

where

$$P_0 = (f)^{-1} \left\{ (p^2 - s^2) - \frac{4}{3}(p^3 - s^3) + \frac{1}{2}(p^4 - s^4) \right\} \quad (24)$$

$$P_\delta = \frac{\delta}{p} \ln\left(\frac{p}{s}\right) \quad (25)$$

The parameter δ is a noise temperature-electric field curve-fitting factor. V_{th} , I_d and L_2 are obtained from equation (1), (8) and (16) respectively.

The noise current flowing may then be obtained by simple circuit analysis and is given by

$$|\overline{I_g^2}| = \frac{|\overline{v_{d1}^2}|}{r_d^2} \quad (26)$$

$$|\overline{I_g^2}| = 4KT_0 \Delta f \frac{V_{th}}{I_d r_d^2} \cosh^2\left(\frac{\pi L_2}{2d}\right) (P_0 + P_\delta) \quad (27)$$

r_d is the drain resistance and is obtained by taking reciprocal of g_d [eq. (21)]

The noise voltage is proportional to bandwidth Δf . The $KT_0 \Delta f$ term of equation further indicates the thermal properties of this noise. An empirical curve-fitting factor δ in the P_δ term indicates that the effective noise temperature of the carriers is higher than that of the crystal in the presence of an applied field. The term P_0 represents the Johnson fluctuations in the drain current.

The expression for the diffusion noise is given as [12].

$$|\overline{v_{d2}^2}| = I_{ds} \frac{64 (d)^2 q D \Delta f}{\pi^2 v_s^2 \epsilon(m)^2 b_p^2 W^2} \sinh^2\left(\frac{\pi b_p}{2a}\right) \left\{ \exp\left(\frac{\pi L_2}{2d}\right) - 4 \exp\left(\frac{\pi L_2}{2d}\right) + 3 + \frac{\pi L_2}{d} \right\} \quad (28)$$

Where b_p is the thickness of the conducting layer, B is bandwidth, W is the width of the channel and D is the high field diffusion constant. The other terms are already defined.

2. Gate Circuit Noise in an AlGaIn/GaN based HEMT

The gate circuit noise is caused by fluctuations in the active channel. These fluctuations are capacitively coupled to the gate electrode and cause the channel current to be modulated, which then appears as noise at the output of the device.

The induced gate noise is

$$|\overline{I_{d2}^2}| = \omega^2 \Delta (R_0 + R_\delta) \quad (29)$$

$$R_0 = \frac{(p^3 - s^3)}{3p^2} [\kappa^2 + \gamma^2 p^2 - 2\kappa' \gamma p] + \frac{(p^4 - s^4)}{2p^2} [\gamma^2 p - \kappa' \gamma] + \frac{(p^5 - s^5)}{5p^2} \gamma^2 \quad (30)$$

$$R_\delta = \delta p \ln \frac{p}{s} [\kappa^2 + \gamma^2 p^2 - 2\kappa' \gamma p] + 2p(p-s) [\gamma^2 p - \kappa' \gamma] + \frac{(p^2 - s^2)}{2} p \gamma^2 \quad (31)$$

$$\Delta = 4KT_0 \Delta f \frac{V_{th}}{I_d r_d^2} \cosh^2\left(\frac{\pi L_2}{2d}\right) B \quad (32)$$

$$B = \left(\frac{\epsilon(m) L_1 V_{th}}{d I_{ds}} \right) \quad (33)$$

$$\kappa' = \kappa - \frac{L_2}{L_1} \quad (34)$$

$$\gamma = \frac{W \epsilon(m) \mu(m) r_d p V_{th}}{L_1 (d + \Delta d) \cosh\left(\frac{\pi L_2}{2d}\right)} \quad (35)$$

$$\kappa = \frac{1}{(s^2-p^2)} \left[s^2(p-s) - \frac{(p^3-s^3)}{3} \right] \quad (36)$$

Where R_0 and R_δ refer to the noise produced by normal thermal noise and the hot-electron noise.

3. Noise performance of devices

The correlation coefficient between the gate and drain circuit noise can be calculated as given below. Since they arise from the same fundamental noise mechanism, they are strongly correlated. It is assumed that the correlation coefficient is purely imaginary. The calculation detailed is according to calculation of the Pucel et al. [12].

$$C = \frac{|\overline{i_g i_d}|}{j \sqrt{\overline{i_g^2} \overline{i_d^2}}} = C_1 + C_2 \quad (37)$$

where $i_d^2 = \frac{V_d^2}{r_d^2}$, $C_1 = C_{11} \sqrt{\frac{P_1 \cdot R_1}{P \cdot R}}$ and $C_2 = C_{22} \sqrt{\frac{P_2 \cdot R_2}{P \cdot R}}$. C_{11} is the gate-drain noise current correlation coefficient in the ohmic region, C_{22} is the gate-drain noise current correlation coefficient in the saturation region. To facilitate the evaluation of noise performance of devices, dimensionless noise coefficients are used [14]:

$$P = \frac{\overline{V_d^2}}{4 \cdot K \cdot T \cdot \Delta f \cdot g_m \cdot r_d^2} = P_1 + P_2 \quad (38)$$

$$R = \frac{\overline{i_g^2}}{4 \cdot K \cdot T \cdot \Delta f \cdot \omega^2 \cdot C_{gs}^2} = R_1 + R_2 \quad (39)$$

where K is the Boltzmann constant, T is the operating temperature and Δf is the frequency range. g_m , r_d , and C_{gs} are the small-signal parameters of device, transconductance, drain resistance and gate capacitance, respectively.

$\overline{V_d^2}$ is the equivalent noise voltage at the drain region and $\overline{i_g^2}$ is the equivalent noise induced gate current. P_1 , P_2 and R_1 , R_2 are of the same as P and R , but with subscript 1 and 2 on different noise sources in the region 1 (ohmic region) and region 2 (saturation region), respectively.

Once all these noise sources and their correlations are determined, the minimum noise figure, F_{min} the noise

conductance, g_n and the minimum noise temperature, T_{min} can be obtained:

$$g_n = g_m \cdot \left(\frac{f}{f_i} \right)^2 \left[P + R - 2 \cdot C \cdot \sqrt{P \cdot R} \right] \quad (40)$$

$$F_{min} = 1 + 2 \cdot g_n \cdot \left\{ R_c + \sqrt{R_c^2 + \frac{r_n}{g_n}} \right\} \quad (41)$$

$$T_{min} = 2 \cdot T \cdot g_n \cdot (R_c + Z_{s,opt}) \quad (42)$$

Where r_n and $Z_{s,opt}$ are the noise resistance and optimized source impedance

$$Z_c = R_c + j X_c = R_s + R_d + R_i - \left(\frac{j}{\omega \cdot C_{gs}} \right) \cdot \left\{ \frac{P \cdot R \cdot (1 - C^2)}{(P + R - 2 \cdot C \cdot \sqrt{P \cdot R})} \right\} \quad (43)$$

Z_c is the correlation impedance, R_s and R_d are the source and drain resistance, R_i is the gate charging resistance. In several cases, the device is not matched for the minimum noise conditions and mismatch effect on the noise figure and noise temperature can be expressed as [15].

$$Z_{s,opt} = R_{s,opt} + j X_{s,opt} = \sqrt{R_c^2 + \frac{r_n}{g_n}} + \left(\frac{j}{\omega \cdot C_{gs}} \right) \cdot \left\{ \frac{P \cdot \sqrt{P \cdot R}}{(P + R - 2 \cdot C \cdot \sqrt{P \cdot R})} \right\} \quad (44)$$

$$F = F_{min} + \frac{g_n}{R_s} \cdot |Z_s - Z_{s,opt}|^2 \quad (45)$$

$$T_n = T_{min} + \frac{T \cdot g_n}{R_s} \cdot |Z_s - Z_{s,opt}|^2 \quad (46)$$

Where $Z_s = R_s + j X_s$ is the input termination or source impedance and $Z_{s,opt}$ is defined as the optimum external source impedance. The above equations show that the mismatch effect is less sensitive for low values of the noise conductance g_n and high value of the unity current gain cut-off frequency f_i .

IV. RESULTS AND DISCUSSION

A two dimensional noise analytical model is developed for a 120 nm gate length AlGaIn/GaN HEMT. The equations developed above are simulated in MATLAB software and compared with the experimental results to prove the validity of the proposed model.

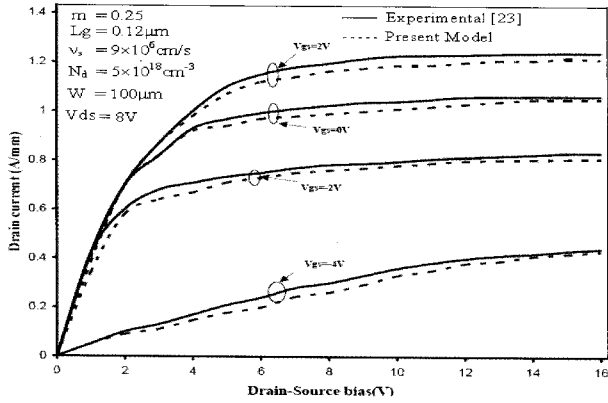


Fig. 2. The variation of the Drain Current with Drain-Source bias.

The current voltage characteristics are shown in above Fig. 2. It can be seen that current increases with the increase in drain source voltage. Complete saturation is not observed due to the inclusion of two-dimensional analyses in the saturation region. The I-V characteristics for different gate voltages are compared with the experimental data [23]. The device exhibited a maximum drain current density of 1.2 A/mm at a gate bias of 2 V and a drain bias of 15 V. This shows that AlGaIn/GaN devices can be effectively used for high power applications. The calculations for drain current have been done for Al mole fraction (m) equal to 0.25. Since we have carried out mole fraction dependent analysis, an increase in mole fraction resulted in an increase in drain current since there is an increase in 2DEG density at the interface.

The variation of cut-off frequency (f_T) with drain current density is shown in Fig. 3. A large variation of cut-off frequency (f_T) was observed with the variation in drain current density. When drain current is low, transconductance is low; hence, we have low value of f_T .

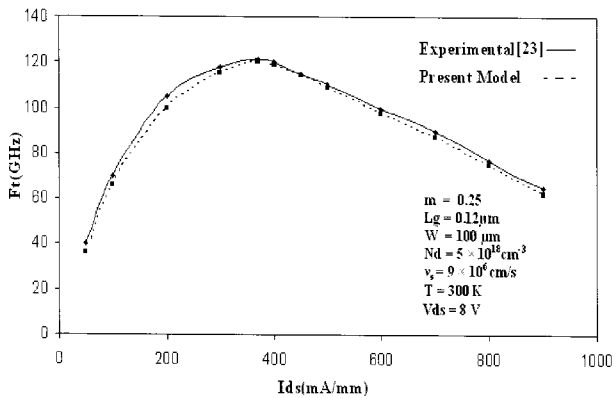


Fig. 3. The variation of cut-off frequency (f_T) with drain current density.

Transconductance increases with the increase in drain current, which result in an increase in cut-off frequency (f_T). After peak g_m a fall in g_m results in a fall in f_T . Thus, a high value of f_T at higher drain currents exhibits the potential of AlGaIn/GaN HEMT for high power at high frequency.

The drain and gate noise coefficients P,R and noise

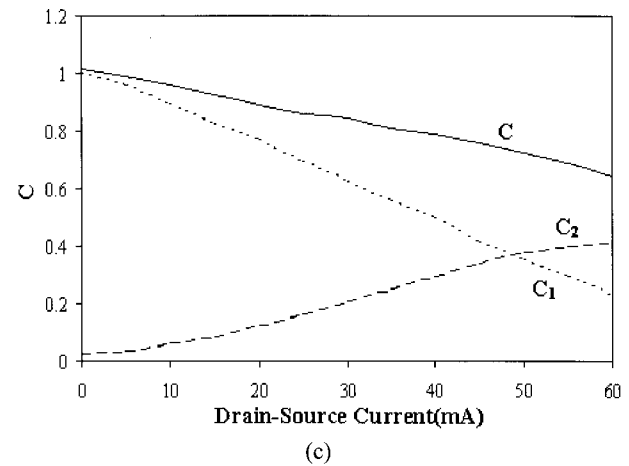
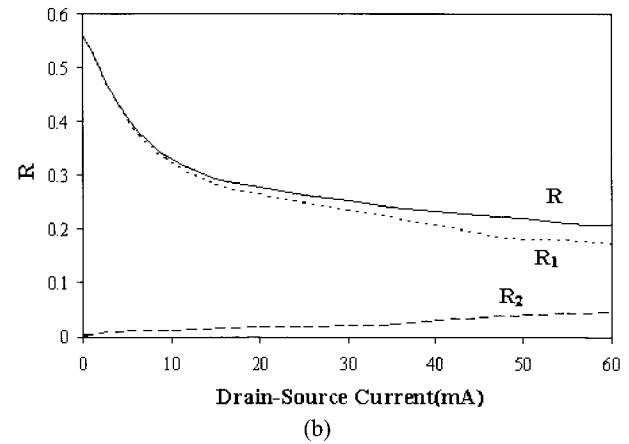
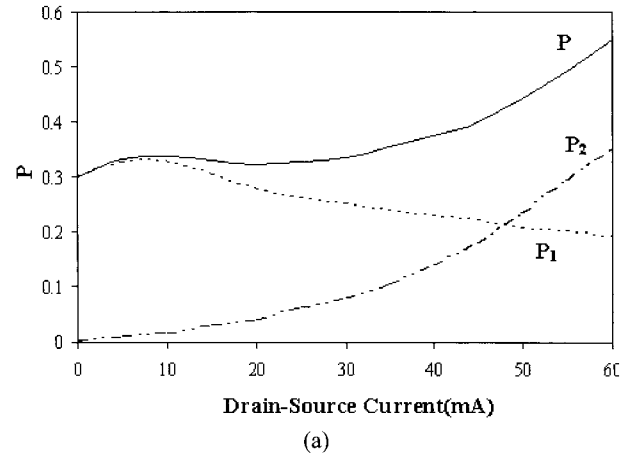


Fig. 4. The variation of Drain noise coefficient (P), Gate noise coefficient (R), and noise correlation coefficient (C) with drain source current plotted in figure (a), (b) and (c) respectively.

correlation coefficient C are plotted as a function of the drain-source current I_{ds} for gate length 120 nanometer and gate width $100 \mu\text{m}^2$ AlGa_N/Ga_N HEMT on SiC substrate in Fig. 4 (a), (b), (c). In Fig. 4 (a), P_1 and P_2 are drain noise coefficients in linear region and saturated region respectively and P is the net resultant of these two. The gate noise coefficient R is larger because of smaller gate capacitance in Fig. 4 (b). The gate noise coefficient R_1 and R_2 are two gate noise coefficients in linear region and saturated region respectively and R is the resultant of the two gate noise coefficients. The correlation coefficient C initially decreases and then again gradually increases with higher current. There is a dip at some intermediate value of drain current where the diffusion noise becomes more dominant than thermal noise in the channel. This dip in C always occurs at a drain-source current, which is higher than that is needed to obtain the minimum noise figure F_{min} as shown in Fig. 4 (c). C_1 and C_2 is the linear and saturated value of the noise correlation coefficient and C is the net total of the C_1 and C_2 .

The variation of minimum noise figure (F_{min}) with drain-current is shown in the Fig. 5. The drain bias was fixed at 10 V and the gate biases were adjusted to control the drain current. The minimum noise figure (F_{min}) depend on gate width, epi-thickness, and doping density. The minimum noise figure decreases with decreasing drain-current. However, similar to gate width, doping density and epithickness affect drain current, gain, and maximum output power. Hence, the minimum noise figure is achieved at the expense of other important device characteristics and these trade-offs must be considered in achieving low noise devices. The minimum noise figure with Drain current shows reasonable agreement with experi-

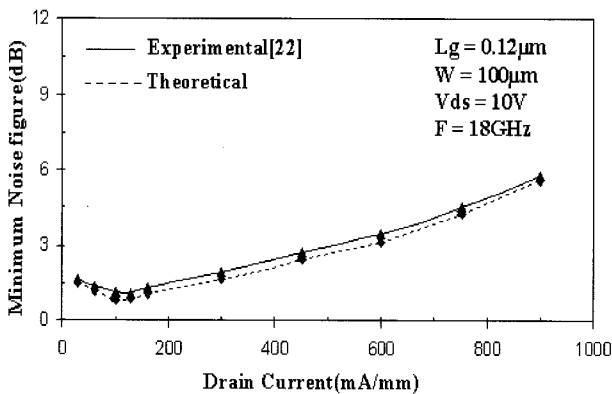


Fig. 5. The variation of Minimum Noise Figure (dB) with Drain-current (mA/mm).

ments and indicates that HEMT noise is dominated by thermal noise with negligible contribution from high field diffusion noise.

In the Fig. 6, the minimum noise figure, F_{min} is plotted with the variations of the Frequency, for an AlGa_N/Ga_N HEMT with gate length $L_g = 120 \text{ nm}$ and gate width $100 \mu\text{m}$, donor layer concentration $N_d = 5 \times 10^{18} \text{ cm}^{-3}$ etc. It is observed that AlGa_N/Ga_N HEMT exhibit better noise performance compared with other AlGaAs/GaAs HEMT model. There is no doubt that AlGa_N/Ga_N have better carrier confinement with respect to AlGaAs/GaAs [15]. At linear region or ohmic region, the current is small due to less potential difference so mobility is very less. As frequency increases the minimum noise figure, become slightly increases.

The variation of noise temperature (K) with drain current is shown in Fig. 7 for gate length 120 nm with mole fraction 0.25. The graph is achieved due to use of 2nd dimensional poisson's equation approach. As observed from figure AlGa_N/Ga_N, have lower noise temperatures. Due to better confinement, saturation velocity enhancement of 2-DEG AlGa_N/Ga_N and small effective channel

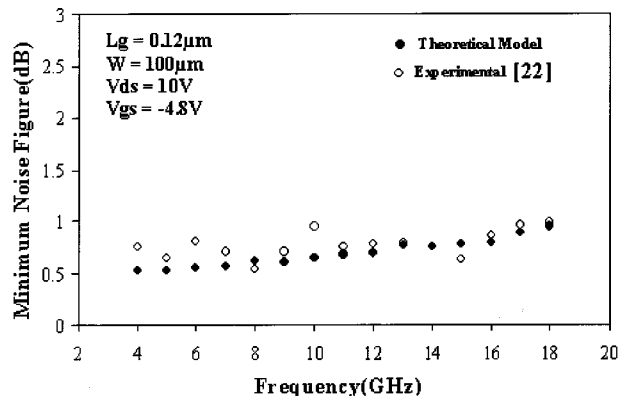


Fig. 6. The variation of Minimum Noise Figure (dB) with Frequency (GHz).

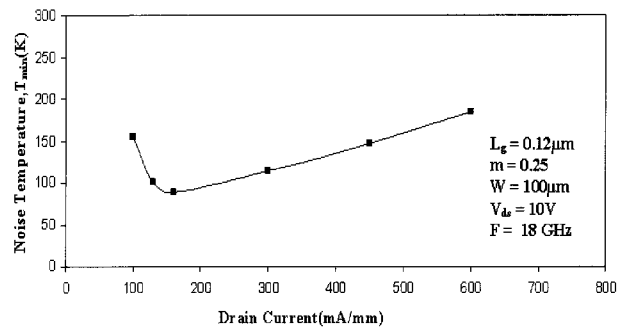


Fig. 7. The variation of Noise temperature (K) with Drain Current (mA/mm).

width. The higher g_m and C_{gs} results in higher cut-off frequency f_t for AlGaIn/GaN hems that results in a lower noise conductance g_n with corresponding lower noise figure and noise temperature.

In Fig. 8 minimum noise temperature varies with the gate length. The trend of the graph shows that at the gate length is decreased the noise temperature also decreases. It is all due to better confinement of 2DEG in AlGaIn/GaN barrier, the effective channel width, high mobility and saturation velocity enhancement. Transit time and total capacitance also decreases as we decrease the gate length so in this way all factors reduce the noise factor.

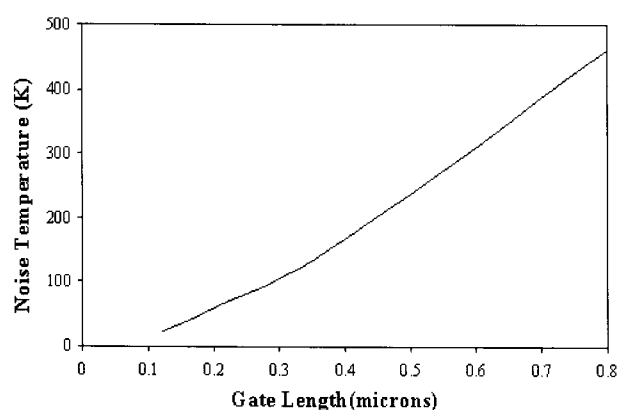


Fig. 8. The variation of Noise temperature (K) with gate length.

V. CONCLUSIONS

In our proposed model, we have analyzed noise performance of AlGaIn/GaN based HEMT. The model is used to analyze the noise performance dependencies on the drain current and frequency. Model shows excellent agreement with the experimental data and the validity of our model. The noise analysis is quite good in linear and saturation region. This noise analytical model completely observed the variation in device characteristics for change in mole fraction (m) and temperature (T). All these excellent performances indicate the low noise and high power applications potentials of AlGaIn/GaN HEMT in microwave frequency ranges. With the combined maturity of nitride-based growth techniques and further optimization of process technologies, it is expected that even better device performance will be obtained in the near future.

REFERENCES

- [1] S. N. Mohammad, A. A. Salvador, and H. Morkoc,

- “Emerging gallium nitride based devices,” *Proc. IEEE*, Vol. 83, pp. 1306-1355, 1995.
- [2] M. N. Yoder, “Gallium nitride: Past, present and future,” in *Int. Electron Devices Meeting Technical Dig.*, pp. 3-12, 1997.
- [3] M. S. Shur, “GaN based transistors for high power applications,” *Solid State Electron.*, Vol. 42, No.12, pp. 2131-2138, 1998.
- [4] U. K. Mishra, Y. F. Wu, B. P. Keller, S. Keller, and S. P. Denbaars, “GaN based microwave power HEMT,” in *Proc. Int. Physics of Semiconductor Devices Workshop*, pp. 878-883, 1998.
- [5] Bernd-Ulrich H. Klepser, Crispino Bergamaschi, and Mathias Schefer, “Analytical Bias Dependent Noise Model for InP HEMT’s,” *IEEE Trans. On Electron devices*, Vol. 42, No. 11, pp. 1882-1889, Nov. 1995.
- [6] T. Felgentreff, G. Olbrich, and P. Russer, “Noise Parameter Modeling of HEMTs with resistor temperature noise sources,” *IEEE MTT-S Digest*, WE3C-3, pp. 853-856, 1994.
- [7] Hikaru Hida, Keichi Ohata, and Yasuyuki Suzuki, “A new Low-Noise AlGaAs/GaAs 2 DEG FET with a surface undoped layer,” *IEEE Trans. On Electron Devices*, Vol. ed-33, No.5, pp. 601-607, May 1986.
- [8] S.S.H. Hsu and D. Pavidis, “Low noise AlGaIn/GaN MODFETs with high breakdown and power characteristics,” *GaAsIC symposium*, pp. 229-232, 2001.
- [9] Lee Sunglae and Webb Kevin J., “Numerical noise model for the AlGaIn/GaN HEMT,” *IEEE MTT-S International Microwave System Digest*, June 6-11, 2004.
- [10] J.C. De Jaeger, S.L. Delage, and Y. Cordier, “Noise Assessment of AlGaIn/GaN HEMTs on Si or SiC Substrates: Application to X-band low Noise Amplifiers,” *13th GAAS Symposium-Paris*, page 229, 2005.
- [11] J. Deng, T. Werner, and M.S. Shur, “Low Frequency and Microwave Noise Characteristics of GaN and GaAs-based HFETs” *GaAs Mantech*, 2001.
- [12] R.A. Pucel, H.A. Haus, and H. Statz, *Advances in electronics and electron physics*. New York: Academic, pp. 195-265, 1975.
- [13] S. Nuttinck, E. Gebara, and M. Harris, “High-frequency noise in AlGaIn/GaN HFETs,” *IEEE microwave and Wireless components letters*, Vol.13, pp. 149-151, 2003.

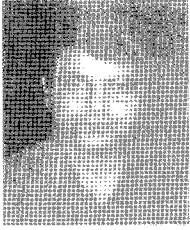
- [14] T.M. Brookes, "The noise properties of high electron mobility transistor," *IEEE Trans. Electron Devices*. Vol. ED-33, pp. 52-57, Jan. 1986.
- [15] A.F.M. Anwar and Kuo-Wei Liu, "A noise model for high electron mobility transistors", *IEEE Trans. Electron Devices*. Vol.41. No.11, pp. 2087-2092, Nov. 1994.
- [16] K.Kamei et al., Extremely low – noise 0.25 μ m gate HEMT, in Proc. 12th GaAs Related compounds conf., pp. 541-546, 1985.
- [17] Y.T. Sullivan, S.G.J. Asbeck, P.M.Waung, C.D.Qiao, and S.S.Lau, Measurement of piezoelectrically induced charge in GaN/AlGaIn heterostructure field effect transistor, *Appl. Phys Lett* (1997); 71(9): 2794-6.
- [18] R.K.Tyagi, A.Ahlawat, M.Pandey, and S.Pandey, An analytical two dimensional model for AlGaIn/GaN HEMT with polarization effects for high power applications, *Microelectronics Journal* 38, pp. 877-883, 2007.
- [19] C.S. Chang and H.R. Fetterman, An analytical model for HEMT using new velocity field dependence, *IEEE Trans. ED* 34, 1456-1462, 1987.
- [20] R. K. Tyagi, Anil Ahlawat, Manoj Pandey, and Sujata Pandey, "A new two-dimensional C–V model for prediction of maximum frequency of oscillation (f_{max}) of deep submicron AlGaIn/GaN HEMT for microwave and millimeter wave applications" *Microelectronics Journal*, Vol.39, Issue12, pp. 1634-1641, December 2008.
- [21] H.Statz,H.A.Haus and R.A.Pucel," Noise characteristics of gallium arsenide field effect transistor," *IEEE Trans. Electron Devices*, Vol. ED-21, pp. 549-562,1974.
- [22] Wu Lu, Jinwei Yang, M.Asif Khan, and Ilesanmi Adesida, AlGaIn/GaN HEMT on SiC with over 100 GHz f_t and Low Microwave Noise, *IEEE Transactions on ED* (2001):48(3) 581-585.
- [23] V.Kumar, W Lu, R.Schwindt, A. Kuliev, G. Simin, J.Yang, M.A.Khan, and H.Adesida, AlGaIn/GaN HEMT in SiC with f_T of over 120GHz, *IEEE Elect. Dev. Lett.* (2002); 23: 455-457.



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