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New Solid-phase Crystallization of Amorphous Silicon by Selective Area Heating

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Abstract

A new crystallization method for amorphous silicon, called selective area heating (SAH), was proposed. The purpose of SAH is to improve the reliability of amorphous silicon films with extremely low thermal budgets to the glass substrate. The crystallization time shortened from that of the conventional solid-phase crystallization method. An isolated thin heater for SAH was fabricated on a quartz substrate with a Pt layer. To investigate the crystalline properties, Raman scattering spectra were used. The crystalline transverse optic phonon peak was at about 519 cm^{-1}, which shows that the films were crystallized. The effect of the crystallization time on the varying thickness of the SiO_2 films was investigated. The crystallization area in the 400nm-thick SiO_2 film was larger than those of the SiO_2 films with other thicknesses after SAH at 16 W for 2 min. The results show that a SiO_2 capping layer acts as storage layer for thermal energy. SAH is thus suggested as a new crystallization method for large-area electronic device applications.

Keywords: Selective area heating, Crystallization, Polycrystalline Si, Capping layer

1. Introduction

Polycrystalline Si (poly-Si) is one of the most important materials for fabricating large-area electronic devices and solar cells. Poly-Si provides higher device reliability, better electrical performance, and a lower defect density than amorphous silicon (a-Si). Many crystallization technologies for poly-Si production have been proposed, including solid-phase crystallization (SPC) [1], rapid thermal annealing (RTA) [2], metal-induced lateral crystallization (MILC) [3], and excimer laser annealing (ELA) [4]. SPC requires a long annealing time, though. RTA has been proposed to reduce the crystallization time, as its temperature is higher than that of SPC, but it has caused problems such as glass bending. MILC has been used to reduce the crystallization time and temperature by employing the catalytic effect of metals such as Ni, but metal contamination occurred on the active layer. One of the most promising crystallization technologies for obtaining high-quality poly-Si is ELA, but it has a high process cost. Thus, these technologies that require high temperature, long annealing time, and high cost are not suitable for large and flexible displays.

To reduce the process temperature, time, and cost, various crystallization technologies for a-Si films with joule-heating-induced crystallization, radio-frequency thermal plasma annealing, and selective area laser annealing had been studied. Hong et al. proposed a crystallization technology for a-Si films that uses Joule-heating [5]. Haruta et al. attempted the rapid crystallization of a-Si utilizing the radio-frequency-inductive coupling thermal plasma torch of argon [6]. Viatella et al. developed selective area crystallization using surface masking of the film during standard laser irradiation [7]. Other groups had presented effective methods for selective laser crystallization to improve electrical performance and carrier mobility. The problem of non-uniformity has remained, however, in the case of large-area AMOLEDs [8]. In this paper, a new crystallization method with a non-laser process that uses selective area heating (SAH) for high-reliability TFTs is suggested. Glass substrates have low thermal damage due to radiant thermal energy. In this study, the energy was limited to a well-defined selective area. The effect of the SiO_2 capping layer with various thicknesses on the crystallization of a-Si by SAH was studied in detail. Processes for mass production

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of large-area displays were proposed.

2. EXPERIMENTAL METHODOLOGY

A 200-nm-thick SiN_x film and a 200-nm-thick a-Si film were deposited successively on a glass substrate using plasma-enhanced chemical vapor deposition (PECVD). The substrate temperature was kept lower than 150°C during the deposition. SiO_2 layers with various thicknesses were deposited on the a-Si films by RF sputtering. Figure 1 (a) shows the experimental setup for the SAH that was provided with a stamp-type thin heater with a micro-controller. The gap between the heater and the sample was about 0.3 mm. The sample was loaded onto a plate in the vacuum chamber, where the SAH was performed via joule heating. Figure 1 (b) shows an emission image of the SAH at 16 W. The surface temperature of the heater was measured with an optical pyrometer. Figure 2 (a) shows the radiant heating in the schematic diagram of the SAH. A Pt thin heater was patterned on a quartz substrate for selective heating of the a-Si film, as shown in Figure 2 (b). A 5,000 Å-thick Pt film was deposited by DC sputtering. Pt proved to be a suitable material for the thin heater due to its resistance to oxidation, its high melting point (1,769°C), and its simple deposition [9]. The area of the thin heater was 2,600 μm x 800 μm, and its thickness was 500 nm. The thin heater had a 20-nm-thick Ta adhesion layer and a 50-nm-thick Ta capping layer for improved reliability. Figure 3 (a) shows the a-Si layer sample. Figure 3 (b) shows the SiO_2 capping layer samples with various thicknesses for the investigation of the effect of the capping layer thickness on the crystallization process. After the crystallization of the a-Si films via thin heater annealing, the properties of the poly-Si were investigated using Raman spectroscopy. The Raman spectra were fitted with a Si wafer. The peak position and full width at half maximum of the Si wafer were 519.891cm^{-1} and 3.17cm^{-1}, respectively. The Raman spectra were measured at room temperature in a confocal geometry using a 514.532nm Ar-ion laser. To avoid laser-induced crystallization, the power of the laser was induced under 0.5mW.

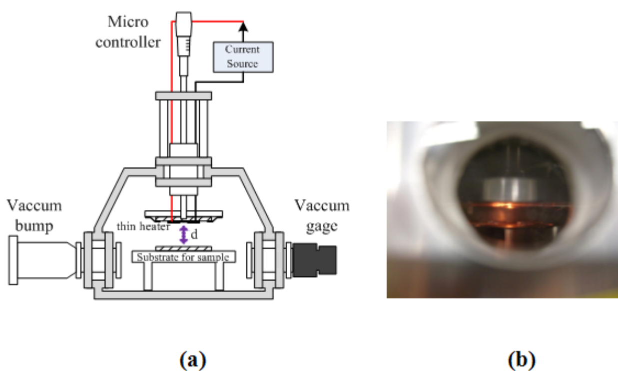


Fig. 1. (a) Experimental setup and (b) emission image of the thin heater.

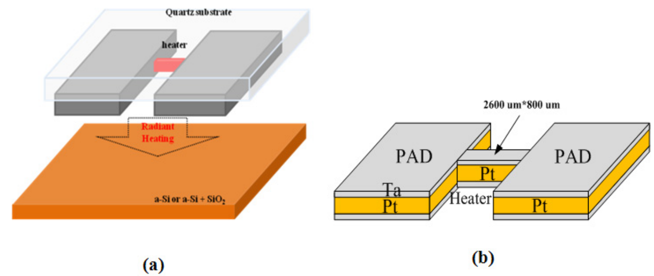


Fig. 2. (a) Schematic diagram of the crystallization process of SAH and (b) structure of the thin heater.

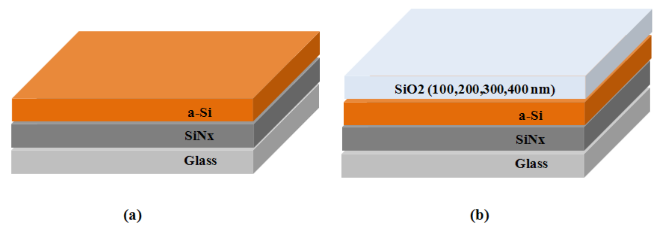


Fig. 3. (a) Si layer sample and (b) SiO_2 capping layer sample with various SiO_2 thicknesses (100-400 nm).

3. RESULTS AND DISCUSSION

Applied power was calculated by applying current and measuring the voltage. The input current was induced from 1A to 1.8 A. The applied power can be described as follows:

$$P = V \times I \tag{1}$$

where P is the applied power, V is the measured voltage, and I is the applied current. The temperature of the thin heater was measured using an optical pyrometer. Figure 4 shows the surface temperature of the thin heater, which was increased in proportion to the applied power. The heater was damaged by electromigration under high current densities. To improve the reliability of the thin heater, the Pt thin heater was provided with an adhesion layer and a capping layer [9]. These layers protected the heater from electromigration and increased its lifetime. Figure 5 (a) shows the photograph of the crystallized Si area in the a-Si layer sample using SAH at 16 W for 4 min. The color of the crystallized area was brighter than that of the a-Si area, and the

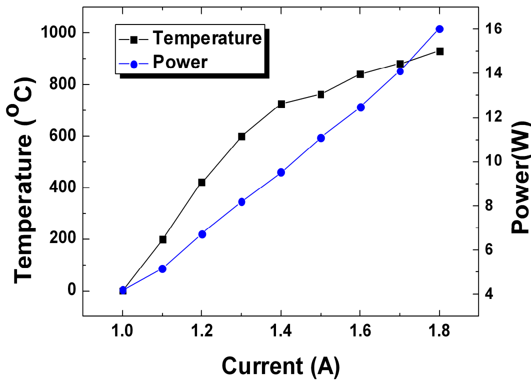


Fig. 4. Relationship between the applied power and the surface temperature of the thin heater.

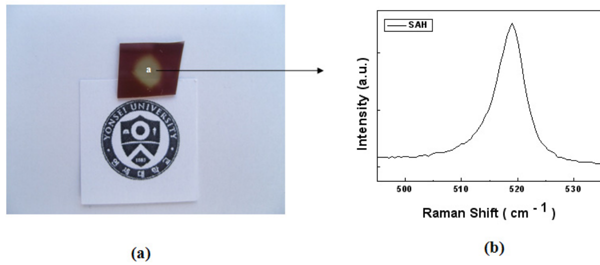
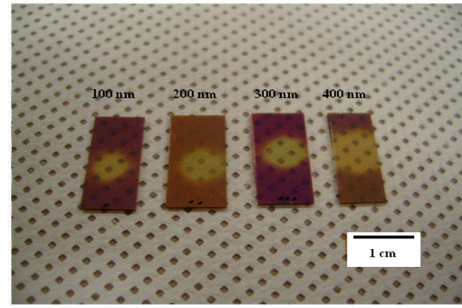


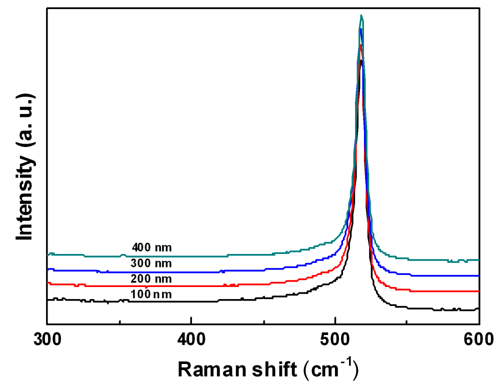
Fig. 5. Photograph of the crystallized Si using (a) the SAH and (b) the Raman spectra of the a-Si.

sharp seemed like a circle due to radiant thermal energy. The crystallinity of the a-Si films was measured by Raman spectroscopy. The crystalline transverse optic (TO) phonon peak of the a-Si films was observed at around 519cm^{-1} at position "a," as shown in Figure 5 (b). It was a poly-Si peak in the SAH-created material [10]. The glass substrate had no damage because the radiant thermal heating was exposed to the well-defined selected area. Figure 6 (a) shows the image of the SiO_2 samples with various thicknesses after SAH at 16 W and 2 min. The Si with the 400-nm-thick SiO_2 capping layer produced a larger crystallized area than the Si with other capping layer thicknesses. The Raman spectra data of the poly-Si with various SiO2 thickness samples show nearly the same poly-Si peaks in Figure 5 (b). As the SiO2 capping layer thickness increased, the diameter of the crystallized Si area also increased, as shown in Figure 5 (c). To study the crystallinity, the crystal volume fraction (X_c) was obtained from the Raman spectra and calculated using the following formula [11]:

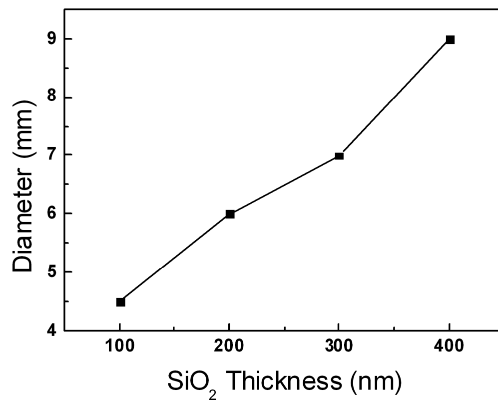
$$X_C = \frac{I_m + I_c}{I_m + I_c + I_a} \quad (2)$$



(a)



(b)



(c)

Fig. 6. (a) Photograph and (b) Raman spectra with micropatterned SiO2 layer after SAH at 16 W for 2 min, respectively. (c) Relationship between the SiO2 layer thicknesses and diameters of the crystallized Si area.

where I_a is an indicator of the amorphous state, I_m is an indicator of the intermediate state, and I_c is an indicator of the crystalline state. According to Equation (2), the crystal volume fractions of the SiO_2 thin films with capping layer thicknesses after the SAH values of 100, 200, 300, and 400nm were 92.6%, 93.4%, 93.8%, and 94.4%, respectively.

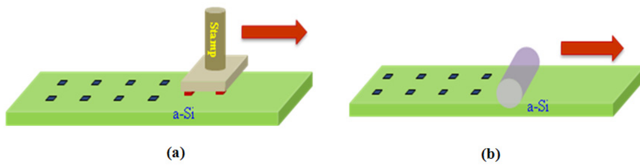


Fig. 7. (a) The proposed stamp and (b) the roll-to-roll process using a new crystallization method with thin heaters.

Figure 5 (b) shows the variations in the crystal volume fraction with increasing capping layer thickness. The volume fraction gradually increased with the increase in the SiO2 capping layer thickness. The volume fraction differences might have been due to an increase in the thermal energy stored in the multilayer structure [12]. Enhanced containment of the thermal energy in the film might have occurred from both the radiant energy and the conductive thermal energy in the capped samples.

Figure 7 shows the proposed processes using a new crystallization method with thin heaters. It can be adopted to crystallize a-Si thin films in the predetermined active area on large substrates effectively and repeatedly. SAH is suggested as a low-cost and promising technology for large-area electronic devices.

4. CONCLUSION

A new crystallization method for highly reliable selective area crystallization was proposed. Because radiant energy was exposed to the well-defined area, the glass substrate had no thermal budget via SAH. The crystallization time was made shorter than that in the conventional SPC method using a stamp-type isolated thin heater and an SiO_2 capping layer. The crystalline TO phonon peak was observed at about 519 cm^{-1}. The crystallinity gradually increased with the increase in the SiO_2 capping layer thickness, which was due to the increase in the thermal energy stored in the SiO_2 capping layer. This new crystallization method is proposed for cost-effective processes such as stamping and roll-to-roll processes.

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