Bidirectional High-Frequency Link Inverter with Deadbeat Control

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ABSTRACT

This paper presents a Bidirectional High-Frequency Link (BHFL) inverter that utilizes the Deadbeat controller. The main features of this topology are the reduced size of the inverter and fewer power switches. On the secondary side of the transformer, the active rectifier employs only two power switches, thus reducing switching losses. Using this configuration, the inverter is capable of carrying a bidirectional power flow. The inverter is controlled by a Deadbeat controller, which consists of the inner current loop, outer voltage loop and a feedforward controller. Additional disturbance decoupling networks are employed to improve the system's robustness towards load variations. A 1-kVA prototype inverter has been constructed and the Deadbeat control algorithm is experimentally verified. The experimental results show that the inverter has high efficiency (91%) with low steady state output voltage total harmonics distortion (1.5%).

Keywords: Inverter, High frequency transformer, Harmonics, Modulation, PWM

1. Introduction

Power inverters are usually found in dc/ac power conversion applications, such as Uninterruptible Power Supplies (UPSs), motor drives and renewable energy source systems. Fig. 1 shows a conventional inverter that converts DC power to ac power using 50Hz transformer isolation. The transformer is needed for applications that require galvanic isolation between the input and output. The H-bridge is switched using the Pulse Width Modulation (PWM) scheme to synthesise sinusoidal output voltage. The higher-order harmonics are filtered by the *LC* low-pass filter to obtain the fundamental (50Hz) voltage. The sinusoidal voltage is then isolated from the

load using the line-frequency (50Hz) transformer. Although this topology has a very simple structure, the line-frequency transformer is very bulky and expensive. Even if the H-bridge is switched at high frequency, the transformer size cannot be reduced because its current is not alternating at high-frequency. An alternative to this topology is the high-frequency link inverter. Compared to the conventional type, the high-frequency link inverter offers a significant reduction in size, weight and cost. This is mainly due to the replacement of the line-frequency
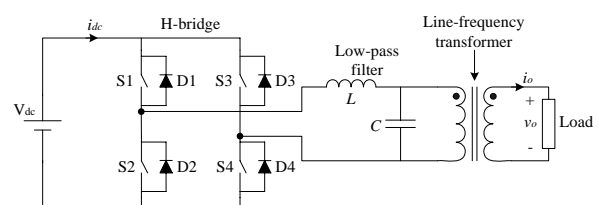
Fig. 1.   Line-frequency transformer-isolated inverter.

transformer with a ferrite-based, high-frequency transformer.

Generally, the high-frequency link inverters can be categorised into two main topologies – high-frequency link inverter with a cycloconverter output stage[1] and high-frequency link inverter with a rectifier output stage[2]. Both topologies are capable of bidirectional power flow, i.e. power can flow from source to load and vice versa. This is mandatory when the load connected to the inverter is inductive.

The high-frequency link inverter with a cycloconverter output stage is shown in Fig. 2. It converts the dc voltage into a high-frequency square wave using an H-bridge. At the secondary side, the sinusoidal output voltage is obtained by "chopping" the high-frequency square wave using the cycloconverter switching method, and subsequently filtering it with a low-pass filter. Fig. 3 shows an example of a cycloconverter switching scheme. However, this topology has several disadvantages. It has high switching losses as all the power switches are operated at high-frequency. Furthermore, it has an inherent problem of voltage surge occurrence, resulting in additional voltage clamp circuit with complex switching scheme[1,3]. A variation of this topology using three
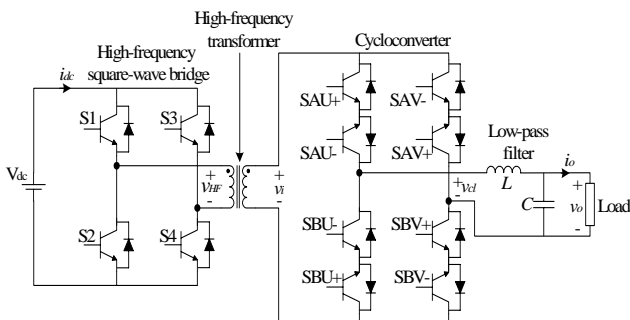
switches on the transformer secondary has been proposed in[4].

The high-frequency link inverter with a rectifier output stage is shown in Fig. 4. At the primary side, the dc voltage is converted into high-frequency ac voltage. At the transformer secondary, the voltage is rectified and unfolded to obtain a sinusoidal PWM waveform. The sinusoidal output voltage is subsequently obtained through a low-pass filter. As the unfolding stage (polarity-reversing bridge) is only operated at line-frequency (50Hz), the switching losses can be reduced. Fig. 5 depicts the waveforms at the main conversion stages.

In this paper, we propose an alternative topology for a bidirectional high frequency link (BHFL) inverter which employs a centre-tapped active rectifier. The main advantage of this topology is the reduced number of power switches that need to be operated at high frequency. This has two important benefits: 1) it lowers the switching
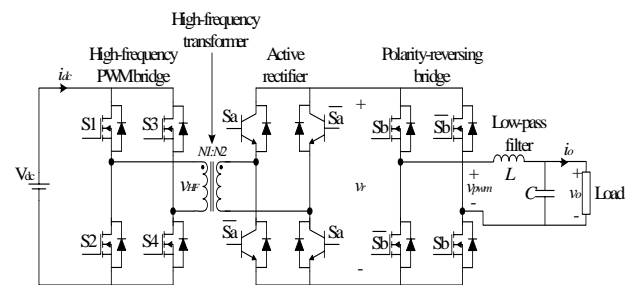

Fig. 4.   High-frequency link inverter with rectifier output stage.

Fig. 2.   High-frequency link inverter with cycloconver.
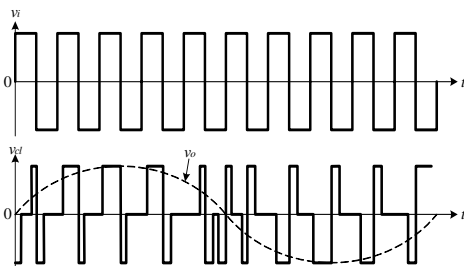
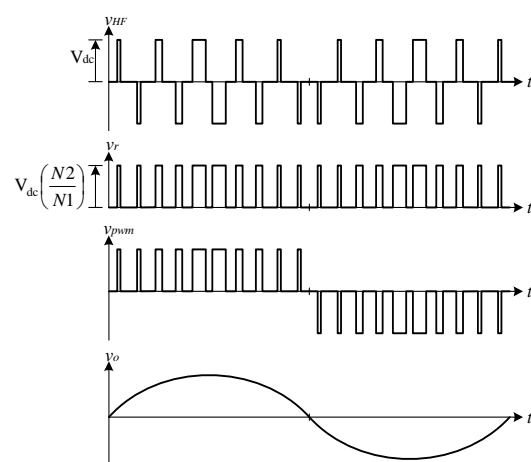Fig. 3.   Cycloconverter switching at the output stage.

Fig. 5.   Timing diagram for high-frequency link inverter with rectifier output stage.

losses and 2) it reduces the component count (reduced number of power switches and gate drivers). The reduced switching losses improve overall inverter efficiency.

In the next sections, the design of the proposed BHFL inverter will be described. This includes the detailed operation of the power circuit and its controller. The BHFL inverter utilises a Deadbeat controller for its closed-loop voltage regulation. The controller incorporates disturbance decoupling networks by taking into account the model discretisation effect. As a result, the system exhibits fast dynamic response towards sudden load changes, and good steady-state response even under nonlinear loads. A 1-kW experimental prototype was built and tested. Typical results on the performance of the inverter, both in steady state and transient conditions will be presented.

2. System Description

2.1 Power Stage

The Bidirectional High-Frequency Link (BHFL) inverter, which is the proposed topology, is shown in Fig. 6[5]. The main conversion circuits are the high-frequency PWM bridge, the active rectifier and the polarity-reversing bridge. First, The dc voltage, V_{dc} is converted into a high-frequency PWM voltage, v_{HF} using the high-frequency PWM bridge. This voltage is isolated and stepped-up using the centre-tapped high-frequency transformer. Then, the voltage is rectified using the active rectifier. The active rectifier, which consists of power switches and anti-parallel diodes, enables a bidirectional power flow. For transfer of power from the dc source to the load, the diodes are utilised. For reverse power flow from the load to the dc source, the power switches ($S3$ and $\overline{S3}$) are turned on. The higher-order harmonics in the rectified PWM voltage, v_{pwm_rect} are then eliminated by the *LC* low-pass filter, and a rectified fundamental component, v_{rect} is obtained. Finally, using the polarity-reversing bridge, the second half of the rectified sinusoidal voltage is unfolded at the zero-crossing, producing sinusoidal output voltage, v_o. The timing diagram for the key waveforms of the power stage is shown in Fig. 7.

The power switches of the BHFL inverter are driven by three gate control signals, namely v_{pwm}, v_s and v_u. The

timing diagram of these control signals is shown in Fig. 8. These control signals will then go through a series of logic gates, as shown in Fig. 9, and become the gating signal for each power switch.

Referring to Fig. 8, v_{pwm} is a rectified SPWM pulse-train, and v_s is a square-wave signal with a frequency that is half of v_{pwm}. The unfolding signal, v_u is a 50Hz square waveform. In Fig. 9, it can be seen that the resulting signals from the logical operations between v_{pwm} and v_s are used to drive the power switches of the high-frequency PWM bridge. Note that v_s is used to alternatively split the rectified SPWM pulses. On the transformer secondary side, v_s is used to drive the power switches of the active rectifier. The power switches of the polarity-reversing bridge are driven by v_u.

Using this configuration, the number of power switches at the active rectifier is reduced, thus the switching losses
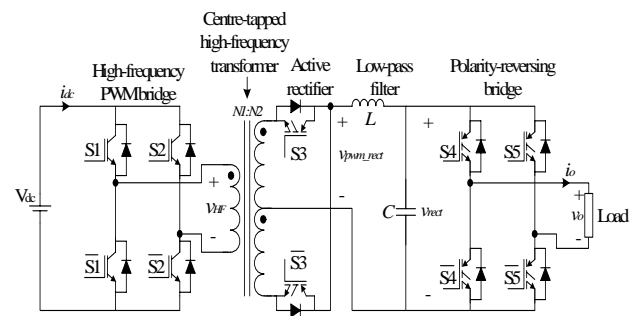

Fig. 6.   The proposed Bidirectional High-Frequency Link (BHFL) inverter.
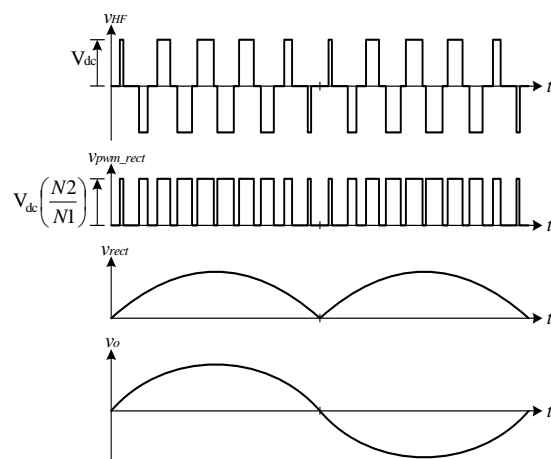

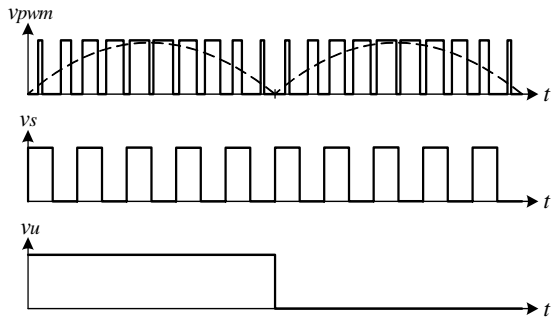Fig. 7.   Key waveforms at the principal conversion stages.

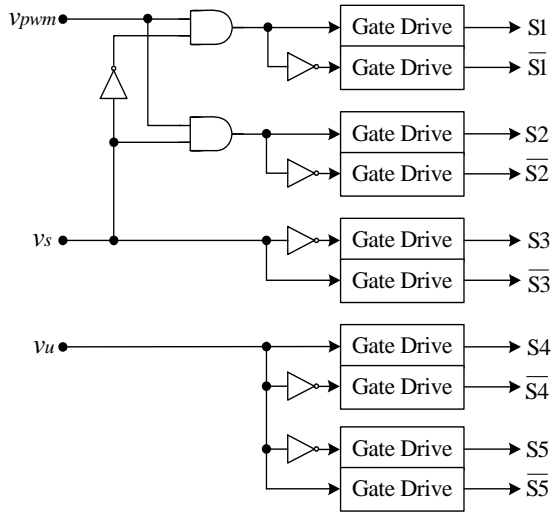Fig. 8.   Gate control signals for the BHFL inverter.

Fig. 9.   Interface between control signals and power switches.

can be reduced. Moreover, the polarity-reversing bridge operates only at line-frequency (50Hz) and is switched during the zero voltage intervals. Hence, the switching losses at this stage are negligible. With that, the overall system efficiency can be increased.

2.1 Controller Design

Inverter performance is normally measured by its ability to produce a high quality sinusoidal output waveform with a good transient response. Besides the well established Proportional Integral (PI) Controller[6], many advanced techniques have been developed to achieve these purposes, for example the zero average current error control[7], the sliding mode control[8] and the Fuzzy Logic Control[9, 10].

The proposed BHFL inverter is controlled by a Deadbeat controller. This control technique has been widely applied in power electronics ever since its introduction by Gokhale *et al.* [11] for PWM inverters.

Deadbeat controllers using a Field-Programmable Gate Array (FPGA) and a Digital Signal Processor (DSP) can be found in[12-13]. In Deadbeat control, any nonzero error vector will be driven to zero at most n sampling periods, where n is the order of the closed-loop system [14]. Therefore, this control technique exhibits a very fast dynamic response.

Deadbeat response is unique to discrete-time control systems. Thus, to design a Deadbeat controller for the BHFL inverter, the discrete-time state-space model of the plant is first derived. The plant is modelled using the state-space averaging technique[14]. Referring to Fig. 6, it is assumed that the dc voltage, V_{dc} is constant. The inverter switching frequency is considered to be high enough when compared to a 50Hz sinusoidal modulating frequency. The high-frequency transformer is assumed to be operating in its linear area. As such, the high-frequency PWM bridge and the transformer can be modelled as constant gains. The polarity-reversing bridge is only operated at line-frequency (50Hz), thus its dynamics can be ignored. With these assumptions, the dynamics of the system can be simplified to a LC low-pass filter connected to the load. Choosing the filter inductor current, i_L and filter capacitor voltage, v_{rect} as state variables, the discrete-time state-space equations of the system can be written as:

$$x(k+1) = Ax(k) + Bu(k) + B_d i_{or}(k) \qquad (1)$$

$$v_{or}(k) = Cx(k) \qquad (2)$$

Where

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} = \begin{bmatrix} \cos(\omega T_s) & -\dfrac{1}{\omega L}\sin(\omega T_s) \\ \dfrac{1}{\omega C}\sin(\omega T_s) & \cos(\omega T_s) \end{bmatrix}$$

$$B = \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \dfrac{1}{\omega L}\sin(\omega T_s) \\ 1-\cos(\omega T_s) \end{bmatrix}$$

$$B_d = \begin{bmatrix} B_{d1} \\ B_{d2} \end{bmatrix} = \begin{bmatrix} 1-\cos(\omega T_s) \\ -\dfrac{1}{\omega C}\sin(\omega T_s) \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

Note that $x(k) = \begin{bmatrix} i_L(k) \\ v_{rect}(k) \end{bmatrix}$ is the state vector,

$\omega = \dfrac{1}{\sqrt{LC}}$ is the cut-off frequency of the low-pass filter in radians per second, and T_s is the sampling period. Based on the discrete-time equations, a digital model of the system can be represented by the block diagram in Fig. 10, where z^{-1} denotes a unit delay.

The Deadbeat controller is designed based on the discrete-time model of the inverter. The controller is shown in Fig. 11. It consists of inner current loop, outer voltage loop, and a feedforward controller. From the discrete-time model of the plant in Fig. 10, it can be seen that there are disturbances terms acting on the inductor current and output voltage. These disturbances are compensated using additional decoupling networks in the following equations:

$$i_d(k) = -\frac{A_{12}}{B_1} v_{or}(k) - \frac{B_{d1}}{B_1} i_{or}(k) \qquad (3)$$

$$v_d(k) = -\frac{B_2}{A_{21}} u(k) - \frac{B_{d2}}{A_{21}} i_{or}(k) \qquad (4)$$

Fig. 12(a) shows the inner current loop controller. The current disturbance decoupling network is added to compensate the disturbances acting on the inductor current. Cancelling the current disturbance coupling allows a simple gain, K_i to be applied in forming the inner current loop. From Fig. 5(a), the current loop control law can be derived:

$$u(k) = K_i \left[i_{ref}(k) - i_L(k) \right] + i_d(k) \qquad (5)$$
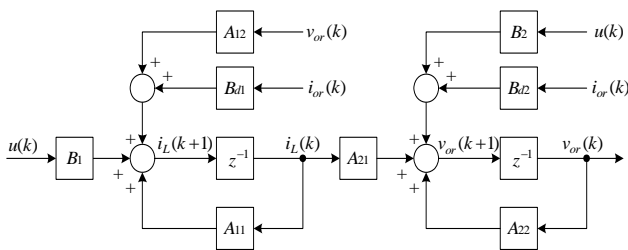
where $u(k)$ is the control signal applied to the PWM

modulator, $i_{ref}(k)$ is the inductor current reference generated by the outer voltage loop, and $i_d(k)$ is the current disturbance decoupling network from (3). The simplified current loop is shown in Fig. 12(b). The discrete-time closed-loop transfer function of the current loop is:

$$C_i(z) = \frac{i_L(k)}{i_{ref}(k)} = \frac{K_i B_1 z^{-1}}{\left[K_i B_1 - A_{11} \right] z^{-1} + 1}$$

$$= \frac{K_i \sin(\omega T_s) z^{-1}}{\left[K_i \sin(\omega T_s) - \omega L \cos(\omega T_s) \right] z^{-1} + \omega L} \qquad (6)$$

From (6), the characteristic equation of the closed-loop current controller can be written as:

$$z - \left[A_{11} - K_i B_1 \right] = 0 \qquad (7)$$

$$z - \left[\cos(\omega T_s) - K_i \frac{1}{\omega L} \sin(\omega T_s) \right] = 0$$

To achieve Deadbeat response, the current loop gain, K_i is designed as:

$$K_i = \frac{A_{11}}{B_1} = \frac{\omega L \cos(\omega T_s)}{\sin(\omega T_s)} \qquad (8)$$

Substituting (8) into (6) yields:

$$i_L(k) = A_{11} z^{-1} i_{ref}(k) = \cos(\omega T_s) z^{-1} i_{ref}(k) \qquad (9)$$

When the value of ωT_s is sufficiently small, $\sin(\omega T_s) \approx \omega T_s$ and $\cos(\omega T_s) \approx 1$. Hence, Eqn. (9) can be written as $i_L(k) = z^{-1} i_{ref}(k)$ which is the Deadbeat response.

Fig. 13(a) shows the outer voltage loop controller. The voltage disturbance decoupling network is added to compensate for the disturbances acting on the output voltage. This improves the robustness of the system towards load variations. Besides, it also acts as an additional current loop command to produce the needed load current without waiting for errors in voltage to occur.
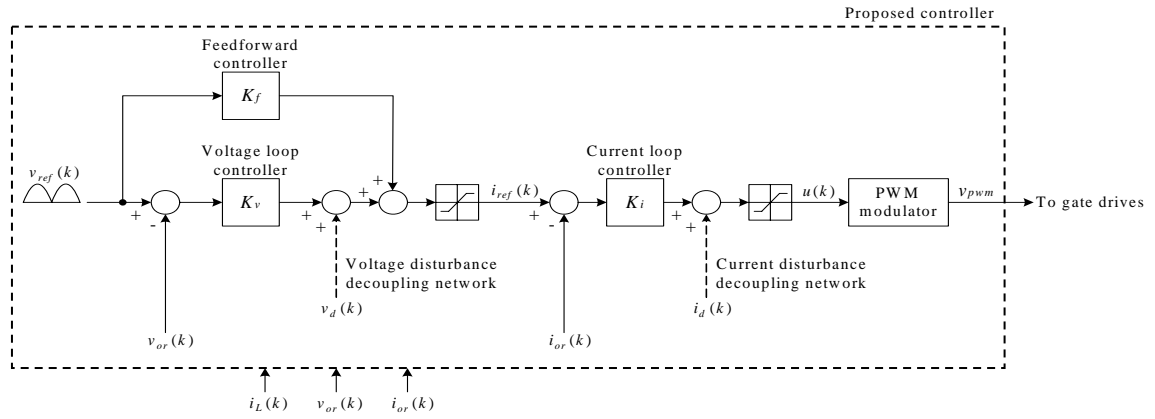

Fig. 10.   Discrete-time model of the BHFL inverter.

Fig. 11.   The proposed controller.
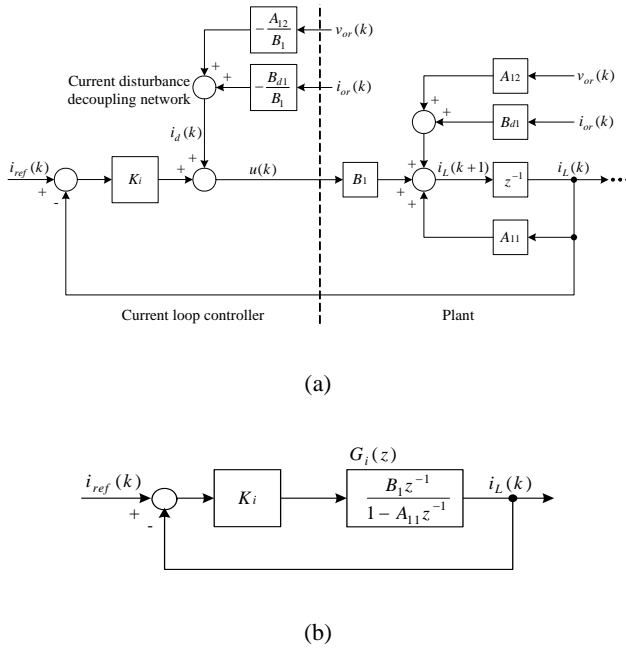

(a)

(b)

Fig. 12.   Current loop controller (a) Exact (b) Simplified.

The design of the voltage loop controller is similar to the current loop controller. The voltage loop gain, K_v is applied to achieve the Deadbeat response. Referring to Fig. 13(a), the voltage loop control law is derived:

$$i_{ref}(k) = K_v \left[v_{ref}(k) - v_{or}(k) \right] + v_d(k) \qquad (10)$$

where $i_{ref}(k)$ is the generated current loop command for the inner current loop, $v_{ref}(k)$ is the rectified

sinusoidal voltage reference and $v_d(k)$ is the voltage disturbance decoupling network from (4). The simplified voltage loop is shown in Fig. 13(b). If the current loop is well designed, the inner current loop is viewed as a constant gain. The discrete-time closed-loop transfer function of the voltage loop is:

$$
\begin{aligned}
C_v(z) &= \frac{v_{or}(k)}{v_{ref}(k)} = \frac{K_v A_{21} z^{-1}}{\left[K_v A_{21} - A_{22} \right] z^{-1} + 1} \\
&= \frac{K_v \sin(\omega T_s) z^{-1}}{\left[K_v \sin(\omega T_s) - \omega C \cos(\omega T_s) \right] z^{-1} + \omega C}
\end{aligned} \qquad (11)
$$

From (11), the characteristic equation of the closed-loop voltage controller can be written as:

$$
\begin{aligned}
& z - \left[A_{22} - K_v A_{21} \right] = 0 \\
& z - \left[\cos(\omega T_s) - K_v \frac{1}{\omega C} \sin(\omega T_s) \right] = 0
\end{aligned} \qquad (12)
$$

Similar to the current loop, the voltage loop gain, K_v is designed to achieve the Deadbeat response:

$$K_v = \frac{A_{22}}{A_{21}} = \frac{\omega C \cos(\omega T_s)}{\sin(\omega T_s)} \qquad (13)$$

Substituting (13) into (11) yields:

$$v_{or}(k) = A_{22} z^{-1} v_{ref}(k) = \cos(\omega T_s) z^{-1} v_{ref}(k) \qquad (14)$$
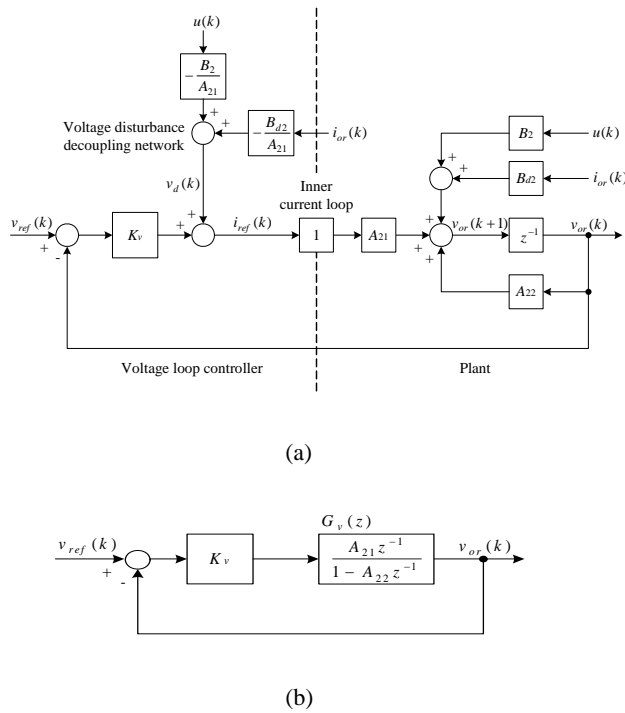
(a)

(b)

Fig. 13.   Voltage loop controller (a) Exact (b)Simplified.

When the value of ωT_s is sufficiently small, (14) can be written as $v_{or}(k) = z^{-1}v_{ref}(k)$ which is the Deadbeat response.

From (14), it can be seen that there is a steady-state error in the output voltage if the value of ωT_s is not sufficiently small. To compensate for the steady-state error, a feedforward controller is added to the output of the voltage loop controller. The feedforward controller imposes a gain scheduling effect on the voltage loop controller according to the reference signal. Fig. 14 shows a voltage loop with the inclusion of a feedforward controller. Referring to Fig. 14, the discrete-time closed-loop transfer function is derived:

$$\frac{v_{or}(k)}{v_{ref}(k)} = \frac{\left[K_v + K_f\right]A_{21}z^{-1}}{\left[K_v A_{21} - A_{22}\right]z^{-1} + 1}$$

$$= \frac{\left[K_v + K_f\right]\sin(\omega T_s)z^{-1}}{\left[K_v \sin(\omega T_s) - \omega C \cos(\omega T_s)\right]z^{-1} + \omega C} \quad (15)$$

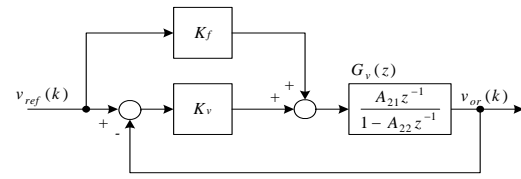To ensure the Deadbeat response, the feedforward gain, K_f is designed as:

Fig. 14.   Voltage loop with feedforward controller.

$$K_f = \frac{1 - A_{22}}{A_{21}} = \frac{\omega C\left[1 - \cos(\omega T_s)\right]}{\sin(\omega T_s)} \quad (16)$$

Substituting (13) and (16) into (15), $v_{or}(k) = z^{-1}v_{ref}(k)$ is obtained which ensures the Deadbeat response.

3. Experimental Results and Discussions

A 1-kVA prototype BHFL inverter has been constructed. The high-frequency PWM bridge is constructed using an APT15GP60BDF1 IGBT. The power transformer is wound on an ETD59 ferrite core. The active rectifier's switches are built using an IRG4PH40K IGBT and a STTA1212D ultrafast high voltage diode, both rated at 1200V. The polarity-reversing bridge is constructed using an IRG4PC40FD IGBT. All the power transistors are driven by a Hewlett-Packard gate-driver chip, HCPL3120. The proposed Deadbeat controller is implemented using a DS1104 DSP from dSPACE (64-bit floating-point processor with TMS320F240 Slave DSP). Hall-effect current sensors, HY10-P and a voltage sensor, LV25-P are used to sense the feedback signals. The parameters of the prototype inverter are provided in Table 1.

Table 1.   Parameters of the prototype inverter.

Parameter	Value
Switching frequency	$f_{sw} = 25$kHz
Nominal input voltage	$V_{dc} = 150$V
Rated output voltage	$v_o = 240$V$_{rms}$
Rated output frequency	$f = 50$Hz
Rated output power	$P_o = 1$kVA
Filter inductor	$L = 0.66$mH
Filter capacitor	$C = 6.8$μF
Sampling period	$T_s = 40$μs

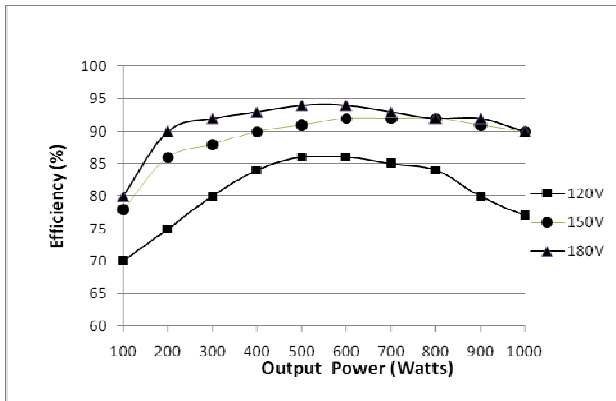Fig. 15 shows the measured efficiency of the inverter

Fig. 15.   Efficiency vs. output power for various input voltages.

with resistive loads at different input voltages and power. The efficiency is measured as a ratio of output power to input power. The input power also includes the auxiliary power supply that is required for the driver, and other electronic circuits (about 15W). It is observed that when the inverter is operated at power in the range of 400-800W, the inverter efficiencies are at their best for all values of input voltages. At low power, the efficiency drops significantly. This is to be expected as power converters tend to have lower efficiencies at a power level that is much lower than its nominal power. At the other extreme, i.e. at the highest power level, the inverter efficiency drops slightly. This can be attributed to the increased switching losses and the ohmic loss in the power transformer at high current operation. It is also noted that the efficiency is lower when the input voltage is lower. The reason for this is that the inverter draws higher current, resulting in higher turn-on losses in the semiconductor switches and in the transformer.

The inverter has been tested under various types of loads including resistive, inductive, phase controlled triac and full-bridge rectifier loads. The parameters of the test loads are summarised in Table 2.

Table 2.   Parameters of the test loads.

Load type	Value
Nominal resistive load	$R = 62.5\Omega$
Inductive load (power factor, $pf = 0.7$)	$R_i = 62.5\Omega$ $L_i = 183\text{mH}$
Nonlinear load (full-bridge rectifier load)	$R_d = 500\Omega$ $C_d = 470\mu\text{F}$

The output voltage and current waveforms under resistive load at about 75% (750W) loading are shown in Fig. 16. The output voltage Total Harmonic Distortion (THD) is 1.5%. The output voltage and current waveforms under inductive load are shown in Fig. 17. It can be seen that the system is capable of carrying a bidirectional power flow. The output voltage THD under this condition is 2.2%. Fig. 18 depicts the THD at different output power levels for resistive and inductive load, respectively. The THD is almost constant for the entire output power range. Fig. 19 shows the output voltage and current waveforms when subjected to a large load disturbance, i.e. form no load to full load. It can be seen that, the voltage dip is recovered quickly after a large step change in the load
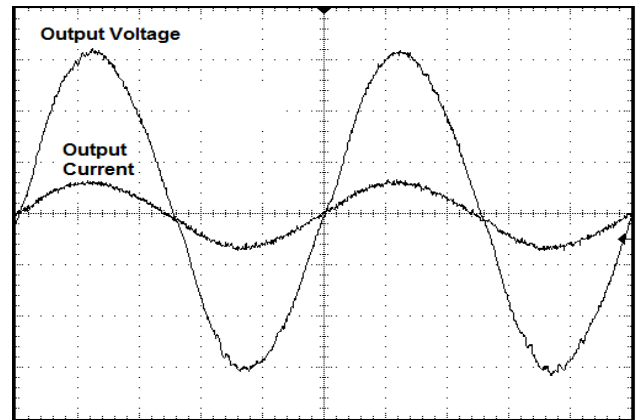

Fig. 16.   Output waveforms under resistive load. Vertical scale: output voltage 100V/div, output current 5A/div, Time scale: 4ms/div
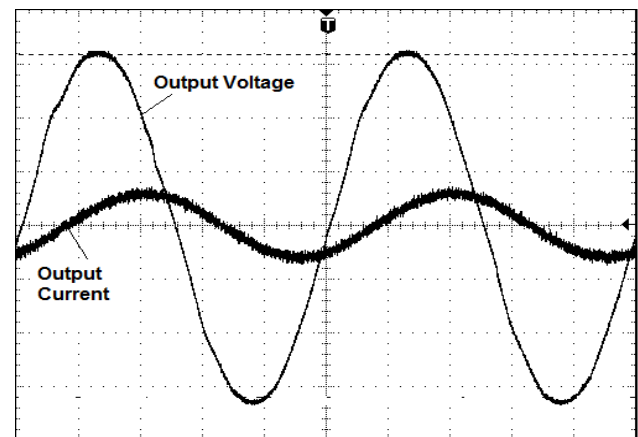

Fig. 17.   Output waveforms under inductive load. Vertical scale: output voltage 100V/div, output current 5A/div, Time scale: 4ms/div.
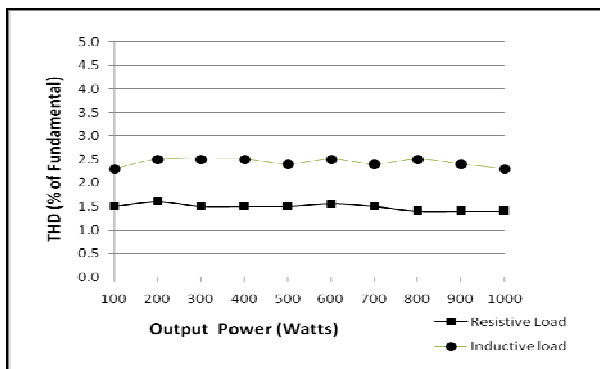
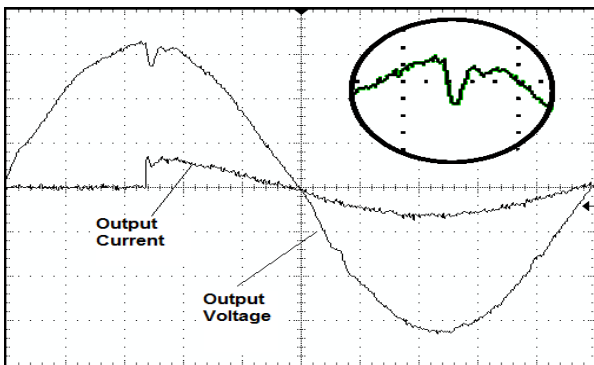Fig. 18.   THD vs output power for resistive and inductive load.

Fig. 19.   Output waveforms under triac load. Vertical scale: output voltage 100V/div, output current 10A/div, Time scale: 2ms/div.

Fig. 20.   Waveforms under full-bridge rectifier load. Vertical scale: output voltage 100V/div, output current 10A/div, Time scale: 4ms/div.

current.   A small overshoot is observed, as depicted by the enlarged section shown on the same plot. The settling time is very short, i.e. well below 5 ms, which can be easily manipulated by an overvoltage protection circuit. The response clearly demonstrates the effectiveness of the Deadbeat controller. To test a worst case loading, the system is connected to a full-bridge rectifier. This type of load is considered to be the most severe type. It causes intense voltage distortion due to its highly distorted current. Fig. 20 shows the steady-state output waveforms under full-bridge rectifier load. As can be seen, the output voltage waveform maintains a reasonably good quality, with a THD of 3.8%. This is still below the normal limit for THD which is 5%.

4. Conclusions

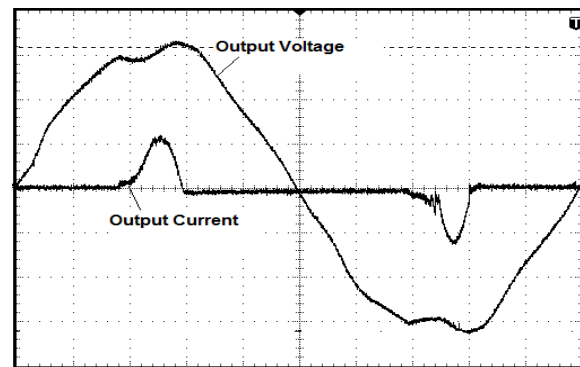A high-frequency link inverter using a Deadbeat controller has been presented. It is a compact, light-weight and low cost solution for dc/ac conversion. Using this topology, the number of power switches is reduced, thus increasing the overall system efficiency. The inverter is also capable of carrying a bidirectional power flow. With a Deadbeat controller, the system is shown to have a fast dynamic response. The voltage transient can be recovered very quickly under step load changes. By adding disturbance decoupling networks which takes into account the model discretisation effect, the system robustness towards load variations is improved. A sinusoidal output voltage waveform with low THD (3.8%) can be obtained even under highly nonlinear rectifier loads. In view of the excellent performances of the inverter, it is thus suitable for wide area of applications, both in stand-alone and grid-connected configurations.

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