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A New Zero Voltage Transition Bridgeless PFC with Reduced Conduction Losses

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ABSTRACT

In this paper a new zero voltage transition PWM bridgeless PFC is introduced. The auxiliary circuit provides soft switching condition for all semiconductor devices. Also, in the resonant path of the auxiliary circuit, only two semiconductor devices exist. Therefore the resonant conduction losses are low. Furthermore, the auxiliary circuit semiconductor elements consist of only one diode and one switch. The proposed auxiliary circuit is applied to a bridgeless PFC converter to further reduce conduction and switching losses. In this paper, the operating modes of this converter are explained and the resulting ideal and simulation waveforms are shown. The presented experimental results justify the theoretical analysis.

Keywords: Boost converter, Bridgeless PFC, Power Factor Correction (PFC), Soft switching, Zero Voltage Transition (ZVT)

1. Introduction

By increasing the use of rectifiers in electrical equipments, undesirable harmonics are injected to the power grid and thus can cause many problems[1]. To reduce the effect of this nonlinear load, some international standards like IEC 61000-3-2 are introduced[2]. Most of the power supplies use conventional rectifier with a large filter capacitor at the end of rectification. This causes excessive peak current, high harmonic distortion and low power factor of about 0.5-0.7. Therefore, the improvement of input power factor has become mandatory[3], [4].

The usual topology employed in power factor correction (PFC) is a rectifier followed by a boost converter as shown in Fig. 1(a)[5]. This conventional PFC converter has three elements in power flow path. To reduce conduction losses, two methods are introduced in the literature. First method is bridgeless PFC as shown in Fig. 1(b) and the other one is single stage PFC (S^2PFC)[6-8]. In higher power applications, S^2PFC is not applied since it will result in extra voltage and current stresses for semiconductor devices and it will require bulky filters. Therefore, bridgeless PFC is a better candidate for high power applications. To reduce the converter weight and volume, high switching frequency is unavoidable[3,4,9]. At high frequencies, MOSFET is the proper choice. Usually zero voltage switching techniques are applied to MOSFET since they can eliminate switching losses as well as capacitive turn on losses[5-8].

Several soft switching bridgeless PFC converters are introduced in literatures[4,13-21]. However, they all suffer from high number of auxiliary elements (especially

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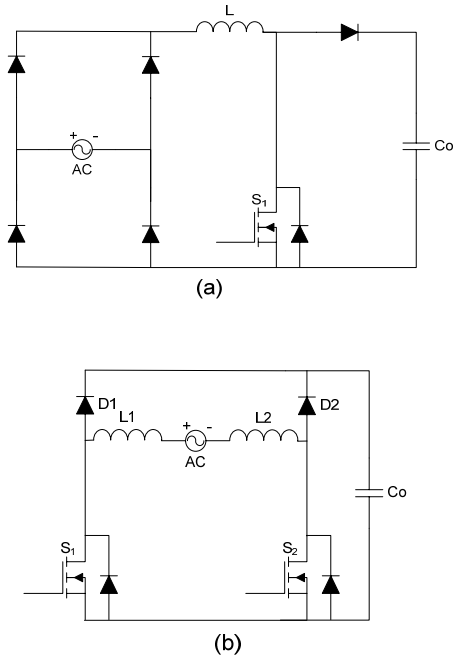


Fig. 1. (a) Conventional PFC converter. (b) Conventional bridgeless PFC.

semiconductor devices) to provide soft switching. Also, in some converters, the auxiliary switch operates under hard switching condition [13-15]. The proposed converter has less number of semiconductor components and the auxiliary switch operates under soft switching conditions. The proposed converter has only five auxiliary elements (one switch, one diode, two capacitors and one inductor). The converters in references [4,16,17] have three semiconductors in the resonant path while the proposed converter has two semiconductors in resonant path. Therefore the conduction losses during the resonant are reduced.

In this paper, a new zero voltage transition (ZVT) PWM Bridgeless PFC is introduced. In the next section, the operation of proposed converter is analyzed. In section III, the design procedure and experimental considerations are explained. The simulation results are presented in section IV and to confirm the theoretical analysis, a prototype of the converter is implemented and the experimental results are shown in section V.

2. Proposed bridgeless PFC circuit operation

The power stage of proposed ZVT-PFC converter is shown in Fig. 2(a). The circuit in doted box is the proposed auxiliary circuit which provides soft switching. The auxiliary circuit is composed of D_3, L_r, C_{r1}, C_{r2} and S_3. The converter operates like a conventional PWM bridgeless PFC except for the switches' turn off and turn on instants. Zero voltage switching (ZVS) at turn off instant is provided by C_{r1} and $C_{r2,}$ while ZVS at turn on instant is prepared by turning on the auxiliary switch for a fixed time.

The converter operation is symmetrical in two cycles of input line. Therefore, the converter operation in one line cycle (positive half line cycle) is explained. To simplify the converter operation analysis, it is assumed that the converter is operating at steady state and all circuit elements are ideal. In addition, the input boost inductance is supposedly large enough to be considered as an ideal dc current source (I_{in}) in a switching cycle. Also, it is assumed that the output capacitance is sufficiently large to be considered an ideal dc voltage source (V_O) as shown in Fig. 2(b).

Based on the above assumptions, circuit operation in a switching cycle can be divided into nine modes as shown by the equivalent circuits in Fig. 3. The theoretical waveforms are illustrated in Fig. 4. Before the first mode, it is assumed that D_1 and the body diode of S_2 are conducting and all other semiconductor devices are off. Also, C_{r2} is charged to V_O and C_{r1} is discharged completely.

➢ Mode 1: [t_0-t_1] (Fig. 4(a))

This mode begins by turning on S_3 and a resonance starts between L_r, C_{r1} and C_{r2}. Therefore, S_3 is turned on under zero current switching (ZCS) condition. The resonant inductor current is:

$$i_{Lr}(t) = \frac{V_O}{Z_1}\sin(\omega_1(t-t_0)) \tag{1}$$

where

$$Z_1 = \sqrt{\frac{L_r}{C_{r1}+C_{r2}}}\,,\ \omega_1 = \frac{1}{\sqrt{L_r(C_{r1}+C_{r2})}} \tag{2}$$

This mode ends when C_{r1} current (I_{Cr1}) reaches the input current (I_{in}). The current through C_{r1} and the duration of this mode is:

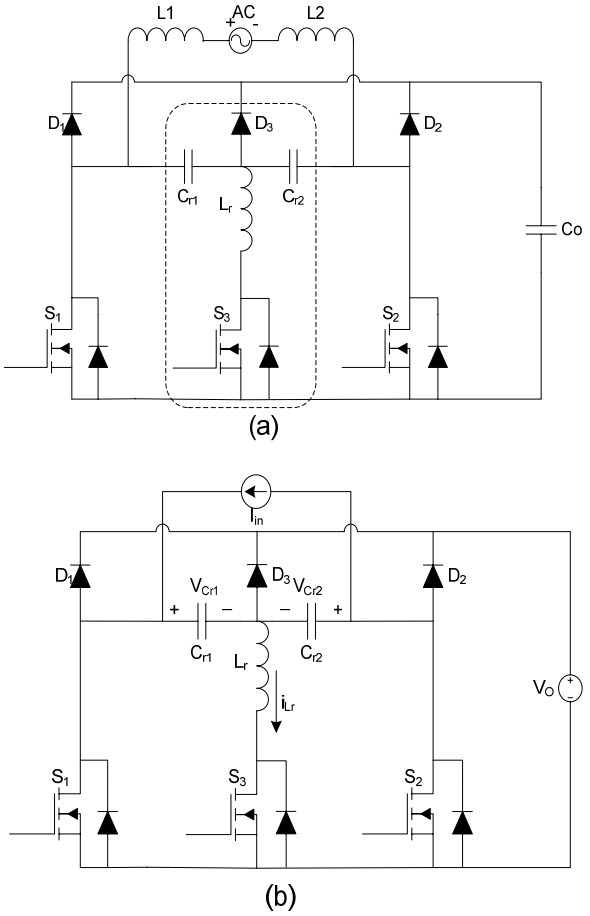


Fig. 2. (a) Proposed ZVT bridgeless PFC converter.
(b) Equivalent circuit of proposed ZVT bridgeless PFC in a switching cycle.

$$i_{C_{r1}}(t_1) = \frac{i_{Lr}(t_1)}{2} = I_{in} \tag{3}$$

$$t_1 - t_0 = \frac{\sin^{-1}\left(\frac{2I_{in}Z_1}{V_O}\right)}{\omega_1} \tag{4}$$

➢ Mode 2: [t_1-t_2] (Fig. 4(b))

In this mode I_{Cr1} is equal to I_{in} and thus, the voltage of C_{r1} increases linearly while the resonance between L_r and C_{r2} continues. The voltages of these two capacitors are as following:

$$V_{C_{r1}}(t) = V_O(1-\cos\omega_1 t_1) + \frac{I_{in}}{C_{r1}}(t-t_1) \tag{5}$$

$$V_{C_{r2}}(t) = -V_O(\cos(\omega_1 t_1))\cos(\omega_2(t-t_1)) \tag{6}$$

where

$$\omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \tag{7}$$

This mode lasts until the voltage of two resonant capacitors become equal. At this time, the voltage across S_1 reaches zero. Therefore, t_2 can be obtained by making (5) equal to (6).

➢ Mode 3: [t_2-t_3] (Fig. 4(c))

In this mode, C_{r1} and C_{r2} are in parallel (C_{eq}=C_{r1}+C_{r2}) and begin to resonant with L_{r1}. S_1 is turned on at ZVS. The resonant current of L_r and the voltage of C_{r1} and C_{r2} are obtained from (8) and (9).

$$i_{Lr}(t) = \frac{V_{C_{r2}}(t_2)}{Z_1}\sin(\omega_1(t-t_2)) - i_{Lr}(t_2)\cos(\omega_1(t-t_2)) \tag{8}$$

$$V_{C_{r1}}(t) = V_{C_{r2}}(t) = V_{C_{r2}}(t_2)\cos(\omega_1(t-t_2)) - i_{Lr}(t_2)Z_1\sin(\omega_1(t-t_2)) \tag{9}$$

This mode continues until S_1 body diode current becomes zero. In other words, this mode ends when i_{Lr} reaches $2I_{in}$. The duration of this mode is calculated by solving the following equation.

$$2I_{in} = \frac{V_{C_{r2}}(t_2)}{Z_1}\sin(\omega_1(t_3-t_2)) - i_{Lr}(t_2)\cos(\omega_1(t_3-t_2)) \tag{10}$$

➢ Mode 4: [t_3-t_4] (Fig. 4(d))

The current through S_1 increases sinusoidally. This mode ends when the S_1 current reaches I_{in} and L_r current reaches zero. Note that V_{Cr1} or V_{Cr2} waveforms still follow equation (9). Duration of this mode is:

$$t_4 - t_3 = \frac{\tan^{-1}\left(\frac{Z_1 i_{Lr}(t_2)}{V_{C_{r2}}(t_2)}\right)}{\omega_1} - (t_3 - t_2) \tag{11}$$

➢ Mode 5: [t_4-t_5] (Fig. 4(e))

At the beginning of this mode, S_3 current is reversed and becomes negative. The current through the body diode of S_3 is divided equally between C_{r1} and C_{r2}. The current

through C_{r1} is an extra current stress on S_1 and the current through C_{r2} reduces the current flowing in S_1 body diode. Due to simultaneous gating of S_1 and S_2, if the current flowing through C_{r2} is larger than I_{in}, then S_2 switch conducts instead of its body diode. During this mode, S_3 is turned off under ZVS. The voltages of C_{r1} and C_{r2} are equal in this mode and are obtained like the previous mode from (9). The duration of this mode is half of the resonance period. The current of L_r can be calculated from (8). This mode ends when L_r current reaches zero.

➢ Mode 6: $[t_5\text{-}t_6]$ (Fig. 4(f))

This mode begins when L_r current reaches zero and the voltage across S_3 rises to V_O-$V_{Cr1,2}(t_5)$.This mode is similar to conventional boost converter and the input inductor is charged. The input current waveform is controlled by the duration of this mode. Voltages of C_{r1} and C_{r2} are equal and constant in this mode and can be obtained by (12).

$$V_{C_{r1}}(t_5) = V_{C_{r2}}(t_5) = V_{C_{r2}}(t_2)\cos(\omega_1(t_5 - t_2)) - i_{Lr}(t_2)Z_1\sin(\omega_1(t_5 - t_2)) \quad (12)$$

➢ Mode 7: $[t_6\text{-}t_7]$ (Fig. 4(g))

By turning off S_1 at the beginning of this mode, S_1 current is forced to flow through C_{r1} and C_{r2}. The voltage of S_1 increases linearly. Therefore, S_1 is turned off under soft switching condition (ZVS). This mode is over when the C_{r2} voltage reaches V_O. The duration of this mode is:

$$t_6 - t_5 = C_{r2}\frac{Vo - V_{C_{r1,2}}(t_4 - t_5)}{I_{in}} \quad (13)$$

➢ Mode 8: $[t_7\text{-}t_8]$ (Fig. 4(h))

Once C_{r2} Voltage reaches V_O at the end of the previous mode, D_3 starts to conduct in this mode. The voltage of C_{r2} is clamped at V_O and C_{r1} discharges. This stage lasts until V_{Cr1} reaches zero. The duration of this mode is:

➢ Mode 9: $[t_8\text{-}t_0]$ (Fig. 4(i))

D_1 turns on at the beginning of this mode and the input inductor energy is transferred to the output. This mode is similar to turn off interval in conventional boost converter.

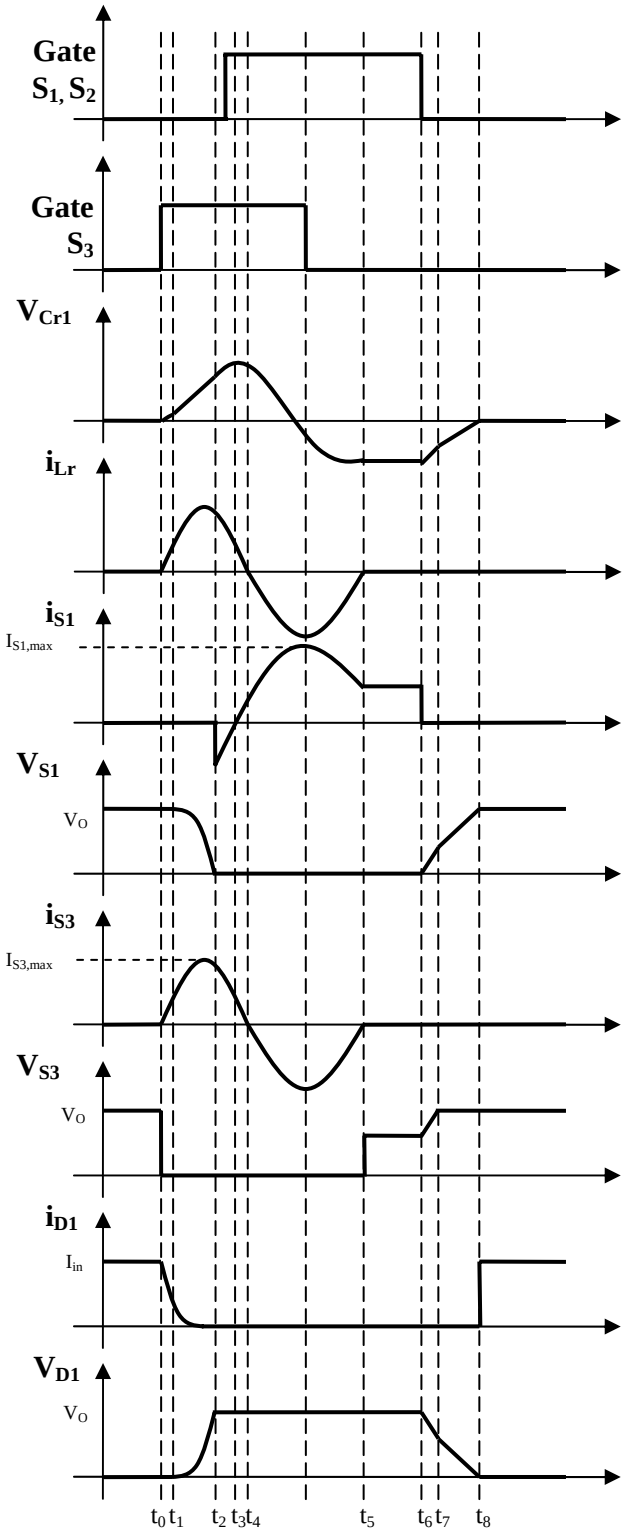


Fig. 3. Theoretical Waveforms of the proposed PFC converter.

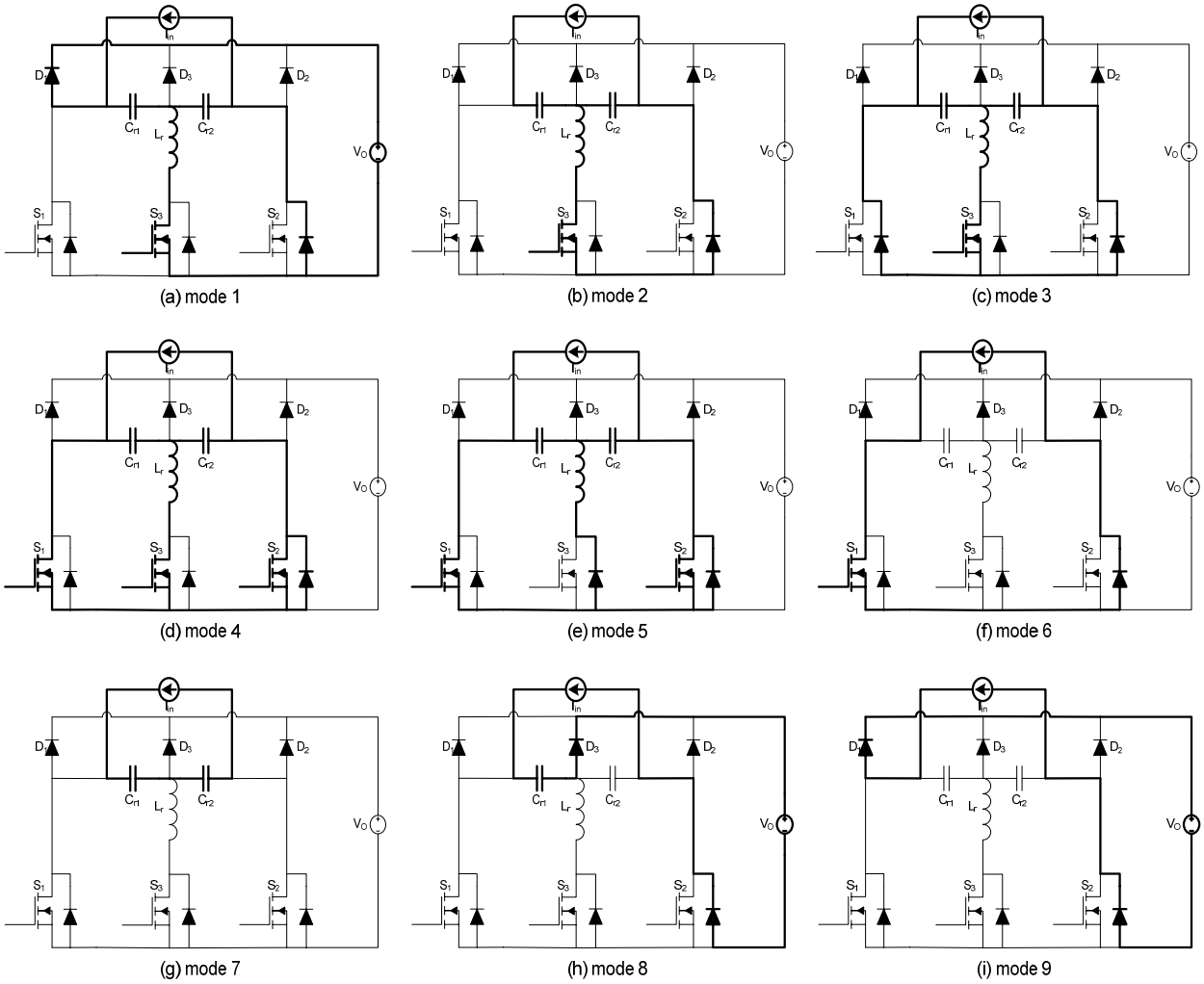


Fig. 4. Equivalent circuit of each mode.

3. Design Considerations

Design considerations of this converter are explained in five sections.

1. The resonant elements (C_{r1}, C_{r2} and L_r):

To provide soft switching, two conditions must be satisfied. First, I_{Cr1} must reach I_{in} in mode 1. Therefore from (1) and (3), the following is established:

$$Z_1 \le \frac{V_O}{2I_{in}} \tag{14}$$

Second condition arises from mode 2. At the end of this mode, the voltage of two capacitors must reach the same voltage to provide zero voltage across S_1. Therefore

$$\begin{aligned} & V_O(1-\cos\omega_1 t_1) + \frac{\pi I_{in}}{\omega_1 C_{r1}} \le V_O(\cos(\omega_1 t_1)) \\ & \Rightarrow \cos(\omega_1 t_1) - \frac{\pi I_{in}}{2V_O\omega_1 C_{r1}} \ge 0.5 \end{aligned} \tag{15}$$

The resonant inductor value is selected based on the output power and the main diode turn off speed [22]. By selecting resonant inductor and the above considerations, the resonant capacitors are chosen.

2. Selection of S_1, S_2 and S_3:

The peak current and the voltage stresses are obtained from the following equations:

$$V_{SW1,2,3\max} = V_{O\max} \tag{16}$$

$$I_{SW1,2\max} = I_{IN\max} + \frac{\Delta I_L}{2} + \frac{1}{2}\sqrt{\left(\frac{V_{C_{r2}}(t_2)}{Z_1}\right)^2 + i_{Lr}(t_2)^2} \quad (17)$$

$$I_{SW3\max} = \sqrt{\left(\frac{V_{C_{r2}}(t_2)}{Z_1}\right)^2 + i_{Lr}(t_2)^2} \quad (18)$$

3. Selection of D_1, D_2 and D_3:

The peak current and voltage stresses are obtained from the following equations:

$$V_{D1,2\max} = V_{O\max} \quad (19)$$

$$I_{D1,2,3\max} = I_{IN\max} + \Delta I_L/2 \quad (20)$$

4. Selection of L_1, L_2 and C_O:

The boost inductance L_1+L_2 and the output filter capacitance C_O are selected to minimize the input current ripple and the output voltage ripple, respectively. The design method of input inductor and output capacitor can be obtained in the same way as in a conventional PWM converter is attained [23].

5. Control circuit:

In general, the control method of this converter can be the same as conventional PWM-PFC. For simplicity, peak current mode control is used in this paper as shown in Fig. 5. The differences between the proposed converter controller and the conventional PWM-PFC controller are in the presence of two monostables, a gate driver and a XOR gate as shown in the doted box in Fig.5. The extra components are required to drive the auxiliary switch. If these four extra elements are added to any control method used for conventional PWM-PFC, then that control system can be used for the proposed PFC and, thus, conventional PFC control ICs can be employed. Based on the converter operation explained in the previous section, the on time of monostable1 is equal to on time of S_3 while the on time of monostable2 is equal to the delay time between turning on signals of S_1 and S_3.

4. Simulation Results

The proposed bridgeless PFC is simulated by PSIM when operating at 300W with V_{AC}=110 V_{rms}, V_O=200 V_{DC} and f_{sw}=70KHz. According to the above design considerations, the circuit elements are obtained as L_r=6μH, C_{r1}=C_{r2}=30nF, L1=L2=300μH, C_O=1000μF.

The simulation results in Fig. 6, show soft switching for semiconductor devices. The ZVS of main switches (S_1, S_2), ZCS of auxiliary switch S_3 and ZVS of main diode (D_1, D_2) are illustrated respectively in Fig. 6(a-c). The input line voltage, line current and input current harmonics are shown in Fig. 7. The input current is practically sinusoidal with low total harmonic distortion (THD) and high power factor (PF). All line current harmonics are below the IEC61000-3-2 requirements [2].

5. Experimental Results

A prototype of simulated PFC converter is implemented to show the validity of theoretical analysis and simulation results. The proposed bridgeless PFC converter is realized by IRFP460 for switches and FES8JT for all diodes. The voltage and current of all semiconductor devices in the proposed PFC converter are shown in Fig. 8. The ZVS of main switches (S_1, S_2), ZCS of auxiliary switch S_3 and ZVS of main diode (D_1, D_2) are shown respectively in Fig. 8(a-c). The zero level of each channel is shown by “1” and “2” on the left side of each figure. In comparison to simulation results, the experimental results exhibit ringing starting at t_5. This is due to the resonance between parasitic inductances, L_r, and junction capacitance of S_3.

The input current and voltage and the efficiency of this converter in different loads are shown in Fig. 9. The waveforms of input voltage and current are almost in phase and the measured power factor is close to unity especially when the input voltage is fully sinusoidal. On average, the efficiency is improved by 2% for different loads.

6. Conclusions

In this paper, a new ZVT PWM bridgeless PFC is introduced and realized. The auxiliary circuit provides soft switching condition for all semiconductor devices. Only one diode and one switch are used in the auxiliary circuit. Since only two semiconductor devices exist in the resonant path of the auxiliary circuit, the conduction losses of resonant path are reduced. The proposed auxiliary circuit is applied to a bridgeless PFC converter in order to further reduce conduction and switching losses. The presented simulation and experimental results of the proposed converter show high efficiency of about 96% and near unity power factor for input current.

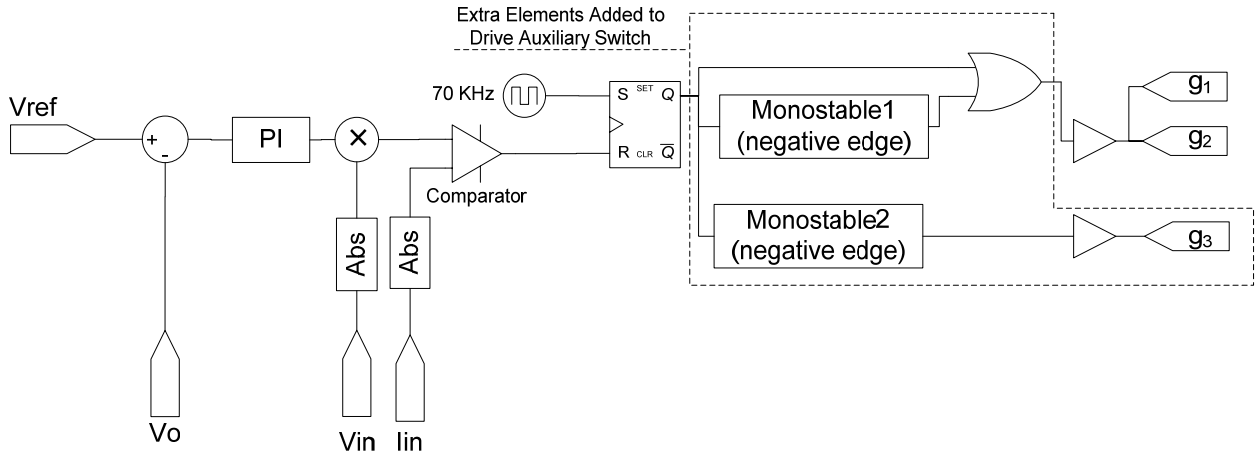
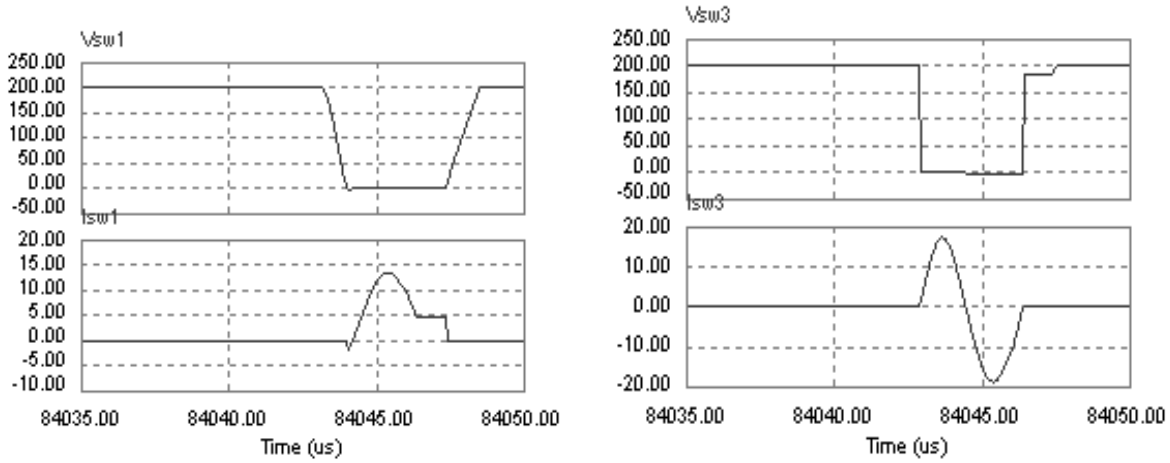
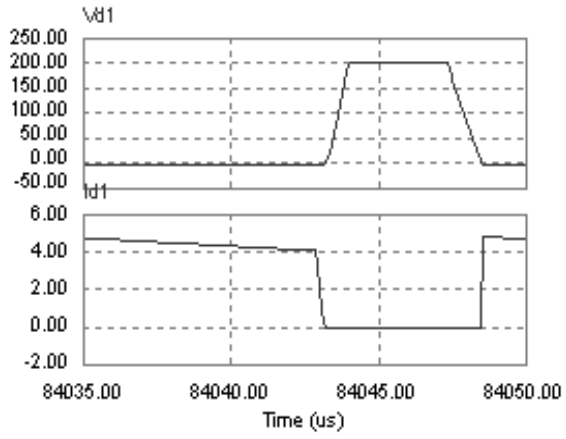


Fig. 5. Control circuit block diagram.

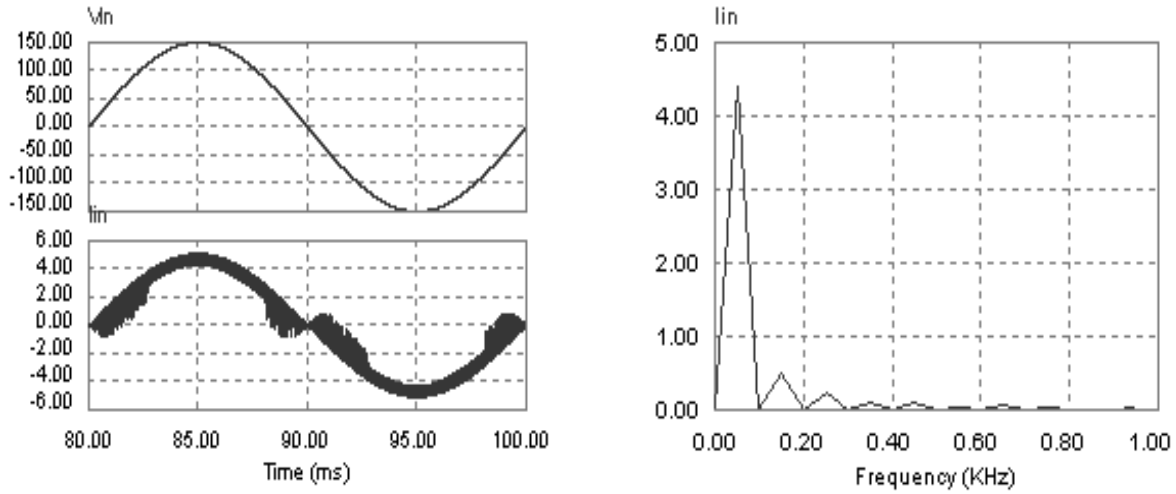


(a) (b)



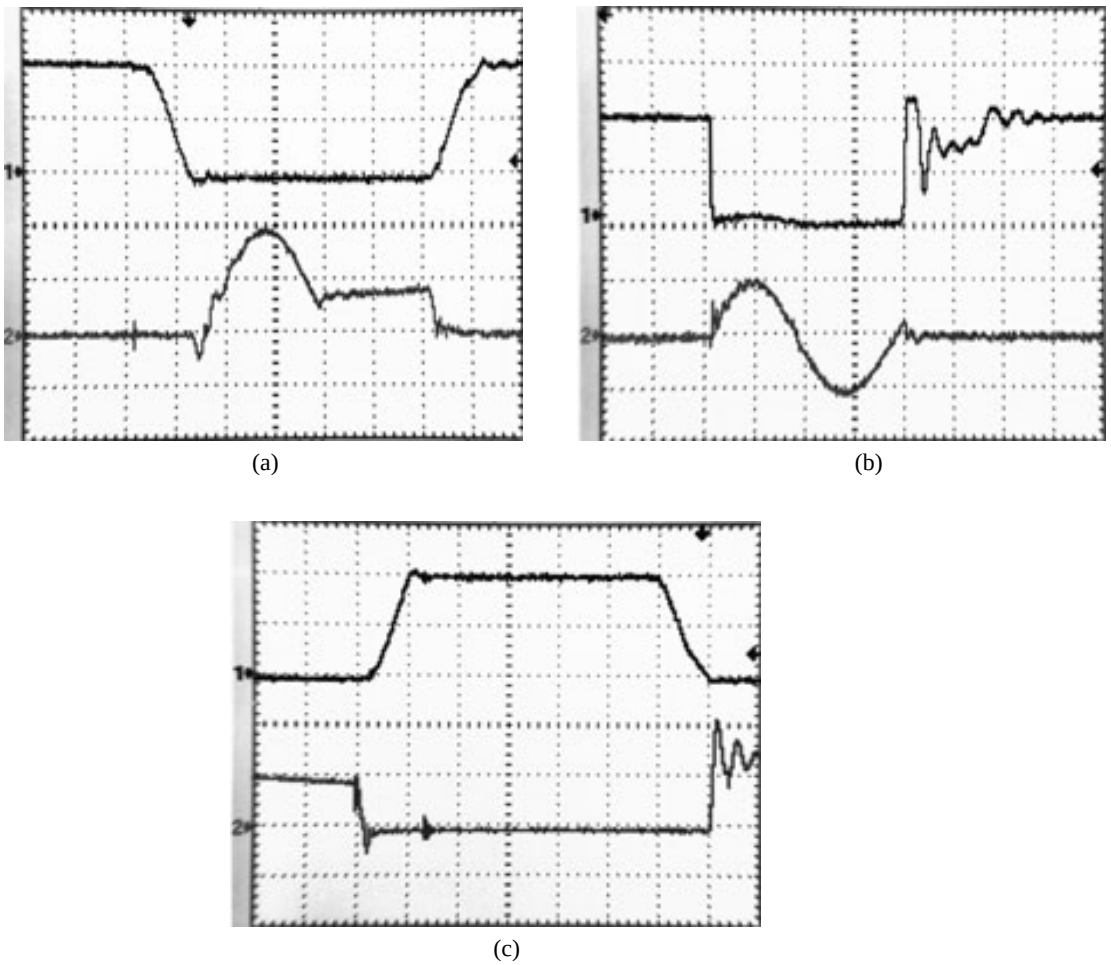
(c)

Fig. 6. Soft switching of (a) main switch, (b) auxiliary switch and (c) main diode(In all figures top waveform is voltage and bottom one is current).



(a) (b)

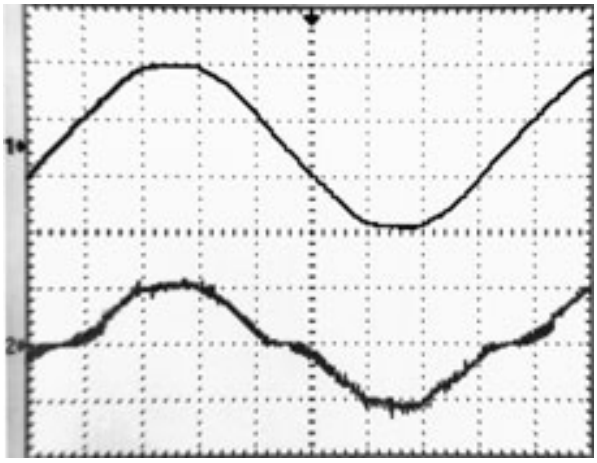
Fig. 7. (a) top: line voltage and bottom: input line current. (b) Input current harmonics.



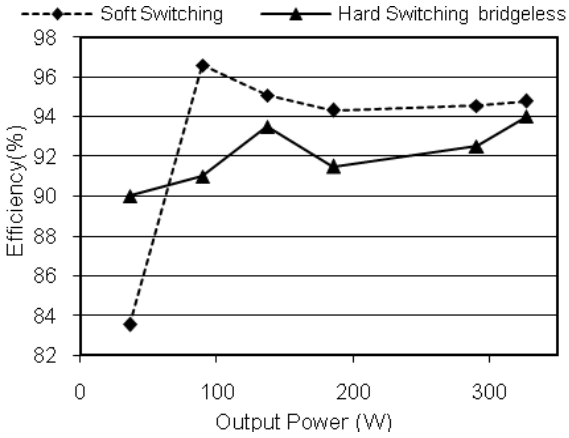
(a) (b)

(c)

Fig. 8. Soft switching of (a) main switch, (b) auxiliary switch and (c) main diode (In all figures the top waveform is voltage (100V/div) and bottom is current (5A/div). Time scale is 1 μs/div).



(a)



(b)

Fig. 9. (a) top: line voltage and bottom: input line current (Voltage scale is 100 V/div and Current scale is 5 A/div). (b) Efficiency comparison of the proposed bridgeless PFC converter with its conventional counterpart.

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