Multi-channel Incremental Data Converters

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ABSTRACT

Incremental converters provide a solution for such measurement applications, as they retain most of the advantages of conventional ΔΣ converters, and yet they are capable of offset-free and accurate conversion. Most of the previous research on incremental converters was for single-channel and dc signal applications, where they can perform extremely accurate data conversion with more than 20-bit resolution. In this paper, a design technique for implementing multi-channel incremental data converters to convert narrow bandwidth ac signals is discussed. It incorporates the operation principle, topology, and digital decimation filter design. The theoretical results are verified by simulation results.

키워드

Incremental Data Converters, multi-channel, multiplexing

Ⅰ. Introduction

The properties of incremental data converters (IDCs) suit the requirements of instrumentation and measurements (I&M), where high absolute accuracy and low power consumption are important. Unlike the conventional ΔΣADC operating continuously, the IDC is active for a predetermined number n of clock periods for each conversion cycle, after which all memory elements in the system are reset. The reset operation makes it possible for a single IDC to be multiplexed among many channels without multiplexing the memory elements.

The basic properties of IDCs used for DC measurement were described in [1]. A second-order IDC was discussed in [2]. A 22-bit 0.3 mW narrow-band IDC was also recently presented in [3]. [4] introduced the design theory of higher-order IDCs and also explained the trade-offs between different realizations.

In this paper, a design technique for implementing multi-channel incremental data converters to convert narrow bandwidth ac signals is discussed. It incorporates the operation principles, some topologies, and digital filter design. Finally, simulation results are described to verify the theory.

The paper is organized as follows. Section Ⅱ introduces the applications and overall requirements of a higher-order multi-channel incremental converter. Section Ⅲ describes the architecture and basic operation of the higher-order multi-channel incremental converter. In Section Ⅳ, a design methodology to optimize the signal-to-quantization+thermal noise ratio of multi-channel IDC and a design example are presented. Section Ⅴ draws the conclusions.

Ⅱ. Applications and Requirements

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Multi-channel IDCs can be utilized in power management (voltages, currents, temperatures, etc.), engine control (speed, fuel mix, etc.) and biomedical signal processing (EKG, EEG, etc.). These applications require the ADCs to be able to perform multi-channel data acquisition where many (N) low frequency analog signals have to be converted into a digital form.

These analog signals have narrow bandwidths (typically, f_B < 3 ㎑). Desirable requirements of the IDC architecture are: 1) large signal-to-quantization noise ratio (e.g., SQNR > 90 ㏈); 2) small chip area (e.g., 0.5 mm^2 for the complete ADCs); and 3) low power consumption (e.g., < 2 ㎽). The parallel analog-to-digital conversion of several channels carrying low frequency signals can be performed in various ways:

- Through parallel ADCs with a shared decimation filter. However, this architecture requires a large chip area and large power consumption.
- Through multiplexed ADCs and filters using replicated storage elements (capacitors and registers). Also in this case, the chip area is large and the structure is subject to inter-channel interference.
- Through multiplexed and reset incremental converters and decimation filters. This is the optimal choice adopted in this paper.

III. Architecture and Operation

Fig. 1 shows the system architecture of the multi-channel IDC, in which all channels share the same ΔΣ modulator and decimation filter.

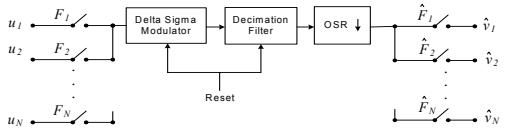

Fig. 1. Multi-channel IDC architecture.

When F_k is high, the k^{th} channel is active for the data conversion. The input signal u_k is applied to the ΔΣ modulator first and then is converted to a bit stream as y_k which goes into the decimation filter next. The last sample from the decimation filter output is the desired digital equivalent of u_k. After one conversion is completed, reset signal '1' is applied to both the ΔΣ modulator and the decimation filter for the data conversion of next channel.

Fig. 2(a) shows time domain signals u_k, x_k, y_k, w_k, v_k and Fig. 2(b) shows spectra of the signals in frequency domain.

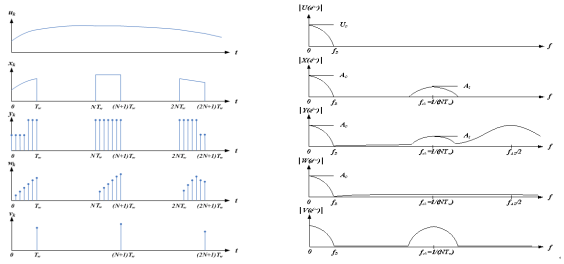

Fig. 2. Signals u_k, x_k, y_k, w_k, v_k in the k^{th} channel. (a) Time domain (b) Frequency domain.

In the N-channel structure, each channel carries a signal with a bandwidth f_B, which typically does not exceed a few ㎑. The time slot devoted by the ADC to each channel is denoted by T_W which can be considered as the duration time of a temporal window multiplying the input analog signal in each conversion cycle. The Nyquist theorem thus requires that the following constraint be met: $NT_w < 1/(2f_B)$, where N is the number of the channels.

During each conversion cycle, the ΔΣ modulator and the decimation filter are functional for n clock periods. For an L^{th} order IDC, at low frequencies, the SQNR is proportional to n^L, where n is the number of clock periods [3]. Thus, $n = f_C T_W$ f_C is the clock frequency, must be sufficiently large in order to achieve the desired SQNR.

Ⅳ. Design Methodology of Multi-channel IDCs

In Fig. 1, the decimated output of the system in the n^{th} conversion cycle is given by

$$v(n) = \{ stf(k) * h(k) * [u(k) + t(k)] + ntf(k) * h(k) * q(k) \}_{k=M-1} \quad (1)$$

Where $stf(k)$, $h(k)$ and $ntf(k)$ denote the inverse z-transforms of the signal transfer function, filter transfer and noise transfer function, respectively. Also, $u(k)$, $t(k)$ and $q(k)$ are the input, thermal noise and quantization noise sequences, respectively. The asterisk denotes the M-sample convolution operation between these sequences. For a given noise-shaping loop, and hence given stf, ntf, t and q the maximum Signal-to-Quantization+Thermal Noise Ratio (SQTNR) can be obtained by minimizing the quadratic cost function

$$\min_{\mathbf{h}} F(h) = \min_{\mathbf{h}} \mathbf{h}^T \cdot \mathbf{K} \cdot \mathbf{h} \quad (2)$$

$$\text{subject to } \mathbf{e}^{\mathrm{T}}\mathbf{h} = 1 \quad (3)$$

Here, $\mathbf{h}$ is a column vector containing the samples of $h(k)$, and $\mathbf{K}$ can be obtained from the parameters of the noise-shaping loop. By choosing these parameters appropriately, the filter impulse response can show minimum thermal noise, or minimum quantization noise. It is also possible to minimize an arbitrarily weighted average of the two noise powers.

Based on the new design methodology, a multi-channel IDC has been designed for the following specifications:

- Number of channels: N = 20;
- Analog signal bandwidth: f_B = 3 ㎑;
- Signal-to-noise ratio: SNR = 100 ㏈;
- Maximum clock rate: f_C = 30 ㎒;
- The maximum number of samples available to each channel is M = 250;

The delta-sigma loop which is suitable for these specifications is shown in Fig.3.

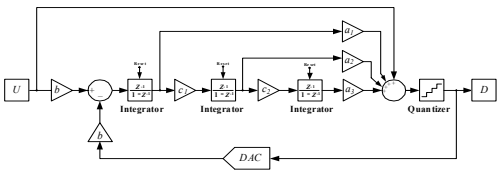

Fig. 3. Block Diagram of the delta-sigma loop.

A third-order cascade-of-integrators feed-forward (CIFF) structure is adopted for the Δ Σ modulator design with a 5-level quantizer. Its signal transfer function is 1; its noise transfer function is

$$NTF(z) = \frac{(1-z^{-1})^3}{1+(a_1b-3)z^{-1}+(a_2c_1b-2a_1b+3)z^{-2}+(a_1b-a_2c_1b+a_3c_1c_2b-1)z^{-3}} \quad (4)$$

Fig.4 illustrates the impulse response of $ntf(k)$.

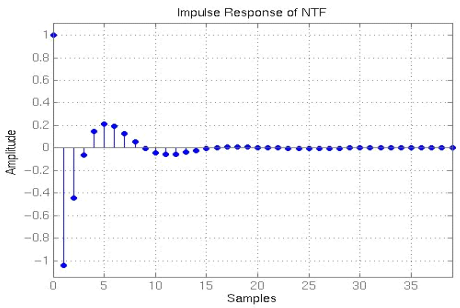

Fig. 4. Impulse response of noise transfer function.

The impulse response of the optimum digital decimation filter was found using the mathematical optimization process discussed above. Fig. 5 shows the resulting $h(k)$. The implementation is based on eq. (1): the digital output sequence $d(k)$ of the loop is convolved in real time with $h(k)$ for M clock periods. Thus, d(0).h(M-1) is found and stored, and then d(1).h(M-2) is added to it, etc. Since $d(k)$ can take on only 5 values, these operations are trivially simple.

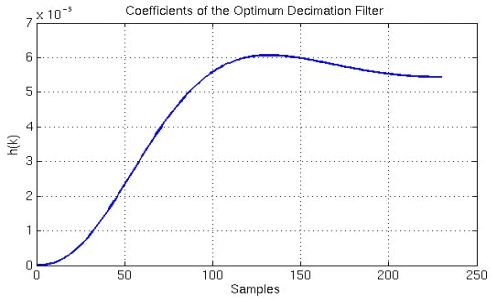

Fig. 5. The coefficients of the optimal decimation filter.

Fig.6 illustrates the simulated sweep of the conversion error for a dc input signal. Except at the two limits, where the quantizer overloads, the specifications are easily met. There are no peaks indicating idle tones, even though no dithering was used.

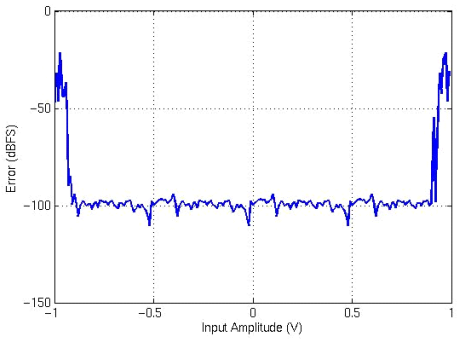

Fig. 6. DC sweep of the input vs error at the optimized FIR filter output.

V. Conclusions

This paper presented architecture and design methodology for multi-channel IDCs. The resolution/number of channels trade-off was explained and could be used to derive an upper bound for the number of multi-channels for a specified clock frequency and accuracy. Simple design methodology to maximize SQTNR of multi-channel IDCs was proposed. A design example and simulation results showed that the specification was easily satisfied with the proposed design methodology.

References

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