An Efficient Interpolation FIR Filter Using LUT

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Abstract— An efficient interpolation FIR filter structure for high-density and low-power electronic devices is proposed. The proposed structure is based on polyphase decomposition property and look-up table method. By computer-aided design simulations, it is shown that the use of the proposed method can result in reduction in the number of gates by 54% and can reduce power consumption by 9%.

Index Terms— High-density, Low-Power, Ployphase decomposition, Look-up table, Interpolation FIR filter

I. INTRODUCTION

High-density and low-power features are key factors of mobile communication devices and portable multimedia terminals. Interpolation FIR (finite impluse response) filter is required in mobile station and is used as a baseband pulse-shaping filter to minimize ISI (Inter-Symbol Interference) at the receiver [1], [2]. It requires a large portion of total silicon space and consumes a large fraction of total power since its output data rate is several times higher than input data rate due to the interpolation operation. It can be noticed that it is very important to reduce gate count and power consumption of the interpolation FIR filter.

Interpolation FIR filter can be implemented using transversal FIR filter design method or LUT (look-up table) design method [3], [4]. 1:4 interpolation filter using a 48-tap transversal FIR filter structure with 1-bit input and 10-bit output is shown in Fig. 1. It can be implemented with 11 10-bit adders and 44 10-bit registers. In Fig. 1, C_0, C_1, ..., C_{47} represent coefficient of filter transfer function $H(z)$.

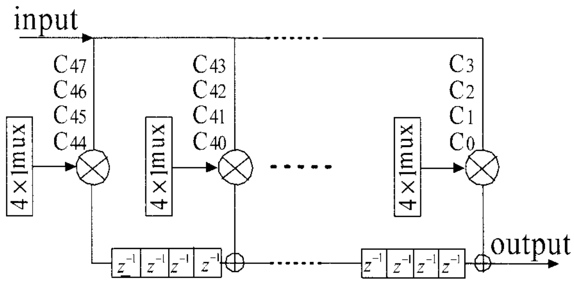

Fig. 1 Transversal FIR filter structure.

Although transversal FIR filter design method has the advantage of simplicity in implementation, it has the drawback of large chip area and slow processing time.

In LUT FIR filter design method, all the possible outputs which can be generated are stored in memory, and the filter outputs are selected by the input data stream. LUT FIR filter method can be efficiently implemented by applying polyphase decomposition to $H(z)$ as

$$H(z) = G_0(z^4) + z^{-1}G_1(z^4) + z^{-2}G_2(z^4) + z^{-3}G_3(z^4) \quad (1)$$

The sub-filters $G_0(z)$, $G_1(z)$, $G_2(z)$, and $G_3(z)$ can be implemented by a LUT [3]. Because FIR filter output with LUT is simply determined by input data stream, processing time of LUT FIR filter is shorter than that of transversal FIR filter.

In this paper, it is shown that the chip area and power consumption of the LUT method can be greatly reduced by exploiting the linear phase property of the decomposed sub-filter coefficients.

The paper is organized as follows. In section Ⅱ, we present conventional interpolation filter with LUT. The proposed LUT structure is described in section Ⅲ. In section Ⅳ, simulation results obtained by the proposed structure and conventional structure are

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evaluated and discussed. Finally, section V draws the conclusions.

II. LUT FIR FILTER DESIGN METHOD

By (1), $H(z)$ has linear phase property and can be divided into four sub-filters as shown in Table 1.

Table 1. Coefficient of each sub-filter

G_0	$C_0 C_4 C_8 C_{12} C_{16} C_{20}$	$C_{23} C_{19} C_{15} C_{11} C_7 C_3$
G_1	$C_1 C_5 C_9 C_{13} C_{17} C_{21}$	$C_{22} C_{18} C_{14} C_{10} C_6 C_2$
G_2	$C_2 C_6 C_{10} C_{14} C_{18} C_{22}$	$C_{21} C_{17} C_{13} C_9 C_5 C_1$
G_3	$C_3 C_7 C_{11} C_{15} C_{19} C_{23}$	$C_{20} C_{16} C_{12} C_8 C_4 C_0$

Fig. 2 shows a 1:4 interpolation FIR filter structure with LUT method [3]. In Fig. 2, number of taps are 48, word-length of input data is 1-bit, and word-length of output data is 10-bits. The serial input is converted into the parallel form, which is used as address for the four sub-look-up tables.

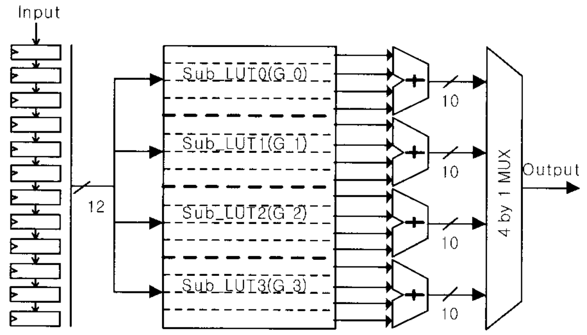

Fig. 2. 1:4 interpolation FIR filter with LUT.

In this structure, four sub-filtering operations are performed simultaneously. Since each sub-filter is composed of 12 coefficients as can be seen in Table 1, 12-bits must be used as an address for the look-up table. Also, since the address size for each sub-look-up table is 12-bits, the required size of each sub-look-up table is 2^{12}. In practical implementations, to avoid the overhead of large look-up table size, the input address is partitioned as shown in Fig. 2. By using the structure in Fig. 2, the total look-up table size reduces to $4{\times}4{\times}2^3$. Notice that in Fig. 2, the reduction in the look-up table size is achieved with the penalty of 4×2 10-bit carry-save adders and four 10-bit ripple carry adders.

III. PROPOSED LUT DESIGN METHOD

In Table 1, the first half of the coefficients of G_0 (i.e., C_0, C_4, ...,C_{20}) is symmetric with the second half of the coefficients of G_3. Also, the second half of the coefficients of G_0 is symmetric with the first half of the coefficients of G_3. The same relation also holds true for G_1 and G_2. This means that an output can be computed by using only the first half of the coefficients of each sub-filter. A filter structure exploiting the symmetric characteristics of the coefficients can be implemented as shown in Fig. 3 [5].

Although the area of the look-up table is reduced by half, additional logic blocks, such as demux and buffer, should be used for the outputs of four sub-filtering operations. Also, it is difficult to use carry-save adders since the adders are located separately.

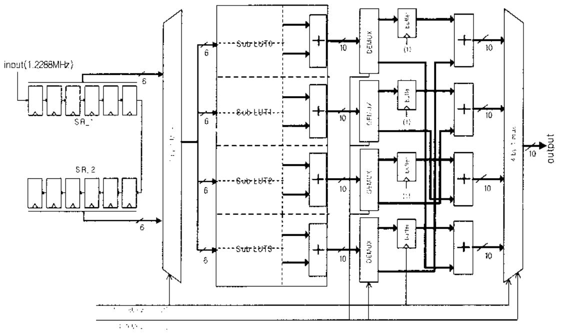

Fig. 3. LUT reduction structure.

Fig. 4 shows the proposed LUT FIR filter structure. Input data (1-bit) stream is shifted along with two 6-bit shift registers SR_1 and SR_2 clocked by clk_1. The outputs from SR_1 and SR_2 are connected to a 2×4 demux. The clock signal clk_1 is used as a select signal for the demux. When clk_1 is high, the outputs of SR_1 are transmitted to the "o1" and "o2" output lines of the demux and the outputs of SR_2 are transmitted to the "o3" and "o4" output lines of the demux. If clk_1 is low, then the outputs of SR_1 are transmitted to the "o3" and "o4" signal lines and the outputs of SR_2 are transmitted to the "o1" and "o2" signal lines. Due to the symmetry among the coefficients in Table 1, the output lines of SR_2 should be connected to the demux input lines in reverse order.

The output signals from the demux are used as address inputs for the look-up table. Notice that the input address size of the proposed structure is 6-bits instead of 12-bits since the first half of each sub-filter is composed of only six coefficients. The 6-bit address inputs can be partitioned into two 3-bit address inputs as shown in Fig. 4. Thus the size of the entire look-up table is reduced by half compared with that of the structure in Fig. 2. The look-up table is composed of four sub-look-up tables. One sub-filtering is performed by adding the outputs from two sub-look-up tables. For example, sub-filtering G_0 and G_3 are performed by adding the outputs from the first and the fourth sub-look-up tables. And sub-filtering G_1 and G_2 are performed by adding the outputs from the second and the third sub-look-up tables.

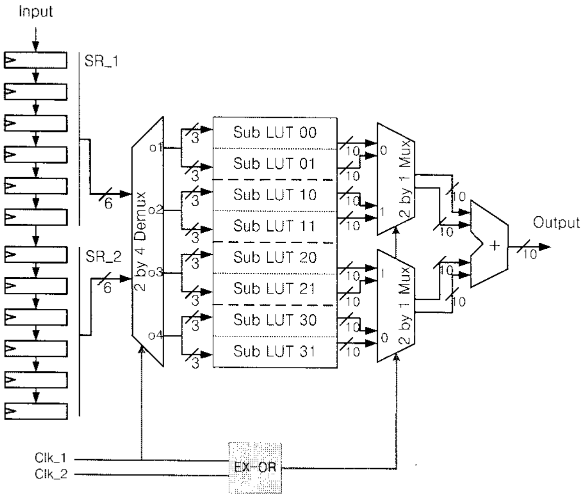

Fig. 4. Proposed interpolation FIR filter structure.

In the proposed structure, two 2×1 Muxs are used to select proper sub-look-up tables and an adder generates final output using signals from two Muxs. When signals from clk_1 (1.2288MHz) and clk_2 (2.4576MHz) are "00", sub-look-up table blocks 00 and 01 are selected by upper Mux and sub-look-up table blocks 30 and 31 are selected by lower Mux. And final output G_0 is obtained by an adder using those sub-look-up table blocks. When clk_1 and clk_2 are "01", sub-look-up table blocks 10 and 11 are selected by upper Mux and sub-look-up table blocks 20 and 21 are selected by lower Mux. And final output G_1 is obtained by adding signals from those sub-look-up table blocks. Two 10-bit carry save adders and one 10-bit ripple-carry adder are used. It can be noticed that area of adders is reduced by 75% compared to that of Fig. 2.

IV. EXPERIMENTAL RESULTS

Synopsys VHDL simulator, logic optimizer, and power analyzer were used for comparison of circuit area and power consumption among transversal filter design method in Fig. 1, conventional look-up table design method in Fig. 2, and the proposed design method in Fig. 4. Table 2 compares the gate counts and power consumption of three types of design methods. Since the structure in Fig. 1 is implemented with eleven 10-bit adders and 44 10-bit registers, a large number of gates are needed. Moreover it consumes about three times more power than the look-up table structures. It can be seen that the use of the proposed method results in reduction in the number of gates by 54%. The size of entire look-up table is reduced by 50% and the size of adders is reduced by 75% compared to those of Fig. 2. Although the number of gates required by the proposed method is only 46% of that of the structure in Fig. 2, the proposed structure reduces power consumption by 9% since some parts of the proposed structure operate two times faster than the structure in Fig. 2.

Table 2. Comparison of area and power consumption

	Area (number of gates)	Power (μW)
Transversal filter	6774	31.6813
Conventional look-up table	2382	10.2083
Proposed look-up table	1096	9.2896

IV. CONCLUSIONS

An efficient interpolation FIR filter structure for electronic devices with high-density and low-power properties has been proposed. The area of proposed LUT structure was reduced by 54% considering polyphase decomposition property and exploiting the symmetric characteristics of the coefficients. Although some parts of the proposed structure operated two times faster than the conventional LUT structure, power consumption of the proposed structure was reduced by 9%.

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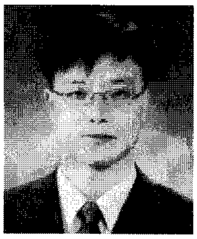

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