2D Transconductance to Drain Current Ratio Modeling of Dual Material Surrounding Gate Nanoscale SOI MOSFETs

N.B.Balamurugan, K.Sankaranarayanan, and M.Fathima John

Abstract—**The prominent advantages of Dual Material Surrounding Gate (DMSG) MOSFETs are higher speed, higher current drive, lower power consumption, enhanced short channel immunity and increased packing density, thus promising new opportunities for scaling and advanced design. In this Paper, we present Transconductance-to-drain current ratio and electric field distribution model for dual material surrounding gate (DMSGTs) MOSFETs. Transconductance-to-drain current ratio is a better criterion to access the performance of a device than the transconductance. This proposed model offers the basic designing guidance for dual material surrounding gate MOSFETs.**

Index Terms—**Silicon-on-insulator (SOI) technology, dual material surrounding gate (DMSGT) MOSFETs, surrounding gate (SGT) MOSFETs, transconductance-to-drain current ratio (g_m/I_{ds}), short channel effects (SCEs), drain-induced barrier lowering (DIBL)**

I. Introduction

In recent years, a number of non-classical MOSFETs have been proposed as device structures to sustain the growth of CMOS technology into nanoscale. The DMSG MOSFET is considered the most attractive device to succeed the planar MOSFETs [1]. Higher current drive, enhanced short channel immunity, higher reliability and increased packing density have been reported by many theoretical and experimental studies on this device [2-4]. Transconductance of a device represents the amplification delivered by the device and the drain current represents the power dissipated to obtain that amplification. This ratio shows that how efficiently the current is used to achieve a certain value of transconductance. Hence transconductance-to-drain current ratio is a better criterion to access the performance of a device than the transconductance and is therefore referred as the quality factor of a device [5]. Therefore, transconductance-to-drain current ratio is an important parameter that governs the transconductance generation efficiency of a device, and plays a major role for achieving a highly improved CMOS technology performance. Further, the maximum voltage gain of a MOSFET occurs when the value of transconductance-to-drain current ratio is largest. Thus higher values of transconductance-to-drain current ratio (g_m/I_{ds}) are extremely important for analog applications.

Compact and accurate models of the transconductance-to-drain current ratio for DMSG MOSFETs are needed in order to facilitate and extend the use of these devices in integrated circuits. Rajendran et al [6], proposed a design methodology based on the surface potential approach of finding the transconductance-to-drain current ratio and body factor n of FD DG SOI MOSFETs. Kranti et al [7], proposed a new design methodology that allows for the estimation of device parameters of VSG and DG MOSFETs to enhance the transconductance-to-drain current ratio (g_m/I_{ds}). But these above models cannot be applied to DMSG devices.

To incorporate the advantages of both DMG and SG

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structures, Kumar et al [2] has proposed a new structure, Dual Material surrounding gate MOSFET in which the SG consists of two materials with different work functions. But they overlooked the short-channel effects of such devices. Chiang et al [3] have reported a model for the 2-D potential distribution of DMSG MOSFETs by using the superposition technique. Despite accuracy of the above model, it involves a lot of mathematical complexity and makes its understanding and application difficult. Research till date on DMSG MOSFETs has focused on modeling of threshold voltage characteristics [2,8] only. None of them provides the explicit transconductance-to-drain current ratio expression to give the physical insight into the device physics of DMSG MOSFETs. Thus to gain insight into the device physics and optimize the device parameters for improved performance, an accurate model for transconductance-to-drain current ratio (g_m/I_{ds}) of DMSG MOSFET needs to be developed.

Recently, we have reported a model for threshold voltage of dual material surrounding gate (DMSG) SOI MOSFETs based on the solution of 2-D Poisson's equation [8]. In this paper, it is extended to model the transconductance-to-drain current ratio and electric field distribution in DMSG MOSFETs. The dependence of silicon film thickness and drain source voltage are accounted for. The accuracy of the model is verified by comparing the model results with the simulation results using the 2-D device simulator MEDICI [9]. Close proximity with published results confirms the validity of the present model.

II. TRANSCONDUCTANCE TO DRAIN CURRENT RATIO MODEL

A schematic view of the DMSG nanoscale MOSFET is shown in Fig. 1 along with spherical coordinate system consists of a radial direction r, a vertical direction z, and an angular component θ in the plane of the radial direction. The Gate consists of two materials M_1 & M_2 with gate lengths L_1 and L_2 and two different work functions V_{b1} and V_{b2}. The relation among the surface potential, charge, and electric field are derived by solving the Poisson's equation in the silicon pillar. The influence of the charge carrier and the fixed charges on the electrostatics of the channel is assumed to be

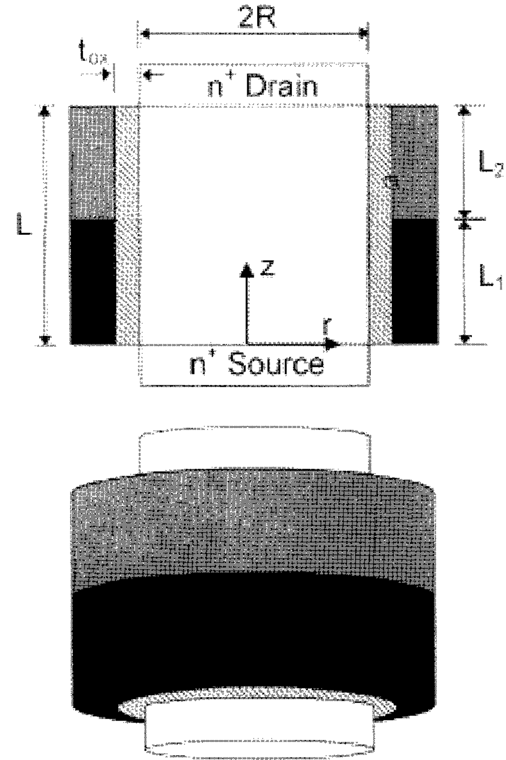

Fig. 1. Schematic view of dual material surrounding gate MOSFETs.

neglected. The potential distribution ϕ(r, z) in fully-depleted DMSG MOSFETs is

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,z)}{\partial r}\right)+\frac{\partial^2\phi(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}} \quad (1)$$

Where $\phi(r,z)$ is the potential distribution in the silicon film, q is the electron charge, N_a is the silicon film doping concentration, and ε_{si} is the permittivity of the silicon film.

The potential distribution in fully depleted silicon film is assumed to be a parabolic profile [10] in radial direction. Using the boundary conditions given in [2], the potential distribution in the silicon film is obtained as

$$\phi(r,z)=\phi_s(z)+r^2\left(\frac{\varepsilon_{ox}}{2R^2\varepsilon_{si}}\frac{V_{GS}-V_{FB}-\phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right) \quad (2)$$

Where $\phi_S(z)$ is the potential at the surface of the silicon film, $2R$ is the diameter of the silicon pillar, t_{ox} is the silicon –oxide thickness, ε_{ox} is the permittivity

of the oxide layer, t_{si} is the thickness of the silicon film, V_{GS} is the gate-source voltage, V_{FB} is flat – band voltage.

Using the same procedure as in our earlier paper [8], the potential in the SOI film $\phi_{s1}(z)$ and $\phi_{s2}(z)$ under metals M_1 & M_2 can be expressed as

$$\phi_{s1}(z) = A\exp(Pz) + B\exp(-Pz) - S_1$$

$$\text{for} \quad 0 \le z \le L_1 \quad \text{under } M_1 \tag{3}$$

$$\phi_{s2}(z) = C\exp(P(z-L_1)) + D\exp(-P(z-L_2)) - S_2$$

$$\text{for} \quad L_1 \le z \le L_1 + L_2 \quad \text{under } M_2 \tag{4}$$

$$\text{Where, } A = \frac{G\cosh(PL_2) + E - F\exp(-PL)}{2\sinh(PL)} \tag{5}$$

$$B = \frac{G\cosh(PL_2) + F\exp(-PL) - E}{2\sinh(PL)} \tag{6}$$

$$C = \frac{G}{2} + 2A\exp(PL_1) \tag{7}$$

$$D = \frac{G}{2} + 2B\exp(PL) \tag{8}$$

$$P = \sqrt{\frac{2\varepsilon_{ox}}{R^2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)}} \tag{9}$$

$$\text{Where } G = S_1 - S_2, \quad S_1 = \frac{Q_1}{P^2}, \quad S_2 = \frac{Q_2}{P^2} \tag{10}$$

$$E = V_{bi} + V_{ds} + S_2 \tag{11}$$

$$F = V_{bi} + S_2 \tag{12}$$

$$\text{Where, } Q_1 = \frac{qN_a}{\varepsilon_{si}} - P^2(V_{GS} - V_{FB}) \tag{13}$$

$$Q_2 = \frac{qN_a}{\varepsilon_{si}} - P^2(V_{GS} - V_{FB}) \tag{14}$$

Where V_{bi} is the built in potential between the source and the body, V_{ds} is the drain-source voltage, L is the channel length and also Q parameter corresponds to the respective regions.

In the case of the DMSGT structure, due to the coexistence of two metal gates with different work functions, the surface potential minimum is solely determined by the metal gate with the higher work function. Therefore the minimum surface potential of the silicon pillar under the gate can be calculated as,

$$\phi_s(z_{\min}) = 2\sqrt{AB} - \frac{Q_1}{P^2} \tag{15}$$

in which the minimum occurs at,

$$z_{\min} = \frac{1}{2P}\ln\left(\frac{B}{A}\right) \tag{16}$$

Therefore the position of minimum surface potential $Z_{\min}$ is obtained as

$$z_{\min} = \frac{\lambda_{dmsg}}{2}\ln\left(\frac{G\cosh(PL_2) + F\exp(-PL) - E}{G\cosh(PL_2) + E - F\exp(-PL)}\right) \tag{17}$$

Where λ_{dmsg} is the characteristics length or natural length of dual material surrounding gate MOSFET which characterizes the SCEs is expressed as

$$\lambda_{dmsg} = \frac{1}{P} = \sqrt{\frac{R^2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)}{2\varepsilon_{ox}}} \tag{18}$$

Therefore the potential $\phi_s(z_{\min})$ at $z_{\min}$ is obtained as,

$$\phi_s(z_{\min}) = \frac{\sqrt{G^2\cosh^2(PL_2) - (E - F\exp(-PL))^2}}{\sinh(PL)} - \frac{qN_a}{\varepsilon_{si}P^2} + V_{GS} - V_{FB} \tag{19}$$

The g_m/I_{ds} ratio is a direct measure of the efficiency of the transistor, since it represents the amplification (g_m) obtained from the device, divided by the energy supplied to achieve this amplification (I_{ds}). It is a measure of the effectiveness for the control of the drain current by the gate voltage.

The transconductance-to-drain current ratio (g_m/I_{ds}) is given [7] by,

$$\frac{g_m}{I_{ds}} = \frac{q}{kT}\left(\frac{\partial\phi_s(z_{\min})}{\partial V_{GS}}\right) \tag{20}$$

Where, $\phi_s(z_{\min})$ is the minimum surface potential, k is the Boltzmann's constant and T is temperature in Kelvin. Differentiating (19) with respect to V_{GS}, we get

$$\frac{\partial\phi_s(z_{\min})}{\partial V_{GS}} = \frac{1}{2\sqrt{AB}\sinh^2(PL)}\left[(F\exp(-PL) - E)(\exp(-PL) - 1)\right] + 1 \tag{21}$$

Substituting (21) in (20), the transconductance-to-

drain current ratio (g_m/I_{ds}) for DMSG MOSFET is obtained as

$$\frac{g_m}{I_{ds}} = \frac{q}{kT}\left\{\frac{1}{2\sqrt{AB}\sinh^2(PL)}[(F\exp(-PL)-E)(\exp(-PL)-1)]+1\right\} \quad (22)$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field component in the r–direction, under the metal gate M_1 is given as

$$E_1(z) = \left.\frac{\partial\phi_{S1}(r,z)}{\partial r}\right|_{r=0} = AP\exp(Pz) - BP\exp(-Pz) \quad (23)$$

Similarly the electric field pattern, in r–direction, under gate M_2 is given as

$$E_2(z) = \left.\frac{\partial\phi_{S2}(r,z)}{\partial r}\right|_{r=0} = CP\exp(P(z-L_1)) - DP\exp(-P(z-L_2)) \quad (24)$$

The above two equations are quite in determining how the drain side electric field is modified by the proposed DMSG structure.

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the calculated surface potential profile for a channel length of 100 nm ($L_1 = L_2 = 50$ nm) of the DMSG structure along with the calculated potential profile of the SMSG structure. It is clearly seen from the figure that due to the presence of DMSG, there is no significant change in the potential under the gate M_1 even as the drain bias is increased. Hence the channel region under M_1 is "screened" from the changes in the drain potential (i.e.) the drain voltage is not absorbed under M_1 but M_2. As a consequence V_{ds} has only a very small influence on drain current after saturation and the drain conductance is reduced. It is evident from the figure that there is a negligible shift in the point of the minimum potential and it lies almost at the interface of the two metal gates irrespective of the applied drain bias.

In the case of DMSG MOSFETs, Drain-Induced Barrier Lowering (DIBL) effect can be efficiently reduced by increasing V_{ds} as compared to the SMSG MOSFETs. The model predictions correlate well with the simulation results proving the accuracy of our proposed analytical model.

Fig. 3 shows the calculated and simulated values of the electric field along the channel length at the drain end for the DMSG SOI MOSFET and the simulated values for the SMSG SOI MOSFET for the same channel length. Because of the discontinuity in the surface potential of the DMSG structure, the peak electric field at the drain is reduced substantially, by approximately 40%, when compared with that of the SMSG structure that leads to a reduced hot carrier effects. As shown in the figure the results from the analytical model are in close proximity of the simulation results.

The transconductance-to-drain current ratio with respect to the channel length, depending on the silicon

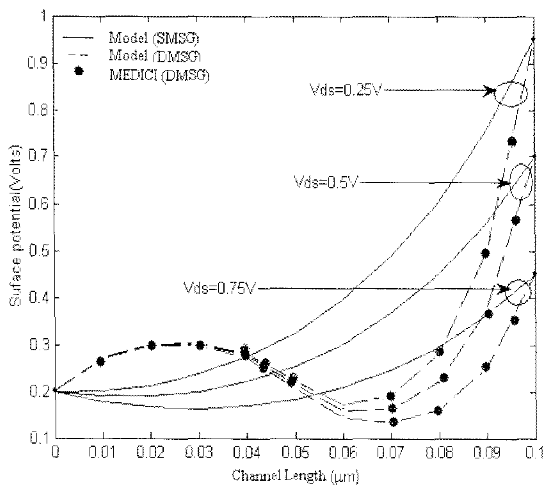

Fig. 2. Surface potential profiles of DMSG and SMSG MOSFETs for channel length, L = 100 nm for different drain biases.

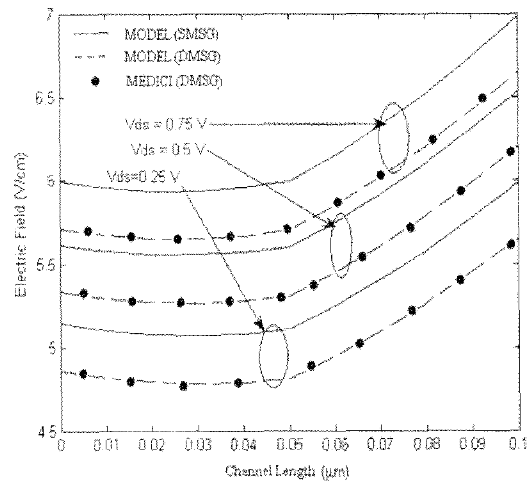

Fig. 3. Longitudinal electric field along the channel toward the drain end obtained from the analytical model in SMSG and DMSG MOSFETs for varying drain voltages.

film thickness is shown in Fig. 4. As the silicon film thickness reduces, the transconductance-to-drain current ratio gets increased for a particular channel length. Therefore, the reduced silicon film thickness yields higher transconductance-to-drain current ratio for optimized performance. It is observed that t_{si} = 50 nm and at L= 180 nm, the corresponding g_m/I_{ds} ratio is 38 V^{-1} because thin-film SOI MOSFETs have a much lower leakage current than bulk SOI devices. Off-state leakage currents smaller than 1 fA μm^{-1} are indeed observed in FD thin - film devices together with suppression of SCEs. The results have been compared with the simulated results using MEDICI simulator and a good agreement achieved between two.

The transconductance-to-drain current ratio (g_m/I_{ds}) with respect to the channel length for a particular drain-source voltage on DMSG MOSFETs is shown in Fig. 5. In addition, the calculated transconductance-to-drain current ratio (g_m/I_{ds}) for DG and SMSG MOSFETs are included and compared to the model. From the Fig. 5, it can be seen that DMSG MOSFETs offers higher transconductance-to-drain current ratio values at channel lengths. DMSG MOSFETs show higher g_m/I_{ds} values when compared with DG and SMSG MOSFETs, thus showing their ability to attain higher transconductance generation efficiency. As channel length is increased, g_m/I_{ds} attain the ideal value of q/kT whereas for smaller lengths, short channel effects dominate and g_m/I_{ds} fall appreciably. Thus DMSG MOSFETs will be more useful for analog circuits application where higher g_m/I_{ds} values are desired over large range of voltages and device parameters.

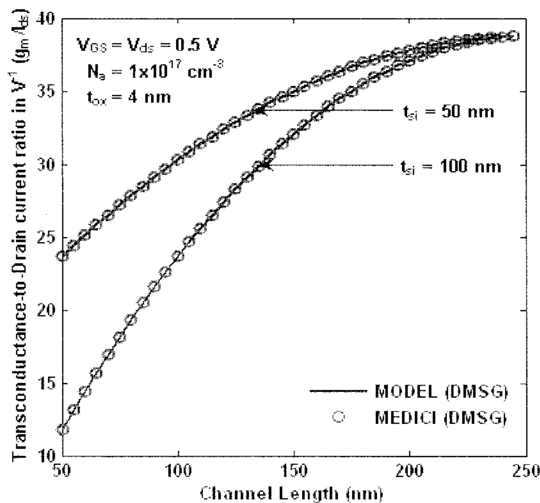

Fig. 4. Transconductance-to-drain current ratio as a function of channel length by varying the silicon film thickness (t_{si}).

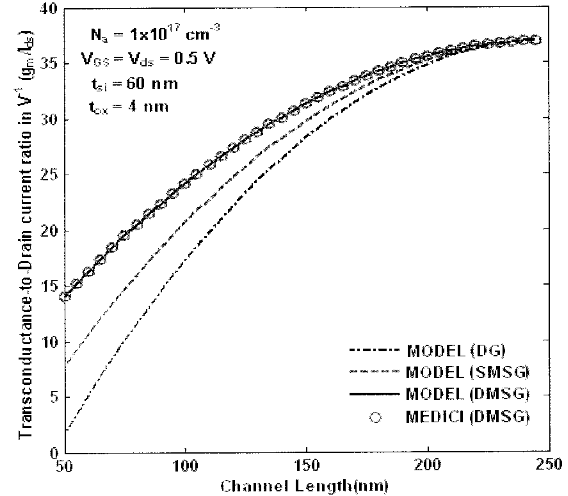

Fig. 5. Variation of Transconductance-to-drain current ratio with channel length at a fixed drain-source voltage, V_{ds} =0.5 V for DG, SMSG and DMSG MOSFETs.

IV. CONCLUSIONS

The transconductance-to-drain current ratio and electric field distribution model for dual material surrounding gate MOSFETs has been developed with higher speed, higher density, and enhanced short channel immunity. DMSG MOSFETs achieve higher g_m/I_{ds} values for all sets of device parameters and voltages as compared to DG and SMSG MOSFETs. g_m/I_{ds} value of DMSG MOSFETs does not collapse at smaller gate lengths and larger silicon film thickness and gate oxide thickness unlike that of DG MOSFETs. DMSG MOSFETs allow greater flexibility in selecting device parameters to achieve the desired g_m/I_{ds} values. Therefore DMSG MOSFETs are superior to DG and SMSG MOSFETs in terms of transconductance generation efficiency and is therefore referred as the quality factor of the device. The accuracy of results obtained using our analytical model is compared with DG and SMSG MOSFETs and is verified using 2-D numerical simulation. The results unambiguously establish th. the incorporation of DMSG structure in a FD SOI MOSFET leads to subdued short-channel effects due to a step-function in the surface potential profile. The shift in the surface potential minima position is negligible with increasing drain biases. The electric field in the channel at the drain end is also reduced leading to reduced hot-carrier effect.

Thus the model provides basic designing guidelines for dual material surrounding gate (DMSG) MOSFETs.

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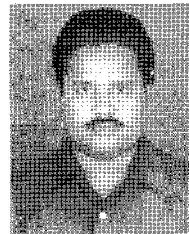

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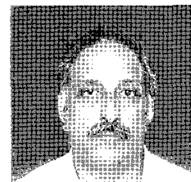

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