A Reduced-Swing Voltage-Mode Driver for Low-Power Multi-Gb/s Transmitters

Heesoo Song, Suhwan Kim, and Deog-Kyoon Jeong

Abstract—**At a lower supply voltage, voltage-mode drivers draw less current than current-mode drivers. In this paper, we newly propose a voltage-mode driver with an additional current path that reduces the output voltage swing without the need for complicated additional circuitry, compared to conventional voltage-mode drivers. The prototype driver is fabricated in a 0.13-μm CMOS technology and used to transmit data streams at the rate of 2.5 Gb/s. De-emphasis is also implemented for the compensation of channel attenuation. With a 1.2-V supply, it dissipates 8.0 mA for a 400-mV output voltage swing.**

Index Terms—**High-speed interface, low power, voltage-mode driver, output driver**

I. INTRODUCTION

As scaling of the CMOS process progresses, systems continue to process more data. Now the bottleneck is no longer the data-processing capability of chips but the bandwidth of inter-chip communication. This has motivated a lot of researches on high-speed interface circuits [1,2]. Currently, many high-speed interface specifications such as XAUI, SATA and PCI-Express have emerged to address the increasing bandwidth of inter-chip communications.

One of the blocks that consumes the most of power in high-speed interface circuits is the driver, which sends data streams through a low impedance channel. Reducing the power consumption of drivers therefore offers a very significant benefit to low-power systems. Although the supply voltages of digital circuits continue to decrease for reducing the power consumption, widely employed current-mode drivers do not draw less current at a lower supply voltage [3,4]. Voltage-mode drivers do consume less current at a lower supply voltage in contrast to current-mode drivers. However they have the difficulty that they requires an additional low-voltage supply for reducing the output voltage swing, since the output voltage swing is constrained by the supply voltage [5-8].

In this paper, we describe a simple but efficient technique to design a voltage-mode driver, which reduces the output voltage swing so that the total drawn current is cut down.

Manuscript received May 11, 2009; revised Jun. 10, 2009.
School of Electrical Engineering, Seoul National University, San 56-1, Shinlim-dong, Kwanak-gu, Seoul, 151-742, Korea
E-mail : climber@mystic.snu.ac.kr

II. PREVIOUS DRIVER DESIGN

1. Current-Mode Drivers

Fig. 1 shows the current-mode driver which is usually preferred in transmitters for multi-Gb/s wire-line communication because of the simple design and high-speed capability [3,4]. In a high-speed transceiver, terminations

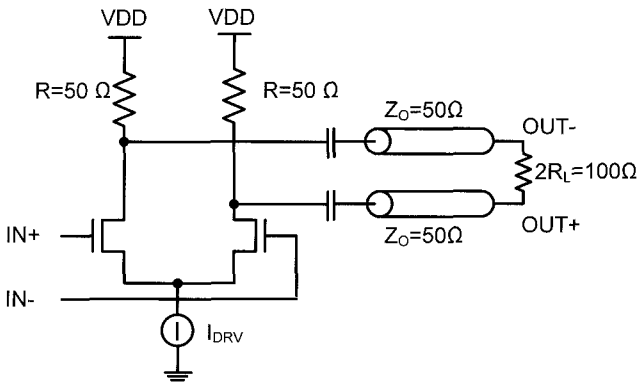


Fig. 1. Current-mode driver with ac-coupling.

at both the source, or transmitter, and the load, or receiver, are requisite to eliminate the reflections which originate from impedance mismatches. This double termination causes the current-mode driver to consume a remarkably high current, since the resistance seen by the driver's output is decreased to half of the load resistor thanks to the resistor at the output node for source termination. Moreover, reduction of the supply voltage does not cut the drawn current at the condition of the same output voltage swing since the drawn current determines the output voltage swing.

When ac-coupling is employed, the design constraints become harsher. The minimum voltage of the driver output is decreased to V_{DD}-1.5*$I_{DRV}R_{EQ}$ whereas it is V_{DD}-1.0*$I_{DRV}R_{EQ}$ without employing ac-coupling, where R_{EQ} means an equivalent resistance of parallel connected R_L and R. The consequently decreased overdrive voltages of transistors for the input pair and the current source demand that the transistors be wider for the capability of driving the same current.

2. Voltage-Mode Drivers

Fig. 2 shows the architectures of the previously published low-swing voltage-mode drivers. They consume less current and introduce ac-coupling without modifying the design, compared to current-mode drivers. In Fig. 2 (a), two NMOS transistors act as push and pull resistor [5,6]. NMOS transistors of the driver are operated as resistors since the gate voltage of a driver's NMOS transistor is much higher than the supply voltage of the driver in that configuration. These voltage-mode drivers require an additional external low-voltage supply to attain a low-swing output voltage since the output voltage swing is determined to half of the supply voltage, as we will explain in more detail. An external voltage source can be substituted for an on-chip regulator, as shown in Fig. 2 (b) [7]. The output voltage swing then can be controllable by changing the regulated supply voltage and the output resistance of the driver is adjusted to 50 Ω by another feedback loop with a replica driver, which is not shown in the figure. However, it has a drawback that it requires a regulator, which is a complicated analog circuit and demands a consequent large capacitor at the regulated supply for ac ground.

Employing only termination on the receiver side, in which the source impedance is made much larger than

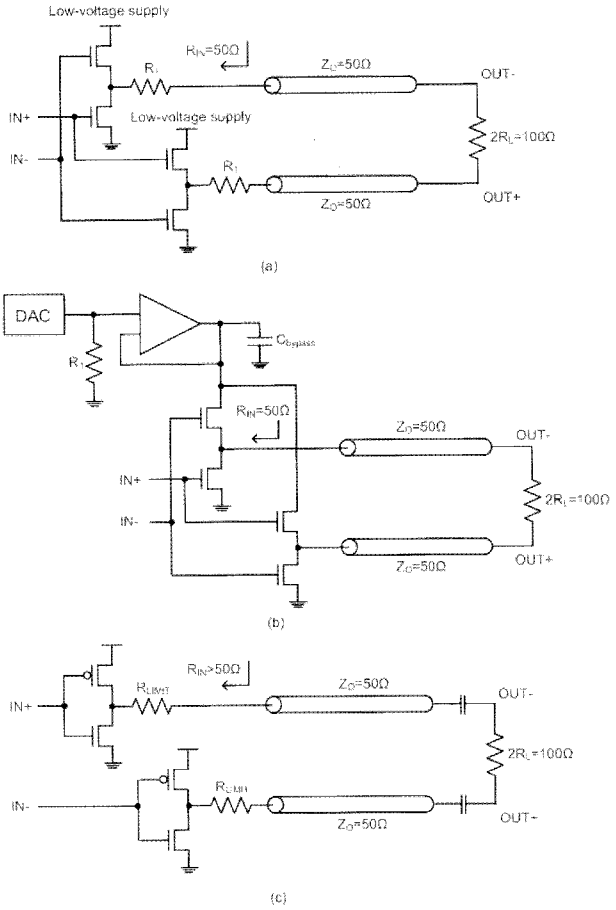


Fig. 2. Previous voltage-mode drivers. (a) voltage-mode driver with a low-voltage supply. (b) voltage-mode driver with a regulator. (c) voltage-mode driver with only receiver-side termination.

the channel impedance, is itself sufficient to cut the drawn current, as shown in Fig. 2 (c) [8]. However, the resultant impedance mismatch between the source and the channel makes it unsuitable for multi-Gb/s communication applications.

III. Proposed Reduced-Swing Voltage-Mode Driver

1. Reducing The Output Voltage Swing

Fig. 3 shows the configuration of the reduced-swing voltage-mode driver, which incorporates a supplementary resistor R_B to make an additional current path [9]. The following relation between R_A and R_B should be met to terminate the source correctly:

$$R_A // R_B = Z_O, \quad (1)$$

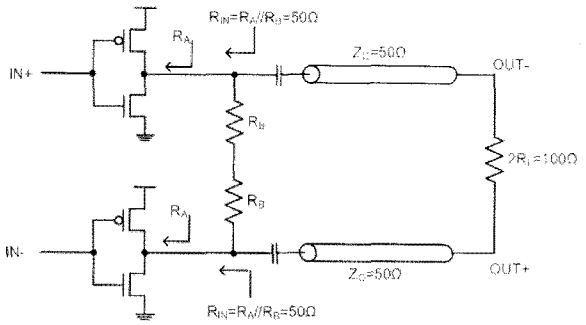


Fig. 3. Reduced-swing voltage-mode driver.

where R_A is the output resistance of the inverter, as the on-resistances of PMOS and NMOS of the inverter are assumed to be same. In this configuration, a part of the driver's drawn current flows through the additional path of R_B resulting in the decreased voltage at the load. If the less output voltage swing is demanded, R_B is made decreased and R_A increased to hold the equation above. The total increased resistance between supply and ground leads to less drawn current with the reduced output voltage swing.

Assuming that the source and load resistances are matched to the channel impedance, the output voltage swing can be calculated as the followings:

$$\begin{aligned} V_{SWING} &= V_{OUT+} - V_{OUT-} \\ &= V_{DD} \times \frac{2R_B // 2R_L + R_A}{R_A + 2R_B // 2R_L + R_A} - V_{DD} \times \frac{R_A}{R_A + 2R_B // 2R_L + R_A} \\ &= V_{DD} \times \frac{R_B // R_L}{R_A + R_B // R_L}, \end{aligned} \quad (2)$$

where V_{DD} is the supply voltage and R_L is the, typically 50 Ω, load resistance.

The current drawn by the driver can be also calculated as followings:

$$I_{DRIVER} = \frac{V_{DD}}{2R_A + 2R_B // 2R_L}. \quad (3)$$

In the case of the conventional voltage-mode drivers, there is no additional current path and R_B can be regarded as infinite. Therefore, the output voltage of the driver can be expressed as follows:

$$V_{SWING} = V_{DD} \times \frac{R_L}{R_A + R_L} = \frac{1}{2} V_{DD}$$

(conventional voltage-mode driver). (4)

Since all driver current flows through the load resistor,

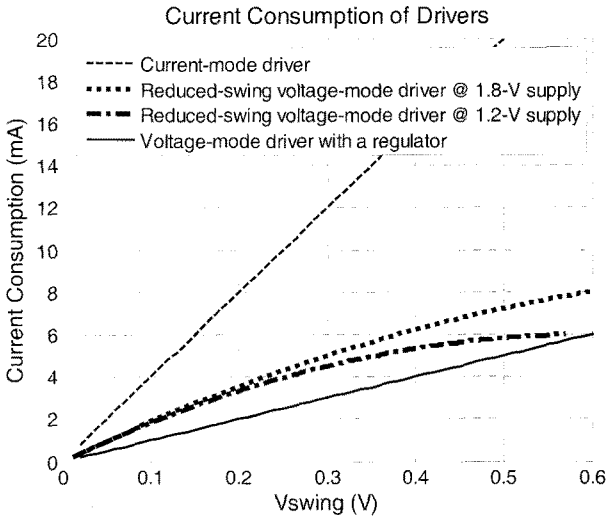


Fig. 4. Current consumption curves for the various drivers.

the output voltage swing becomes half of the supply voltage. The relation between the drawn current, the supply voltage and the output voltage swing is

$$I_{DRIVER} = \frac{V_{DD}}{2R_A + 2R_L} = \frac{V_{DD}}{200\Omega} = \frac{V_{SWING}}{100\Omega}$$

(conventional voltage-mode driver). (5)

Fig. 4 compares the current consumptions of the current-mode driver and various voltage-mode drivers. The curves represent the currents drawn by the drivers themselves and exclude the supplementary current from auxiliary circuitry such as a pre-driver and a regulator. The current consumption of the current-mode driver is V_{SWING}/R_{EQUIV} regardless of the supply voltage, where R_{EQUIV} is 25 Ω in the double-terminated configuration. The current consumed by the voltage-mode driver with a regulator is $V_{SWING}/100$ Ω, which is a quarter of that required by the current-mode driver, and its supply voltage is regulated to attain the desired voltage-swing. This involves a complicated analog circuit and a large area of capacitor.

In the case of the proposed driver, the current consumption is calculated with two supply voltages of 1.8 V and 1.2 V since the supply voltage has the relation with the current consumption; voltage-mode drivers draw less current at a lower supply voltage. For the 400-mV output voltage swing, which is the typical value for many multi-Gb/s transmitters, our driver has a lower design overhead than the voltage-mode driver with a regulator at the cost of slightly higher drawn current. However it is possible

that the voltage-mode driver with a regulator consumes more current than the proposed driver due to current drawn by a regulator.

2. Implementation of the Proposed Driver

Fig. 5 shows how we implemented our new voltage-mode driver with inverters and resistors. The on-resistance of inverters is typically made to be much smaller than the resistance of resistors since it is changed according to process, voltage and temperature variation. The driver uses a PMOS transistor as a pull-up resistor since all circuit in the driver block operates with a shared supply, unlike previous voltage-mode drivers which require an additional low-voltage supply.

De-emphasis to compensate the inter-symbol-interference due to the narrow bandwidth of the channel is implemented with an auxiliary driver, which have the weak strength and input signals of negative polarity and one-clock latency compared to a main driver [6]. When the input data has a transition, all the PMOS transistor or NMOS transistor is turned on and the driver operates as explained before. When the input data has no transition, there exists a resistor ladder from the supply to the ground and it makes an equivalent supply voltage to have a lower voltage than the original value. The output voltage reduces in consequence. It is noteworthy that this spilt driver does not change the output resistance.

De-emphasis can alternatively be implemented by changing the resistance of R_A and R_B simultaneously. However the exact matching of the resistors and the precise timing of input signals make the design too intricate to be attractive.

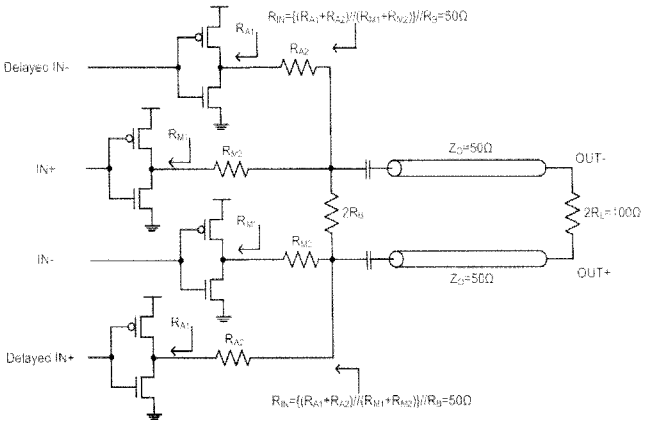


Fig. 5. Implementation of the proposed driver.

IV. Experimental Results

An experimental 2-channel serial link is fabricated in a 0.13-μm CMOS technology and packaged in a 176-pin thin quad-flat-package (TQFP). Fig. 6 shows the micro-photograph of the fabricated chip. The proposed voltage-mode driver is used in the transmitter and occupies 85×60 μm^2.

R_A and R_B are determined to be 75 Ω and 150 Ω, respectively, for the 400-mV output voltage swing. R_A is composed of a 65-Ω non-salicided poly-resistor and the 10-Ω output resistance of the inverter. To achieve 33% de-emphasis, the driver for resistance R_A is divided into six parts; the five small drivers are operated as a main driver and the sixth driver is operated as an auxiliary driver. With a 1.2-V supply and those resistances, the proposed driver has the 400 mV and 266 mV output voltage swing for emphasis and de-emphasis, respectively, and draw 5.33 mA and 6.80 mA for each case. The current consumed by pre-drivers and dynamic charging current make the measured dissipated current be 8.0 mA.

Fig. 7 shows the transmission of a waveform consisting

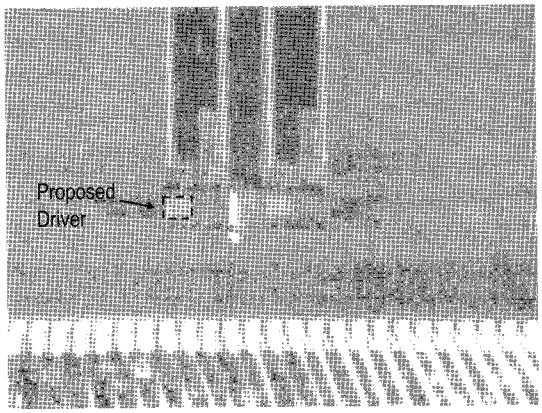


Fig. 6. Microphotograph of the fabricated chip.

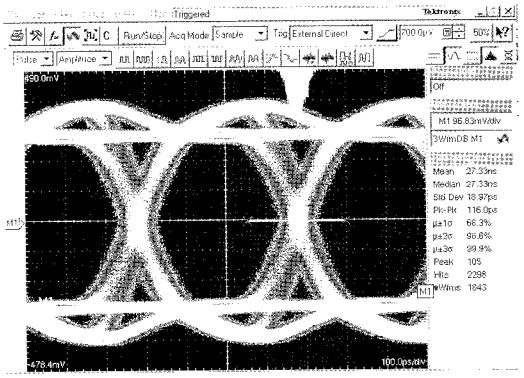


Fig. 7. Measured eye diagram of the proposed voltage-mode driver at 2.5 Gb/s.

of a 2^{10}-1 pseudorandom binary sequence (PRBS) at the rate of 2.5 Gb/s. The eye opening is slightly degraded owing to the jitter of the transmitter PLL.

V. CONCLUSIONS

We have briefly described a low-power technique for a voltage-mode driver. Inserting an additional current path in the source-side leads to reduce the output voltage swing and the current consumption. This simple technique requires neither another low-voltage supply nor a complicated regulator. Experimental results show that the proposed driver can be successfully operated at 2.5-Gb/s data communication systems. We expect that it will find applications in the content of multi-Gb/s communication specifications such as XAUI, SATA and PCI-Express.

ACKNOWLEDGMENTS

This work is supported by IC Design Center (IDEC) which provides EDA tools for research.

REFERENCES

[1] M.-J. E. Lee, W. J. Dally, and P. Chiang, "Low-power area-efficient high-speed I/O circuit techniques," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1591-1599, Nov. 2000.

[2] F. Yang, J. H. O'Neill, D. Inglis, and J. Othmer, "A CMOS low-power multiple 2.5-3.125-Gb/s serial link macrocell for high IO bandwidth network ICs", *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1813-1821, Dec. 2002.

[3] M. Green and U. Singh, "Design of CMOS CML circuits for high-speed broadband communications", IEEE International Symposium on Circuits and Systems, pp. 204-207, May 2003.

[4] J. Cao, M. Green, A. Momtaz, K. Vakilian, D. Chung, K. Jen, M. Caresosa, X. Wang, W.-G. Tan, Y. Cai, I. Fujimori, and A. Hairapetian, "OC-192 transmitter and receiver in standard 0.18-μm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1768-1780, Dec. 2002.

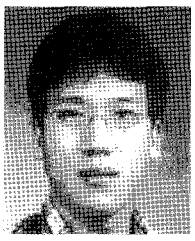
[5] S. Sidiropoulos and M. Horowitz, "A 700-Mb/s/pin CMOS signaling interface using current integrating receivers," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 681-690, May 1997.

[6] K.-L. J. Wong, H. Hatamkhani, M. Mansuri, and C.-K. K. Yang., "A 27-mW 3.6-Gb/s I/O transceiver," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 602-612, Apr. 2004.

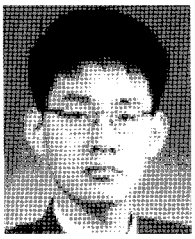
[7] J. Poulton, R. Palmer, A. M. Fuller, T. Greer, J. Eyles, W. J. Dally, and M. Horowitz, "A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2745-2757, Dec. 2007.

[8] W.-J. Choe, B.-J. Lee, J. Kim, D.-K. Jeong, and G. Kim, "A 3-mW, 270-Mbps, clock-edge modulated serial link for mobile displays," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 2012-2020, Sept. 2007.

[9] H. Lu, H. Wang, C. Su, and C.-N. J. Liu, "Design of an all-digital LVDS driver," *IEEE Transaction on Circuits and Systems I: Regular Papers*, to be published.



Heesoo Song received B.S. and M.S. degrees in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2002 and 2004, respectively, where he is currently working toward the Ph.D. degree. His research interests include high-speed I/O interface and low power CMOS circuit design.



Suhwan Kim received the B.S. and M.S. degrees in Electrical Engineering and Computer Science from Korea University, Seoul, Korea, in 1990 and 1992, respectively, and the Ph. D. degree in Electrical Engineering and Computer Science from the University of Michigan, Ann Arbor MI, in 2001. From 1993 to 1999, he was with LG Electronics, Seoul, Korea. From 2001 to 2004, he was a Research Staff Member in IBM T. J. Watson Research Center, Yorktown Heights NY. In 2004, Dr. Kim joined Seoul National University, Seoul, Korea, where he is currently an Assistant Professor of Electrical Engineering. His research interests encompass high-performance and low-power analog and mixed signal circuits, and driving methods and circuits for flat panel display.

Deog-Kyoon Jeong received the B.S. and M.S. degrees in Electronics Engineering from National University, Seoul, Korea, in 1981 and 1984, respectively, and the Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 1989. From 1989 to 1991, he was with Texas Instruments, Dallas, Texas, as a Member of the Technical Staff and worked on the modeling and design of BiCMOS gates and the single-chip implementation of the SPARC architecture. He joined the faculty of the Department of Electronics Engineering and Inter-University Semiconductor Research Center, Seoul National University, as an Assistant Professor in 1991. He is currently a Professor of the School of Electrical Engineering, Seoul National University. His main research interests include the design of high-speed I/O circuits, VLSI systems design, microprocessor architectures and memory systems.