Application of Area-Saving RF Test Structure on Mobility Extraction

Jaehong Lee, Junsoo Kim, Byung-Gook Park, Jong Duk Lee, and Hyungcheol Shin

Abstract—**An RF test structure is proposed and its applicability is confirmed by measuring DC characteristics and high frequency characteristics. Effective mobility extraction is also performed to confirm the validity of proposed test structure. The area of suggested test structure consumed on wafer was decreased by more than 50% and its characteristics do not be degraded compared with conventional structure.**

Index Terms—**MOSFET, RF, test structure**

I. Introduction

As the semiconductor technology node decreases, devices can be highly integrated. However the cost of fabrication also increases. Thus it has been an important issue to reduce the area consumption on the wafer. However, for RF device test, large area is needed to arrange the signal pads, thus conventional structure consumes large wafer area. Thus there have been some reports to reduce the chip area without any degradation in the device performance [1,2]. In this paper, we reduced chip area by changing device layout. When extracting some parameters (such as carrier mobility, velocity and so on) as well as the DC and the RF characteristics, our work enables to reduce the area consumption to 40% compared with the conventional test structure.

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Inter-University Semiconductor Research Center (ISRC), and School of Electrical Engineering, Seoul National University, San 56-1, Shinlim-dong, Kwanak-gu, Seoul, 151-742, Korea
E-mail : jaehong2@snu.ac.kr

II. Test Structure

In this work, we designed RF test structure to reduce the area on the wafer. As shown in Fig. 1. (a), conventional RF test structure which has two signalport – source and body are connected to ground – occupies over 0.06 mm^2 per one device. To measure this structure, two Ground-Signal-Ground (GSG) probes are needed. A

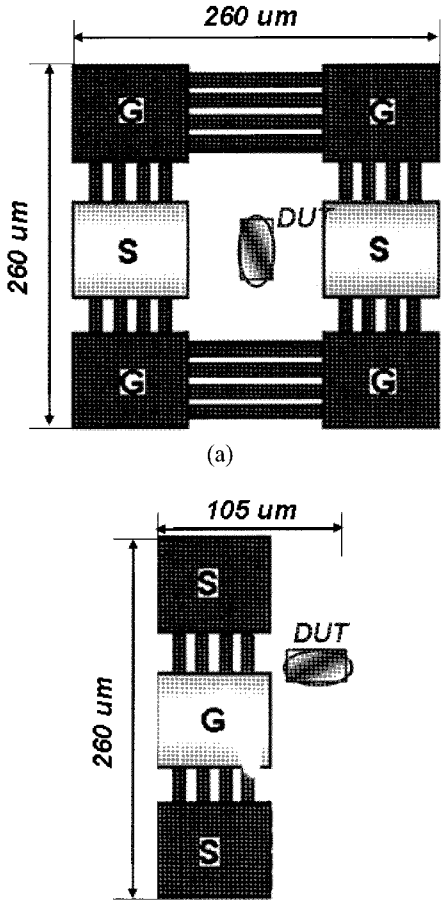

Fig. 1. Schematic diagrams of RF CMOS devices with (a) GSG pads and (b) SGS pad.

new RF test structure proposed in this work (Fig. 1. (b)) consumes less than 0.03 mm^2 and needs only one Signal-Ground-Signal (SGS) probe.

III. Results and Discussion

The proposed structure has an advantage in consuming wafer area by only 46%. However, to confirm reliability of measured data, comparison procedures with conventional RF test structure are essential. At first, we observed DC characteristics. In Fig. 2, DC characteristics of the NMOS device are present. Device under test (DUT) has a 60 nm gate length, 0.8 μm of unit finger width, and 32 fingers. Devices in the GSG pattern and the SGS pattern show almost same DC I-V characteristics. S-parameter measurement can be also performed with these structures. Because of the parasitic components caused by pads interconnection lines, proper de-embedding procedure of parasitic elements is essential. In this paper, measurements are performed up to 10 GHz, OS (open-short) de-embedding method can guarantee de-embedding accuracy. The procedure of de-embedding is as follows [3].

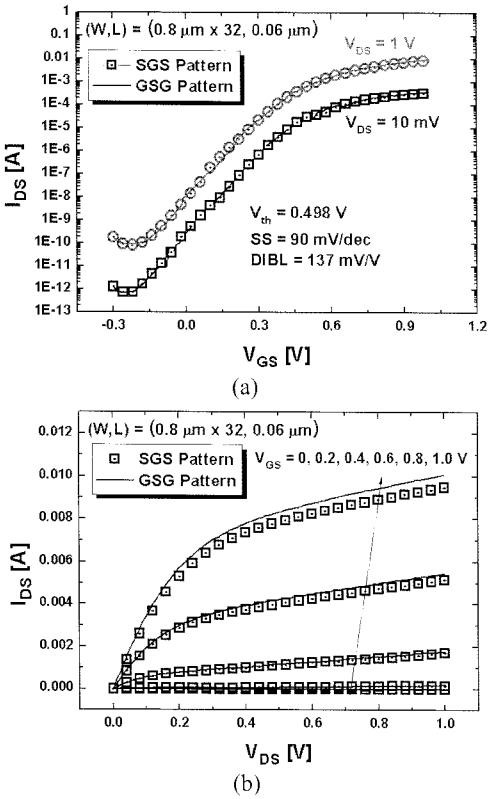

Fig. 2. Comparison of DC characteristics between GSG and SGS patterned structures. (a) Id-Vg characteristics at Vd = 0.01 V and 1.0 V and (b) Id-Vd output characteristic.

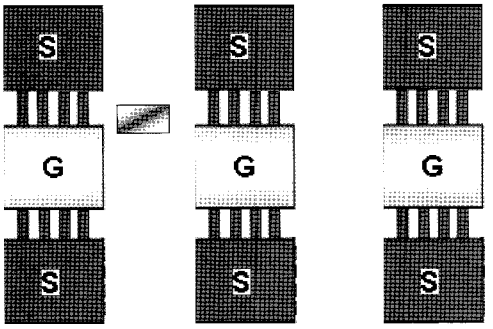

Fig. 3. Schematic diagrams of the test structure used in de-embedding procedure of (a) DUT (b) Open and (c) Short.

$$Y_{\text{int}} = \left(\left(Y_{dut} - Y_{open}\right)^{-1} - \left(Y_{short} - Y_{open}\right)^{-1}\right)^{-1}$$

And the schematic diagrams of the structures are shown in Fig. 3.

As shown in Fig. 4, measured data from both structures show almost same high frequency characteristics. In general, 60 nm MOS device operates for above 10 GHz frequencies. However, in this work, it is focused on the application of RF test structure such as extracting carrier mobility, velocity and so on. Thus the data up to 10 GHz is enough because the channel inversion charge can be obtained by RF C-V method, and the capacitance can be extracted from the low frequency region [4]. Furthermore, SGS probe tip cannot be guaranteed the accuracy of measurement in high frequency region above 15 GHz. Because it has just one ground line in probe tip, the fringing field originated from signal line cannot be shielded. Therefore this effect can be a problem at high frequency region above 15 GHz. For high frequency application over 15 GHz, it would be better using GSGSG than SGS pattern. However, GSGSG pattern consumes more area than SGS pattern. Fig. 5 shows gate-to-all capacitance of the device. Gate-to-all capacitance is obtained from measured Y-parameters [4]. In order to extract effective mobility of electrons, total inversion charge in the channel should be known and it can be obtained by integrating gate-to-channel capacitance [4]. Extracted C_{gdi} and total inversion charge are shown in Fig. 6 and 7. In these figures, we can see that extracted parameters from SGS patterned structure are almost the same with those from conventional structure.

In Fig. 8, electron effective mobility is presented [5]. As shown in the figure, mobility can be extracted from our structure and the differences with that from

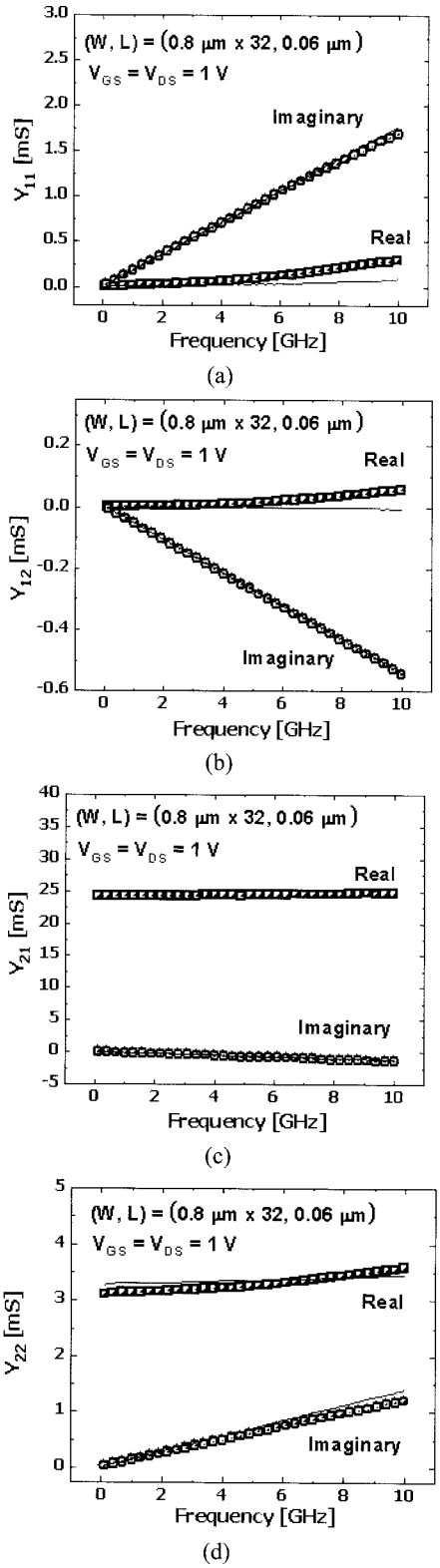

Fig. 4. Comparison of high frequency characteristics between GSG and SGS patterned test structures. Real and imaginary part of (a) Y_{11} (b) Y_{12} (c) Y_{21} and (d) Y_{22}.

conventional structure are only less than 10%. Though our structure consumes only 40% of area compared with

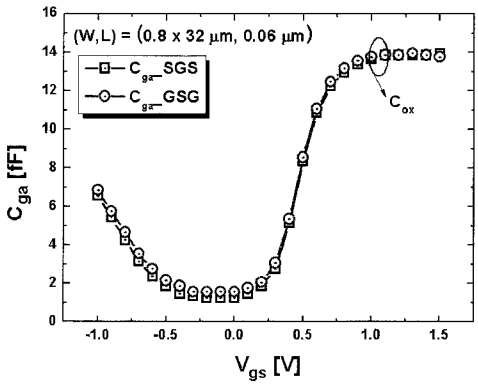

Fig. 5. Gate-to-all capacitances of DUTs from measured Y-parameters of GSG and SGS patterned structures.

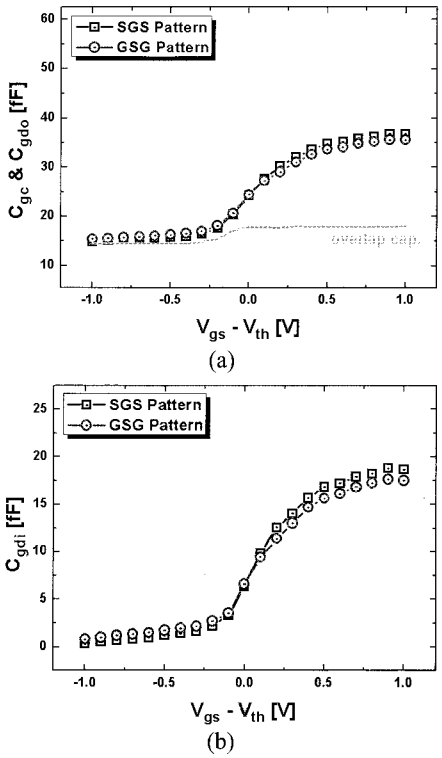

Fig. 6. Extracted gate capacitances. (a) Gate-to-channel capacitance and gate-to-drain overlap capacitances. (b) Intrinsic gate-to-drain capacitance.

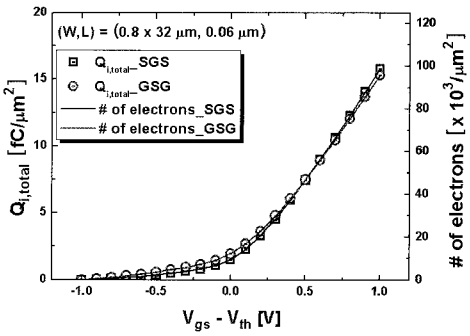

Fig. 7. Comparison of total inversion charge and number of electrons in channel between GSG and SGS patterned structures.

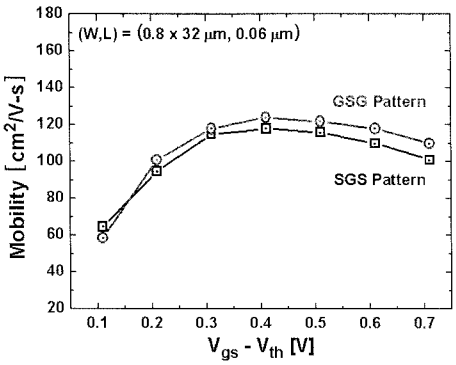

Fig. 8. Extracted effective mobility of electrons in GSG and SGS patterned structures.

conventional structure, but shows almost same performances.

IV. Conclusions

In this paper, we proposed new layout of RF CMOS devices which saves wafer area more than half of conventional RF CMOS devices. DC and RF characteristics were compared with the conventional structure, and it was proved that the proposed structure has no degradation in performance. Moreover, this test structure can be applied to extract effective mobility of electron and predict effective carrier velocity [6].

Acknowledgments

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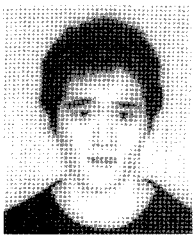
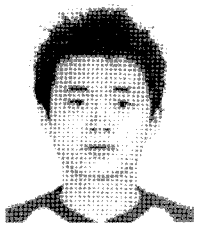
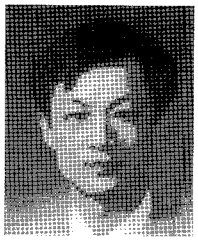


Jaehong Lee was born in Korea on October 25, 1983. He received B.S. degree in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2006, where he is currently working toward the Ph.D. degree. His major interest is deep submicrometer device modeling and characterization issues.

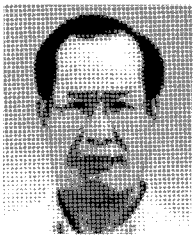


Junsoo Kim was born in Korea on July 13, 1980. He received B.S. degree in electronic engineering from Kyunghee University, Gyunggi-do, Korea, in 2003. He is currently pursuing the Ph.D. degree in Seoul National University, Seoul, Korea. His major interest is deep submicrometer device modeling and characterization issues.



Byung-Gook Park received his B.S. and M.S. degrees in Electronics Engineering from Seoul National University (SNU) in 1982 and 1984, respectively, and his Ph. D. degree in Electrical Engineering from Stanford University in 1990. From 1990 to 1993, he worked at the AT&T Bell Laboratories, where he contributed to the development of 0.1 micron CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25 micron CMOS. In 1994, he joined SNU as an assistant professor in the School of Electrical Engineering (SoEE), where he is currently a professor. In 2002, he worked at Stanford University as a visiting professor, on his sabbatical leave from SNU. He has been leading the Inter-university Semiconductor Research Center (ISRC) at SNU as the director from June 2008.

His current research interests include the design and fabrication of nanoscale CMOS, flash memories, silicon quantum devices and organic thin film transistors. He has authored and co-authored over 580 research papers in journals and conferences, and currently holds 34 Korean and 7 U.S. patents. He has served as a committee member on several international conferences, including Microprocesses and Nanotechnology, IEEE International Electron Devices Meeting, International Conference on Solid State Devices and Materials, and IEEE Silicon Nanoelectronics Workshop (technical program chair in 2005, general chair in 2007). He is currently serving as an executive director of Institute of Electronics Engineers of Korea (IEEK) and the board member of IEEE Seoul Section. He received "Best Teacher" Award from SoEE in 1997, Doyeon Award for Creative Research from ISRC in 2003, Haedong Paper Award from IEEK in 2005, and Educational Award from College of Engineering, SNU, in 2006.



Jong Duk Lee was born in Youngchun, Kyungpook, Korea. He received the B.S. degree in physics from Seoul National University in 1966. He received the Ph.D. degree from the Department of Physics at the University of North Carolina at Chapel Hill in 1975. He served at the Military Communication School as a ROTC officer from 1966 to 1968. He then worked at the Engineering College of Seoul National University as a teaching assistant in the Department of Applied Physics until 1970. He was an Assistant Professor in the Department of Electronics Engineering at Kyungpook National University from 1975 to 1978. In 1978, he studied microelectric technology in HP-ICL at Palo Alto, CA, USA, and soon afterward worked for the Korea Institute of Electronic Technology (KIET) as the director of the semiconductor division. He established the KIET Kumi Facility and introduced the first poly-silicon gate technology in Korea by developing 4K SRAM, 32K and 64K Mask ROM's, and one-chip 8-bit micro-computer.

In July 1983, he moved to the Department of Electronics Engineering of Seoul National University, which has been merged to School of Electrical Engineering in 1992, where he is now a Professor. He started to establish the Inter-University Semiconductor Research Center (ISRC) in 1985, and served as the director from 1987 to 1989. He served as the chairman of the Electronics Engineering Department from 1994 to 1996. He worked for Samsung SDI Co., Ltd. as the Head of Display R&D Center for a year on the leave of SNU in 1996. He was the member of the steering committee for IVMC(International Vacuum Microelectronics Conference) from 1997-2001 and KCS (Korean Conference on Semiconductors) from 1998-2008. He was the conference chairman of IVMC'97 and KCS'98 who led the IVMC'97 and the KCS'98 successfully. He was also the member of IEDM(International Electron Devices Meeting) Subcommittee on Detectors, Sensors and Displays operated by IEEE Electron Devices Society from 1998 to 1999, he has been elected to the first president of the Korean Information Display Society in June 1999 to serve until Dec.31,2001. He concentrated his study on the image sensors such as Vidicon type, MOS type, and also CCD to help Samsung SDI Co. and Samsung Electronics Co. since 1985. His current research

interests include sub 0.1 um CMOS structure and technology, CMOS image sensors and FED(Field Emission Display), and organic LEDs and TFTs. He published more than 221 papers in the journals such as IEEE-ED and EDL, Journal of Vacuum Science and Technology, Applied Physics and Journal of Electrochemical Society, including 160 SCI journal papers. He presented more than 361 papers including 213 international conference papers. He also registered 12 US, 4 Japanese, and 28 Korean patents. Now he is a member of IEEE, ECS, AVS, SID, KPS, KVS, IEEK, and KSS.

Hyungcheol Shin received the B.S. (*magna cum laude*) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1993. From 1994 to 1996, he was a Senior Device Engineer with Motorola Advanced Custom Technologies. In 1996, he was with the Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology (KAIST), Daejeon. During his sabbatical leave from 2001 to 2002, he was a Staff Scientist with Berkana Wireless, Inc., San Jose, CA, where he was in charge of CMOS RF modeling. Since 2003, he has been with the School of Electrical Engineering and Computer Science, Seoul National University. He has published over 300 technical papers in international journals and conference proceedings. He also wrote a chapter in a Japanese book on plasma charging damage and semiconductor device physics.

His current research interests include Nano CMOS, Flash Memory, DRAM cell transistors, CMOS RF, and noise. Prof. Shin was a committee member of the International Electron Devices Meeting. He also has served as a committee member of several international conferences, including the International Workshop on Compact Modeling, and as a committee member of the IEEE EDS Graduate Student Fellowship. He is a Lifetime Member of the Institute of Electronics Engineers of Korea (IEEK). He received the Second Best Paper Award from the American Vacuum Society in 1991, the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences, KAIST, in 1998, The Haedong Paper Award from IEEK in 1999, and the Excellent Teaching Award from Seoul National University in 2005 and 2007. He is listed in *Who's Who in the World.*