Full CMOS Single Supply PLC SoC ASIC with Integrated Analog Front-End

Chul Nam, Young-Gun Pu, Sang-Woo Kim, and Kang-Yoon Lee

Abstract—**This paper presents a single supply PLC SoC ASIC with a built-in analog Front-end circuit. To achieve the low power consumption along with low cost, this PLC SoC employs fully CMOS Analog Front End (AFE) and several LDO regulators (LDOs) to provide the internal power for Logic Core, DAC and Input/output Pad driver. The receiver part of the AFE consists of Pre-amplifier, Gain Amplifier and 1 bit Comparator. The transmitter part of the AFE consists of 10 bit Digital Analog Converter and Line Driver. This SoC is implemented with 0.18 μm 1 Poly 5 Metal CMOS Process. The single supply voltage is 3.3 V and the internal powers are provided using LDOs. The total power consumption is below 30 mA at stand-by mode to meet the Eco-Design requirement. The die size is 3.2 x 2.8 mm^2.**

Index Terms—**Power line communication, PLC, full-CMOS, analog front end (AFE), LDO regulator, eco design**

I. INTRODUCTION

Power line communication (PLC) presents a "No New wires" solution with the additional advantages of ubiquitous node availability, easy installation and above all, cost effectiveness. In PLC networks, alternating current (ac) power lines are used as a medium to send and receive discrete frequency-based control, monitoring and communication messages to run smart home services, exchange data and share high-speed internet access among multiple PCs and other services.

However, it is a fact that In-home low voltage power lines were not designed and never meant for data communication. With the recent advancement in the fields of very large scale integration (VLSI) and digital signal processing (DSP), the "Smart Home" dream has come true and the idea of establishing a PLC based home network has become a reality. Once a high speed power-line based home network is established, it becomes practical to control the entire home environment, even remotely establish its security, conserve energy, and convert it into really comfortable living [1].

The physical topology and properties of the home wiring, the appliances connected and the behavioral characteristics of the electric current itself all combine to pose numerous technological hurdles in the use of the power line as a networking medium.

For efficient and reliable communication over power lines, a robust physical (PHY) layer is required, which has clear and strong specifications for its source and channel coding, modulation and multiplexing techniques. Since CENELEC B band of 95~148.5 kHz causes relatively large noise interferences on the other frequency band in low band PLC [2], ZBUS power line Protocol [3] is preferred to use in this environment using a Chirp modulation [4]. ZBUS power line communication protocol is composed of 4 layers such as PHY, MAC, NETWORK and APP compared to Open System Interconnection (OSI) standardization.

Currently, the PLC modem ASIC in medium or high speed PLC is implemented by two chip solutions such as MAC and AFE [5]. The conventional AFE on printed circuit-board (PCB) [6] in low speed is still used in some applications. Both low and medium or high speed PLC modem is required to be one chip to save space and cost.

Manuscript received Jun. 2, 2009; revised Jun. 12, 2009.
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In this paper the low speed PLC SoC is presented with full CMOS AFE incorporated adopting the ZBUS power line protocol which has a carrier frequency of 95~125 kHz, a chirp modulation and data speed up to 1.2~7.2 kbps. By virtue of several internal LDO regulators, this SoC is capable of operating the 3.3 V single power supply in 0.18 um process. It also makes possible to meet the Eco Design requirement that the standby power consumption should be less 1 W.

II. PLC SoC Architecture

Fig. 1 shows the architecture of PLC SoC ASIC which consists of Logic Core in blue line, Analog Front End (AFE) in black dot line and Power Management block in red line.

The logic core block consists of 32bit CPU(EISC^{TM}) [7], Pin Multiplexer, Reset/Clock Controller, 3 Channel Timer, 2 Channel UART, TWI, GPIO, Interrupt Controller, WDT, I2S with ADPCM, SPI-Flash Controller, Memory Controller, 4KB SRAM, SPI and MODEM (including ECC, SYNC, MAC, and Modulator / Demodulator). The AFE includes Pre-Amplifier, Gain Amplifier, 1 bit ADC (Comparator) and 10 bit DAC. The power management is composed of Brown-out detector (BOD) and Low dropout regulator (LDO) for 3.3 V single power supply for the SoC. In particular, the 64 KB Flash memory is stacked on the SoC to use the program memory and register memory.

The input signal from the PLC line is interfaced with the AFE receiver through pre-filter and transformer and the output signal with 10 bit DAC through the Line driver by TDD (Time Division Duplex) method at the same time.

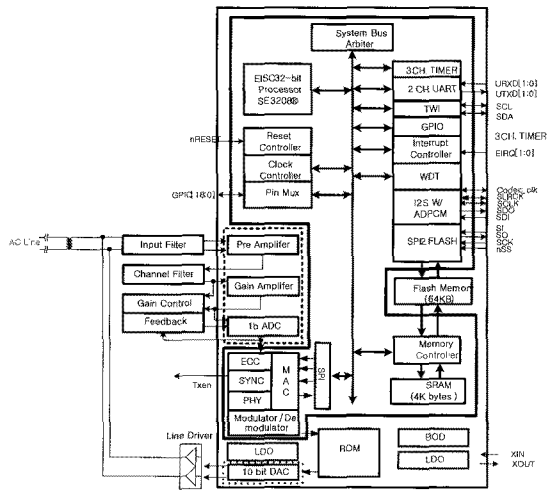

Fig. 1. The architecture of PLC SoC ASIC.

III. Building Blocks

1. Receiver

The receiving part consists of pre-amplifier, Gain amplifier and comparator (1 bit ADC). High voltage DC component in receiving signal is isolated by the transformer and high frequency component is removed by the pre-filter shown in Fig. 2.

The pre-amplifier is designed to accommodate the rail-to-rail input common mode voltage ranging from 0.1 V to 3.0 V by using complementary folded cascode structure as shown in Fig. 3 [8]. In order to gain the low input referred noise level about 10 $nV/\sqrt{Hz}$, the gain of the pre-amplifier is set 2~3.

The channel filter following the pre-amplifier as shown on Fig. 4 is a kind of band-pass filter using series

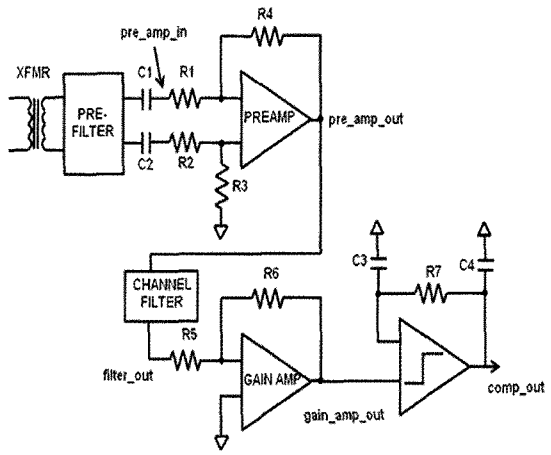

Fig. 2. Receiver.

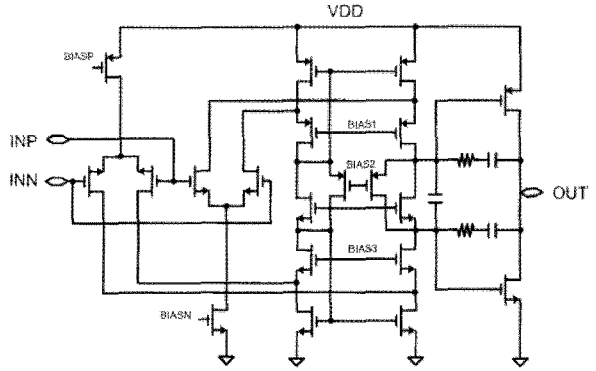

Fig. 3. Folded cascode Amplifier.

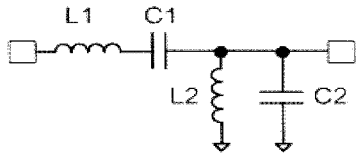

Fig. 4. Band-pass channel filter.

and parallel resonator with bandwidth of 46 kHz and center frequency of 107 kHz.

The high frequency noise component outside the bandwidth is remarkably removed in this BPF as shown in Fig. 5.

In a low speed PLC, the comparator can be a kind of data converter. The comparator acts as 1 bit ADC having 1.5 mV input referred hysteresis.

The output of comparator is converted into the digital data to be processed in logic block.

Fig. 6 shows input and output signal of each block at receiver.

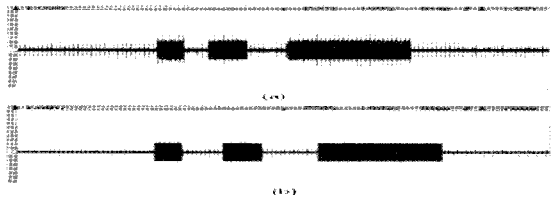

Fig. 5. (a) Receiving signal (b) channel filter output.

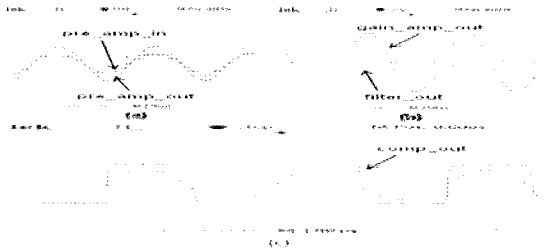

Fig. 6. (a) Pre-amplifier (b) gain amplifier (c) comparator input and output signal.

2. Transmitter

In transmitter, the 10 bits current steering DAC [9] is only part which is interfaced with the line driver as shown in Fig. 7. The DAC has current steering partially segmented 5+5 architecture. The full scale current (I_{OFS}) is up to 8.75 mA. The simulation result of INL and DNL shows in Fig 8.

The differential output is preferred to remove the common mode noise and reduce the mismatch between power lines.

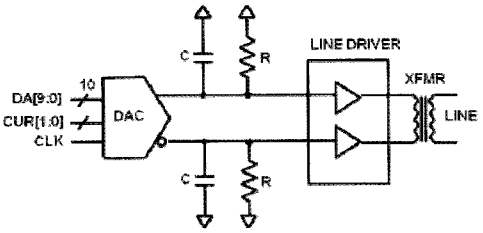

Fig. 7. Transmitter.

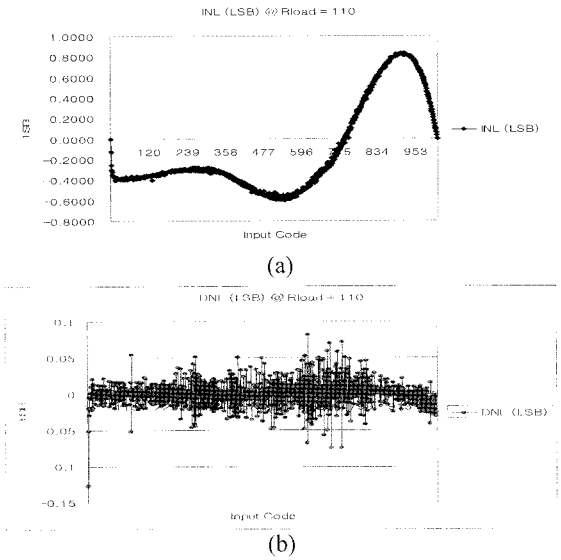

Fig. 8. (a) INL (b) DNL of 10bit DAC.

The line driver outside can supply up to 1 A to the load line which equivalent impedance is several ohms. The performance of Receiver and transmitter is summarized in Table 1.

Table 1.

Part	Block	Parameter	Result
Rx	Pre-amplifier	Av	60 dB
		CMR	0.3-3 V
		ηi	10 $nV/\sqrt{Hz}$
		CMRR	100 dB
		PSRR	75 dB
	Gain-Amplifier	Av	60 dB
		V_{IOS}	15 mV
	Comparator	V_{HYS}	1.5 mV
		tpd	28 nsec
Tx	DAC	Resolution	10 bit
		ENOB	9 bit
		I_{OFS}	8.75 mA
		INL	1 LSB
		DNL	1 LSB

Note) ηi: Input referred noise, V_{IOS} : Input offset voltage ,V_{HYS}: Input referred hysteresis, tpd: propagation delay

3. Power Management

In order to operate under the single 3.3 V supply voltage, the SoC employs the independent 1.8 V LDO regulators [10] for the logic core, 10 bit DAC and crystal oscillator, respectively. Fig. 9 shows the power plan based on each regulator. The crystal oscillator uses the dedicated regulator to minimize the noise injection into power and ground lines. 10 bits DAC is designed with 1.8 V devices instead of 3.3 V devices so as to minimize the size and power consumption which is also required for 1.8 V regulator.

A 100 mA regulator is dedicated into the core logic block. The wide metal power ring is also routed around the core logic to reduce the IR drop. The driving capability of each LDO is summarized in Table 2.

The regulator is a kind of linear regulator using the Bandgap Reference (BGR) Circuit as the reference voltage in Fig. 10. The output voltage is determined simply as equation (1).

$$v_{out} = v_{bg} \cdot (1 + \frac{R_1}{R_2}) \tag{1}$$

,where vbg is the Bandgap reference voltage, that is 1.2 V.

In regulator, the external capacitor (C_{EXT}) is connected

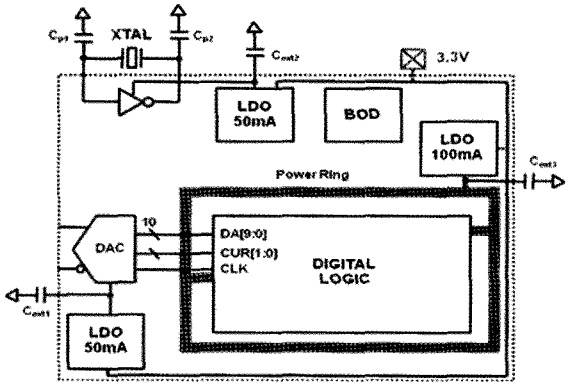

Fig. 9. Power Plan.

Table 2.

Supply Voltage		3.3 V
Drive Capability	Core Logic	100 mA
	DAC	50 mA
	Crystal Oscillator	50 mA

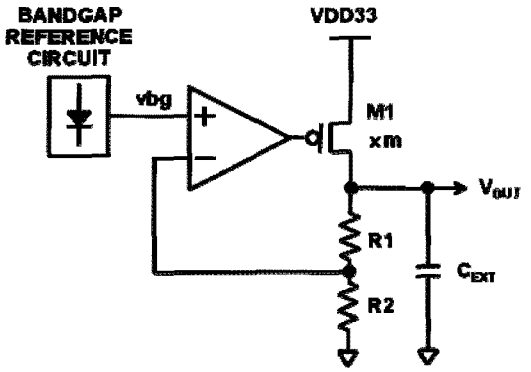

Fig. 10. LDO Regulator.

to guarantee the phase margin for the stability of regulator.

Brown-out detector (BOD) is designed to prevent the ASIC from malfunctioning due to the unstable power supply. As shown in Fig. 11 (a), as the power supply (VDD33) goes down and then V1 goes down and reach to the reference voltage, vbg, BOUT goes low to make that the CPU uses the reset signal.

Normally, V1 is a division voltage of resistors, R1, R2 and R3 if Ron of MP is quite small compared with these resistors. That is

$$V1 = \frac{R2 + R3}{R1 + R2 + R3} \cdot VDD33 \tag{2}$$

The trigger voltage, Vtr at which BOUT goes low is determined by reference voltage, vbg

$$\frac{R2 + R3}{R1 + R2 + R3} \cdot Vtr = Vbg \tag{3}$$

By substituting equation (2) into equation (3),

$$Vtr = Vbg \cdot \frac{R1 + R2 + R3}{R2 + R3} = Vbg \cdot \frac{VDD33}{V1} \tag{4}$$

Now that VDD33 and V1 are known, Vtr is calculated by equation (4). BOUT is triggered into low state at 2.7. Fig. 11 (b) shows the simulation result.

IV. Exprimental Results

This SoC ASIC was implemented by 0.18 μm 1 poly 5 Metal CMOS process. The chip area is 3200 x 2800 μm^2. AFE, 3 LDOs and 10 bit DAC are located on the left side

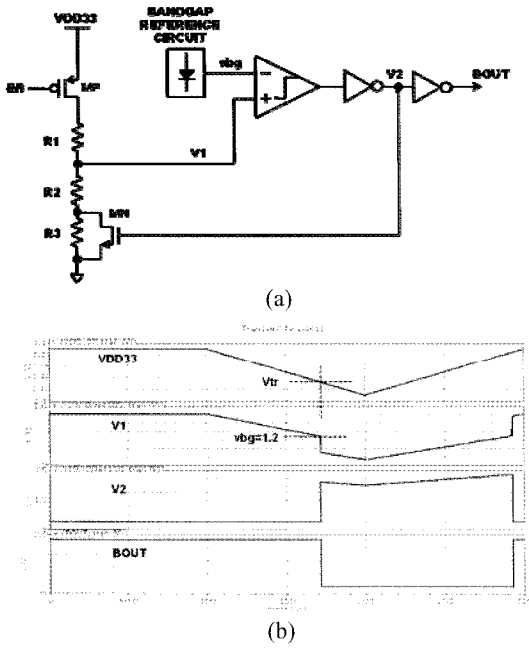

Fig. 11. (a) Block diagram (b) Simulation Result of the Brown-Out Detector (BOD).

in chip microphotograph as shown in Fig. 12.

Fig. 13 shows PLC communication signal on power line. Table 3 summarizes the performance of chip.

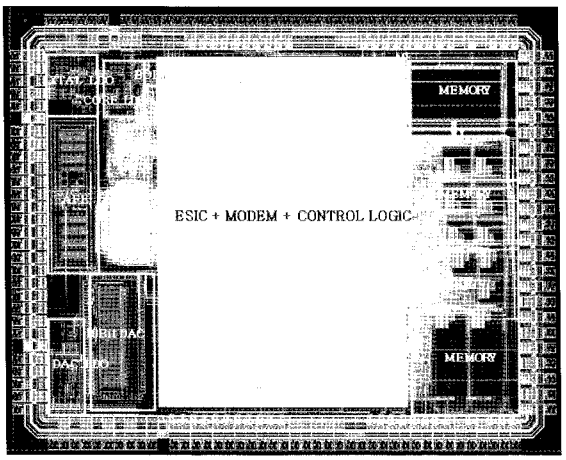

Fig. 12. Chip Microphotograph.

Table 3.

Supply Voltage		3.3 V
PLC SoC	Power Consumption @standby	<30 mA
LDO	Drive Capability	50~100 mA
	Total static power	<100 uA
AFE	Power Consumption	10 mA
	RX gain Range	<60 dB
	RX Power consumption	5 mA
	TX(DAC)power consumption	5 mA

V. CONCLUSIONS

This paper presents the 3.3 V single power supply PLC SoC with a built-in CMOS analog Front End (AFE) suitable for the low speed PLC Communication.

Both internal LDO and CMOS AFE enable the SoC to increase the power efficiency and low power implementation. Particularly, the stand-by power consumption under 0.1 W meets the Eco design requirement [11] by reducing half of the discrete design.

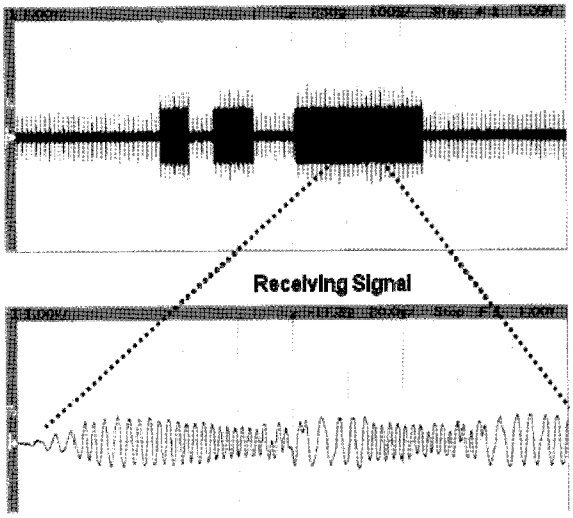

Fig. 13. Receiving waveform on the power line.

ACKNOWLEDGMENTS

This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD, Basic Research Promotion Fund) (KRF-2006-331-D00409).

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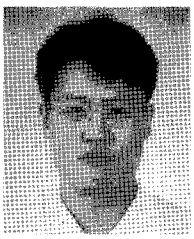

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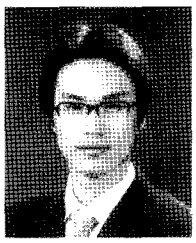

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