# A Study on the Electrical Properties of Al<sub>2</sub>O<sub>3</sub>/La<sub>2</sub>O<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub> Multi-Stacked Films Using Tunnel Oxide Annealed at Various Temperatures

#### Hyo June Kim, Seung Yong Cha, and Doo Jin Choi<sup>†</sup>

Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea (Received June 15, 2009; Accepted July 16, 2009)

#### ABSTRACT

The structural and electrical properties of  $Al_2O_3/Al_2O_3/Al_2O_3$  (ALA) films using a tunnel oxide annealed at various temperatures were investigated. The program/erase properties of the ALA films using the tunnel oxide annealed at 600°C were superior to others. The program/erase voltage and time of the ALA films using the tunnel oxide annealed at 600°C were 11 V for 10 ms (program) and -11 V for 100 ms (erase), respectively, and the corresponding memory window was about 1.59 V. In the retention test, the  $V_{th}$  distributions of all films were not changed up to about  $10^4$  cycles. In this study, all data showed sufficient characteristics to be used in flash memory devices.

Key words: SONOS, Memory window, Flash, High-k dielectrics, La,O3

## 1. Introduction

lash memory was first developed by Dr. Masuoka Fusio at Toshiba in 1984,10 and was announced at the 1984 IEEE International Electron Devices Meeting (IEDM). Subsequently, flash memory technology has continuously evolved and advanced. Flash memory can be divided into two categories based on the general operating principle of the device,2) i.e., NOR and NAND type flash memories. Since the NAND flash memory has superior program/erase time, endurance and integration compared with NOR flash memory, the NAND type is widely used in large capacity storage devices such as personal computer cards, and various memory cards.<sup>3)</sup> However, current NAND flash memory uses a floating gate for charge storage, which has some drawbacks including a threshold voltage  $(V_{th})$  shift and a wide distribution of  $V_{th}$ . Moreover, stress-induced leakage current (SILC) causes problems in scaling down NAND flash memory. 41 Hence, a floating gate can no longer be used for charge storage in non-volatile flash memory.

In order to solve these problems, the layer type multistacked film structure was proposed,<sup>5)</sup> which is often referred to as SONOS or MONOS (silicon/metal-oxide-nitride-oxidesilicon).<sup>6-8)</sup> However, this structure is also faced with a scaledown limitation in terms of thickness reduction.<sup>9)</sup> In particular, the tunnel oxide (bottom oxide) problem is quite serious. As thickness of the tunneling oxide decreases, program/ erase time becomes shorter while the program/erase voltage also is reduced and retention in the device is thereby deteri-

<sup>†</sup>Corresponding author : Doo Jin Choi E-mail : drchoidj@yonsei.ac.kr

Tel: +82-2-2123-2852 Fax: +82-2-365-5882

orated. One potential way of dealing with this problem is to change the material associated with the tunnel oxide from, SiO<sub>2</sub> to a more suitable material.

In this study, 5 nm  ${\rm Al_2O_3}$  annealed at various annealing temperatures was used as a tunnel oxide. A 5 nm  ${\rm La_2O_3}$  layer deposited on the tunnel oxide was used as trap layer, while a 15 nm  ${\rm Al_2O_3}$  layer deposited on the trap layer was used as a blocking oxide. The electrical properties of these  $({\rm Al_2O_3/La_2O_3/Al_2O_3})$  structures were investigated for various tunnel oxide annealing conditions.

## 2. Experimental procedure

The Al<sub>2</sub>O<sub>3</sub>/La<sub>2</sub>O<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub> (ALA) films shown in Fig. 1 were deposited on (100) n-type Si wafers (SILTRON, Korea) using a metal organic chemical vapor deposition (MOCVD) system. Annealing temperatures of the tunnel oxide were 600, 750 and 900°C, and these were achieved using a rapid thermal process (RTP, ULVAC MILA 3000) for 90 sec under N<sub>2</sub>. After annealing, the thickness of the tunnel oxide was 5 nm. La(tmhd)<sub>3</sub> tetraglyme adduct [Tris(2,2,6,6-tetramethyl-3,5heptanedionato) lanthanum (III) tetraglyme adduct, La(C<sub>11</sub>H<sub>19</sub>O<sub>2</sub>)<sub>3</sub>·CH<sub>3</sub>(OCH<sub>2</sub>CH<sub>2</sub>)<sub>4</sub>OCH<sub>3</sub>, Strem Chemical Inc., USA] and Al-acetylacetonate [Al(CH<sub>3</sub>COCH)<sub>3</sub>, Strem Chemical, Inc., USA] were used as precursors for the La and Al metal, respectively. No was used as a carrier gas for the La and Al precursors. Prior to deposition, the wafers were cleaned with organic solvents. They were then treated with a 10% hydrofluoric (HF) solution to remove the native oxide layer.

The substrate temperature was maintained at  $350^{\circ}$ C during deposition for all films, and the working pressure was maintained at 5 torr (266.6 Pa). Film thickness was measured by an ellipsometer (Gartner, L117,  $\lambda = 632.8$  nm). To measure the electrical properties of the ALA films, (metal-

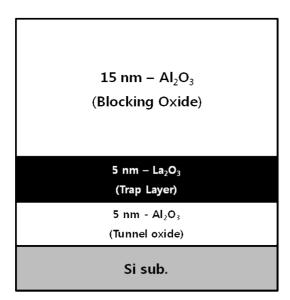


Fig. 1. A schematic diagram of the ALA multi-layered structure deposited on the Si substrate.

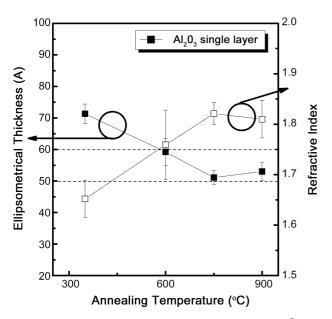
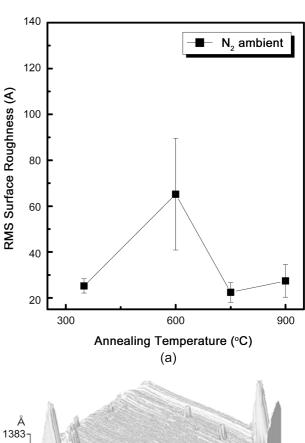


Fig. 2. The thicknesses and refractive index of the  ${\rm Al_2O_3}$  tunnel oxide on the various annealing temperatures.

blocking oxide - trap layer - tunnel oxide – semiconductor) capacitors (i.e.,  $Pt/Al_2O_3/La_2O_3/Al_2O_3/Si)$  were fabricated. The Pt electrode was fabricated using magnetron sputtering with shadow masks with a capacitor area of  $9.25\times10^{-4}\,\mathrm{cm}^2$  for all specimens. A C-V analysis was performed using a Keithley 590 C-V analyzer at 1MHz in order to investigate memory window and the optimized program voltage.

## 3. Results and Discussion

Fig. 2 shows the thicknesses measured by ellipsometry and the refractive index of the  $Al_2O_3$  tunnel oxide for the various annealing temperatures. At the as-deposited temperature (350°C), the tunnel oxide thickness was about 7.13



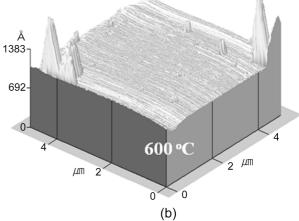


Fig. 3. (a) RMS surface roughness of the  $Al_2O_3$  films and (b) AFM image of the  $Al_2O_3$  film annealed at  $600^{\circ}$ C.

nm, while thicknesses for the 600, 750 and 900°C annealed samples were about 5.92 nm, 5.11 nm and 5.3 nm, respectively. Thus, after the annealing process, the film thicknesses were very similar. However, the films annealed at 750°C and 900°C were more densified than at 600°C. In our previous  $\rm La_2O_3$  study, TEM images indicated that the interfacial layer ( $\rm La_xSi_yO_z$ ) grew during the 900°C annealing process due to oxygen incorporation.  $^{10}$  Hence, we believed that film thickness generally increases during a high temperature annealing process, however, the thickness of annealed  $\rm Al_2O_3$  films actually decreased.

It was thought that the short range order of the  $Al_2O_3$  was smaller than that of  $La_2O_3$  film and the density of the  $Al_2O_3$  was higher than that of the  $La_2O_3$  due to their atomic size. Hence, during the high temperature annealing process,

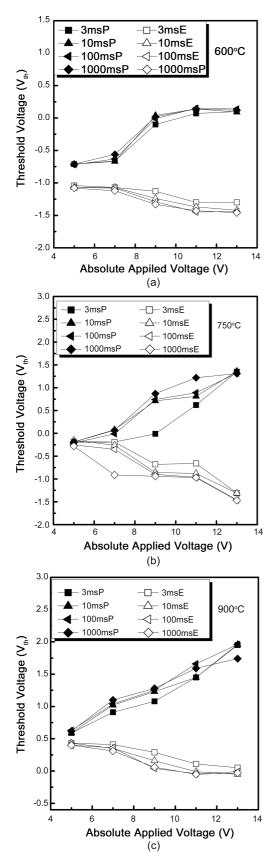


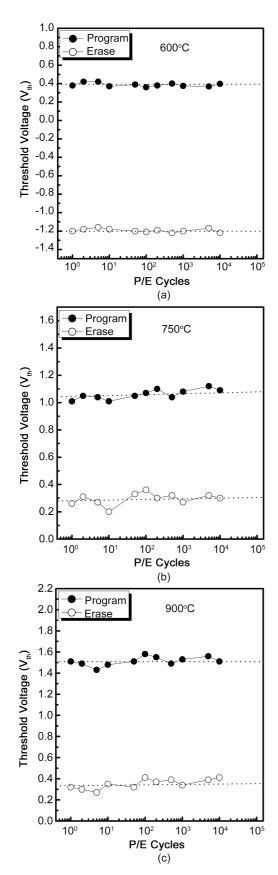
Fig. 4. Threshold voltages  $(V_{th})$  of the ALA films using the tunnel oxide annealed at (a)  $600^{\circ}$ C, (b)  $750^{\circ}$ C, and (c)  $900^{\circ}$ C for the various program/erase voltages and times.

residual oxygen could not as easily penetrate through and react with the  ${\rm Al_2O_3}$  film as it could the  ${\rm La_2O_3}$  film. This was confirmed by monitoring the refractive index of the  ${\rm Al_2O_3}$  (Fig. 2). As the annealing temperature increased, refractive index of the  ${\rm Al_2O_3}$  increased, though the values at 900°C and 750°C are the same within experimental error.

Fig. 3 shows (a) the RMS surface roughness of the  ${\rm Al_2O_3}$  films and (b) an AFM image of the  ${\rm Al_2O_3}$  film annealed at 600°C. The RMS surface roughness values of the all films except for the film annealed at 600°C were about 2.5 nm. In the case of the 600°C annealed film, the RMS surface roughness value was about 6.5 nm, and hillock formation was observed because 600°C is not a sufficient temperature to allow for atomic diffusion during annealing. However, the hillocks disappeared for annealing at 750°C and 900°C due to atomic and surface diffusion. In general, high surface roughness causes an unstable interface with many surface defects; charges thereby may easily be captured or trapped on at these defects. Hence, we believed charge trapping properties would superior for the 600°C annealing.

Fig. 4 shows threshold voltages (V<sub>th</sub>) of the ALA films using the tunnel oxide annealed at the (a) 600°C, (b) 750°C and (c) 900°C for various program/erase voltages and times. We already reported similar results for ALA film using the as-deposited tunnel oxide (i.e., 350°C), 12 i.e., 11 V for 10 ms for programming and  $-11\,\mathrm{V}$  for  $100\,\mathrm{ms}$  for erasing with a memory window of about 1.12 V. In this study, the electrical properties of the ALA films using the tunnel oxide annealed at 600°C were 11 V for 10 ms for programming and -11 V for 100 ms for erasing, and the memory window was about 1.59 V. On the other hand, 13 V for 1000 ms (programming) and -13 V for 1000 ms (erasing) were required in the ALA films using the tunnel oxide annealed at 750°C, while the  $900^{\circ}\mathrm{C}$  films showed 13 V for 100 ms on the program voltage and -13 V for 1000 ms on the erase condition. The memory windows for the 750°C and 900°C films were 2.79 V and 1.64 V, respectively. As shown in Fig. 3 (a), the erase voltage was lower than the as-deposited film, and the memory window was higher than the as-deposited film. On the other hand, memory windows, shown in Figs. 3 (b) and 3 (c), were higher than that of Fig. 3 (a), and program/erase voltage and time of Figs. 3 (b) and 3 (c) were higher and longer than those of Fig. 3 (a). Hence, we believed the ALA film using the tunnel oxide annealed at 600°C was superior to the others.

Fig. 5 shows the results of retention tests of the ALA films using the tunnel oxide annealed at (a) 600°C, (b) 750°C and (c) 900°C. All specimens were measured at the 11 V for 10 ms (program condition) and –11 V for 100 ms (erase condition). Memory margins ( $V_{\rm th}$  of the program -  $V_{\rm th}$  of the erase) of the ALA films were not changed up to about  $10^4$  cycles. The memory margins of the ALA films using the asdeposited tunnel oxide showed similar results. <sup>12)</sup> In general, a flash memory device should be able to ensure a minimum of  $10^5$  cycles to be commercially viable. Since the result of a linear fit of the data shows that difference in  $V_{\rm th}$  between program and erase mode can be endured up to  $10^5$  cycles, it



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Fig. 5. Retention test of the ALA films using the tunnel oxide annealed at (a) 600°C, (b) 750°C, and (c) 900°C.

is thought that these data are sufficient to justify using ALA structures for commercial flash memory devices.

#### 4. Conclusions

In order to investigate the charge trap characteristics of ALA (Al<sub>2</sub>O<sub>3</sub>/La<sub>2</sub>O<sub>3</sub>/Al<sub>2</sub>O<sub>3</sub>) films using tunnel oxide annealed at the various temperatures, we deposited a 7 nm-Al<sub>2</sub>O<sub>3</sub> films for use as the tunnel oxide. Then, the films were annealed at 600°C, 750°C and 900°C. The final thicknesses of the Al<sub>2</sub>O<sub>3</sub> films were about 5 nm. A 5 nm-La<sub>2</sub>O<sub>3</sub> films used as a trap layer was then deposited on the tunnel oxide, followed by a 15 nm-Al<sub>2</sub>O<sub>3</sub> films structural characteristics (hillock formation) of the ALA films using the tunnel oxide annealed at 600°C appeared and substantially influenced the electrical properties, thereby, the program/erase conditions and memory characteristics were superior to other films using the tunnel oxide annealed at 750°C and 900°C. Although the value of the memory window of the ALA films using the tunnel oxide annealed at 600°C was not large, the value was over 1 V, and could be sufficiently distinguished by using the sense amplifier. Hence, we conclude that theses structures can be used in flash memory devices.

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