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65 nm CMOS 기술을 적용한 20 GHz 이하의 1 단 저잡음 증폭기 설계

(Design Optimization of a One-Stage Low Noise Amplifier below 20 GHz in 65 nm CMOS Technology)

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(Yehao Shen, Jaehong Lee, and Hyungcheol Shin)

요 약

20 GHz 이하의 주파수 범위에서 저잡음 증폭기의 성능지수를 최대화하기 위해 65 nm RF CMOS 기술을 이용하여 제작된 입력 트랜지스터의 바이어스 전압과 폭을 최적화 하였다. 만일 13 GHz 보다 동작 주파수가 높을 경우, 보다 높은 이득을 확보하기 위해 2단 증폭기의 적용이 필요하였다. 또한 5 GHz 보다 낮을 경우, 제한된 범위 내에서의 전력소모를 제어하기 위해, 입력 트랜지스터의 게이트와 소스사이의 추가적인 커패시터를 삽입하였다. 본 논문은 20 GHz 이하에서 동작하는 1단 LNA의 전반적인 성능을 검토하였고, 본 접근법은 다른 CMOS LNA 설계 기술에 적용가능하다.

Abstract

One-stage low noise amplifier (LNA) using 65 nm RF CMOS technology below 20 GHz is designed to find the optimal bias voltage and optimal width of input transistor so that the maximum figure of merit (FoM) has been achieved. If the frequency is higher than 13 GHz, the amplifier needs two-stage to achieve the higher gain. If the frequency is lower than 5 GHz, one additional capacitor between gate and source should be added to control the power under the limitation. This paper summarizes one-stage LNA overall performances below 20 GHz and this approach can also be applied to other CMOS technology of LNA designs.

Keywords: low noise amplifier (LNA), figure of merit (FoM), noise figure.

Ⅰ. Introduction

Recently, wireless market has evolved towards standards implementing higher bandwidth and data rate at higher frequencies. Radio frequency (RF) performance of CMOS transistors has been significantly improved due to continuous technology scaling-down. A low noise amplifier (LNA) is the first building block in the receiver system. Being the first circuit, the noise performance of an LNA plays a critical role in total receiver system noise. Therefore, an LNA should add little noise and provide high power gain for suppressing noise contribution from the next stages[1]. In this paper, we design one-stage LNAs to achieve the maximum figure of merit (FoM) below 20 GHz and present the performance results of the designed LNA.

Ⅱ. Design optimization of LNA

The conventional topology for one-stage CMOS

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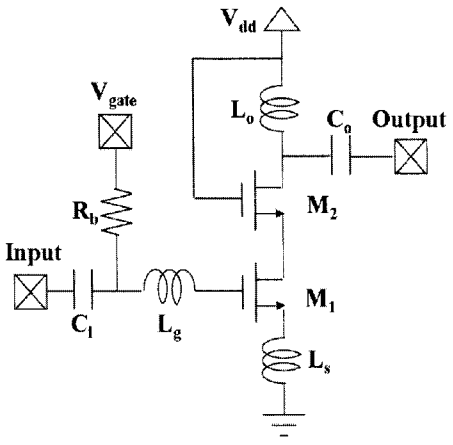

그림 1. CMOS 기술을 적용한 1단 저잡음 증폭기의 구조

Fig. 1. Conventional topology for one-stage CMOS low noise amplifier (LNA).

LNA is illustrated in Fig. 1. Core of the LNA consists of cascode transistor M_1 and M_2[2]. V_{dd} is set to be 1.2 V in this work. Figure 2 shows the small-signal equivalent circuit of LNA including both C_{gs} and C_{gd}. R_I is the sum of parasitic resistance of L_g and transistor gate resistance. R_{sig} is the source impedance of the circuit.

Although there are many performance factors in LNAs, we concentrate on three important characteristics such as power gain, noise figure and power dissipation. These are included in figure of merit equation which is defined as below.

$$FoM_{LNA} = \frac{G \cdot f}{(F-1) \cdot P} \tag{1}$$

where G is signal power gain in absolute unit, F is noise factor in absolute unit, P is power dissipation, and f is operation frequency.

From the small signal equivalent circuit, analytic equations of power gain, noise figure and power dissipation are derived as below.

$$Gain = \frac{P_{load}}{P_{in}} \approx \frac{1}{4} \cdot \left(\frac{g_{m1}}{\omega \left[C_{gs1} + C_{gd1} \left(1 + \frac{g_{m1}}{g_{m2}} \right) \right]} \right)^2 \tag{2}$$

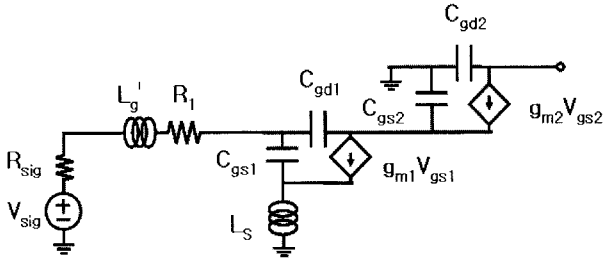

그림 2. 저잡음 증폭기의 소신호 등가회로

Fig. 2. Small signal equivalent circuit of conventional low noise amplifier.

$$F = 1 + \frac{R_I}{R_{sig}} + 4R_{sig}\alpha\frac{1}{\gamma}\frac{S_{id1}}{4kT} + 4R_{sig}\beta\frac{1}{\gamma}\frac{S_{id2}}{4kT} \tag{3}$$

$$P = V_{DD} \times I_D \tag{4}$$

In Eq. (3), α, β and γ can be expressed only with device parameters[3]. S_{id} is power spectral density (PSD) of channel thermal noise[4]. S_{id} for short channel devices is calculated with an analytic model [5].

III. Discussion

In order to achieve the best performance of an LNA, maximum FoM should be realized. The most important step of getting the maximum FoM is to find the optimal bias voltage and optimal width of the transistor. DC parameters such as I_d and g_m were measured in the devices from the wafer of 65 nm CMOS technology. Other small signal parameters such as R_g, C_{gs} and C_{gd} were also obtained from the S-parameters of device through measurement. From the input impedance equation, we determined L_g value. As well known, inductor quality factor, Q decreases with L_g increasing by an almost linear function. From the model of Q versus L_g, Q value can be obtained and the parasitic resistance of L_g, R_{lg} can also be calculated. Then, we determined L_s value by making real part of input impedance equal to 50 Ω. Last, the gain, noise figure and power consumption were calculated by using Eqs. (2)-(4), respectively to get the FoM. By changing the width

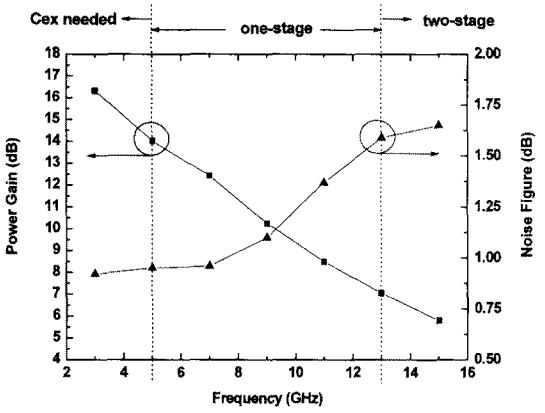

그림 3. 최대한의 성능 지수(FoM)를 얻기 위한 주파수별 전력 이득과 잡음 지수

Fig. 3. Power gain and noise figure versus frequency under maximum FoM condition.

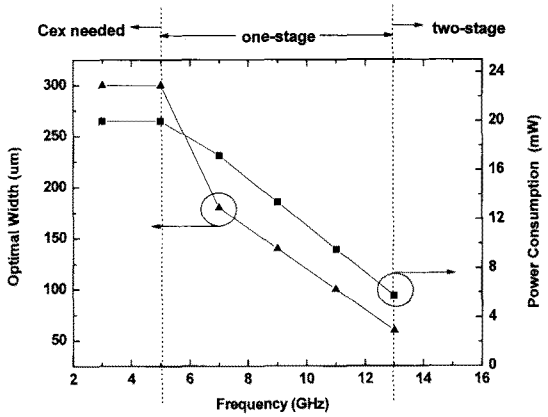

그림 4. 최대한의 성능 지수(FoM)를 얻기 위해 최적화된 주파수별 폭과 전력 소모

Fig. 4. Optimal width and power consumption versus frequency under maximum FoM condition.

표 1. 주파수별 1단 저잡음 증폭기의 성능 지수

Table 1. Performance results of one-stage LNA at different frequencies.

Frequency (GHz)	3	5	7	9	11	13	15
Gain (dB)	16.33	14.02	12.43	10.25	8.5	7.05	5.81
Noise Figure (dB)	0.92	0.95	0.96	1.1	1.37	1.59	1.55
Power Consumption (mW)	20	20	17.18	13.36	9.54	5.73	8.59
FoM (GHz/mW)	27.21	25.38	28.99	24.64	21.98	26.03	15.47
Optimal Bias (V)	0.6	0.6	0.65	0.65	0.65	0.65	0.65
Optimal Width (um)	300	300	180	140	100	60	90
C_{ex}(fF)	125	0	0	0	0	0	0

of transistors, I_d, g_m, C_{gs} and C_{gd} will change proportionally. The maximum FoM can be obtained by comparing each other under different widths.

Figure 3 shows the power gain and noise figure versus frequency respectively under the maximum FoM conditions. From Fig. 3, we can see that with the frequency increasing, the power gain decreases. If the frequency is above 13 GHz, the gain becomes smaller than 7 dB which is not enough for the normal specification, so that the two-stage LNA should be used to enlarge the power gain. We can also see clearly that higher frequency leads to larger noise figure.

Figure 4 shows the optimal width and power consumption versus frequency respectively under the maximum FoM conditions. Larger transistor width is needed at low frequency, so that the power consumption becomes higher. From Fig. 4 we can figure out that if the frequency is lower than 5 GHz, the power dissipation will be larger than 20 mW which was set to be the power consumption limit in our work's specification. In this situation, one additional capacitor C_{ex} between gate and source of M_1 should be added to control the power under the limitation. The value of C_{ex} should be chosen considering the compromise between the size of L_s and the available power gain. Too large L_s can lead to the increase in noise figure, while large C_{ex} leads to the gain reduction due to the degradation of the effective cutoff frequency of the composite transistor.

Table 1 summarizes the performance results of one-stage LNA at different frequencies including power gain, noise figure, power consumption, maximum FoM, optimal bias voltage and optimal width of transistor. After the optimal width of transistor is fixed, optimal bias voltage can be achieved by comparing FoM values under different bias voltages.

Ⅳ. Conclusions

In this paper, we designed one-stage LNA below 20 GHz in 65 nm RF CMOS technology in order to achieve the maximum FoM. When the frequency is higher than 13 GHz, a two-stage LNA should be used to achieve higher power gain. When the frequency is below 5 GHz, one extra capacitor, Cex has to be added in the circuit to control the power consumption to meet the specification. This design optimization presents a summary of one-stage LNAs performance results under 20 GHz using 65 nm CMOS technology and can be applied in other CMOS technologies, too.

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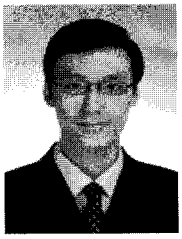

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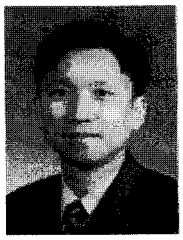

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