전력시스템을 위한 Active Damping Device

논 문
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An Active Damping Device for a Distributed Power System

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Abstract - Distributed power systems (DPSs) has been widely used various industrial/military applications due to their various advantages. Furthermore, the "All electric" concept, in conjunction with DC DPS, appears to be more advanced and mature in the AEV(All-Electric Vehicular) industry. Generally, AEV carry many loads with varied functions. However, there may be large pulsed loads with short duty ratios which can affect the normal operation of other loads. In this paper, a converter with spilt capacitors and a simple adaptive controller is proposed as a active damping device to mitigate the voltage transients on the bus. The proposed converter allows the smaller capacitive storage. In addition, the proposed control approach has the advantage of requiring only one sensor and performing both the functions of mitigating the voltage bus transients and maintaining the level of energy stored. The control algorithm has been implemented on a TMS320F2812 Digital Signal Processor (DSP). Simulation and experimental results are presented which verify the proposed control principle and demonstrate the practicality of the circuit topology.

Key Words : All-Electric Vehicle, Active Damping Device, Bidirectional Converter, Distributed Power System

1. Introduction

Distributed power systems (DPSs) offer many advantages to power system designers: high power capability, high efficiency, reliability, modularity, redundancy, expandability, and reduced development cost [1-2]. Also, DPS architecture has been used widely in such applications as aerospace systems, telecommunications, autonomous production lines, and defence electronic power systems. In addition, the concept of all-electric vehicle (AEV), in conjunction with DPS, has been found in land and sea-based vehicles as well, particularly for military applications, such as tanks and ships [3-4]. In these applications power availability and power density are of paramount importance and developments appear to be more advanced and mature than those in the AEV industry.

The loads in the AEV perform various functions, which are reflected in the type of load they present to the distribution and generation part of the electrical power distribution. Specially, in the AEV system, large pulse loads with short duty may affect the normal operation in the rest of loads. Moreover, the resulting transients on the supplying voltage bus are inevitably seen by the rest of the loads [5].

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Active damping devices or active dampers are power electronic converters that dampen the voltage transients on the bus. These active dampers could be divided into two types: voltage-storage and current-storage. The current-storage active damper exhibits inherently large conduction losses due to the circulating DC storage current. In addition, the converter is not effective in suppressing transients if the disturbance current exceeds the value of the storage current [6]. However, the active damper with voltage-storage avoids the above disadvantages by employing capacitive storage. The bus voltage must always be smaller than the storage voltage, and only their difference is available to transfer energy to the bus [7-8]. Furthermore, storage with large capacitance is employed. This renders the use of the capacitor as a storage component in this converter configuration rather inefficient. A converter that uses capacitive storage more efficiently is presented in this paper.

2. Converter Operation and Design

The proposed converter (Fig.1) differs little from the conventional active damper with the large capacitive storage [7-8]. The filter capacitor C_F has small value and its function is to filter out switching ripple. The inductor L_F limits the current interchanged between the bus and the storage capacitor C_{ST}. However, the storage voltage V_{ST} is referred not to the lowest (ground) potential, but to the voltage bus potential. This feature is attractive

because it allows the entire energy stored in the capacitor C_{ST} to be spent on bus transient mitigation. This ultimately allows for the smaller storage capacitor to be used and can negate the necessity to employ large (pressurised) electrolytic capacitor.

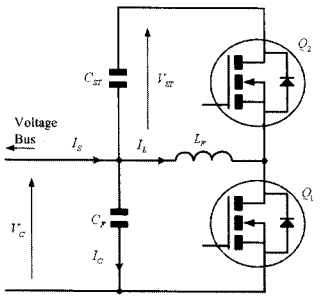


Fig. 1 Topology of the proposed converter

The principal idealised waveforms of the converter in steady-state are shown in Fig. 2. The two switches (Q_1, Q_2) are turned on alternately and are operated with a small dead-time t_d to allow for zero voltage switching (ZVS) by utilising the small energy stored in the filter inductor during commutation. The triangular inductor current results in a small voltage ripple (exaggerated here for clarity) superimposed on the nominal storage voltage level V_{ST}^*.

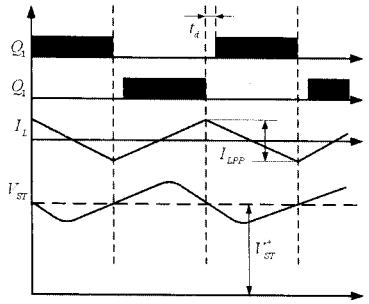


Fig. 2 Idealised waveforms of the converter

To maintain zero net current through the inductor, within each switching cycle the volt-second products for Q_1 on and Q_2 on need to be balanced, resulting in a steady-state duty ratio of

$$D_S = \frac{V_{ST}}{V_C + V_{ST}} \tag{1}$$

where the duty ratio Q_2 is defined as the ratio between the on-time of the bottom switch Q_1 and the switching period T_S. V_C is the bus voltage.

Prolonging the turn-on time of the bottom switch Q_1 results in current being sunk from the voltage bus and energy being transferred to the storage capacitor. Alternatively, prolonging the conduction of the top switch Q_2 results in energy being sunk from the storage capacitor and energy being injected into the bus.

The design of the converter as an active damper starts with the choices regarding the storage. The storage voltage needs to be as high as possible, but is limited by the voltage rating of the MOSFETs and other safety issues and was therefore chosen to be 500 V. A short pulsed-power load was rated at around 10 J, which means also the minimum energy storage capability of the storage capacitor. Thus, the needed energy storage has been sufficiently chosen 12.5 J and the necessary capacitor is C_{ST}=100 μF - small enough to utilise a small (in volume and weight) parallel set of high voltage foil capacitors. For comparison, with the converter in Fig. 2, a capacitor with the similar voltage rating would need to have a value of 1 mF - approximately ten times as larger [7-8].

The steady-state duty ratio, according to equation (1) and for a bus voltage V_C at 250 V, is D_S=0.66. The switching frequency was chosen to be 100 kHz, well within the capabilities of all power MOSFETs. To limit the inductor current to 2 A peak-to-peak, the value of the filter inductor L_F is 877 mH. The value of 1.2 μF for the filter capacitor L_F is calculated to limit the resulting voltage ripple, even when the conditioner is not connected to the bus, to 1 % of the nominal bus voltage, i.e. 2.7 V.

3. An Adaptive Control

Generally, controllers for active dampers with capacitive/inductive storage have several common disadvantages. First, these controllers require two control loops: (1) a main control loop, (2) an auxiliary control loop. The main control loop is to damp for the bus transients and the auxiliary control loop is to keep the storage current/voltage close to the desired level. However, in these types of controllers, the choice of the main control gain and the auxiliary control gain is quite so difficult because two control loops have conflicting objective. Second, these controllers require at least two voltage/current sensors because the control loop is two.

The proposed control approach uses the fact that if the current through the filter capacitor C_F is maintained to be zero, the resulting voltage at the input of the converter will remain unchanged. That is, the bus voltage will be maintained constant. In the part the bars over the variables mean the local average within the switching cycle. The duty ratio D is assumed not to change within a switching cycle.

A control law for the proposed converter may be

sought from the duty ratio. The storage voltage in the converter varies linearly with the duty ratio for the bus voltage. Namely, by means of the duty ratio, the converter can adjust the energy flow through the storage. Thus, the proper adjustment of the duty ratio D can stabilise the bus voltage through the converter. Also, the duty ratio, as a control law for the converter, can be separated two terms for both functions of mitigating the voltage bus transients and maintaining the level of energy stored: (1) the steady-state duty ratio of the converter, and (2) the current change of the filter capacitor due to the disturbances.

$$D=\frac{\overline{V_{ST}}}{\overline{V_C}+\overline{V_{ST}}}+\overline{I_C} \tag{2}$$

where D is the duty ratio at the steady state and $\overline{I_C}$ is the current of the filter capacitor C_F.

In equation (2), after the controller has damped the bus transient ($\overline{I_C}$ is brought down to zero) and in the absence of disturbance current, the average inductor current $\overline{I_L}$ will also be zero. The energy of the disturbance current is absorbed by the storage capacitor, causing its voltage to deviate from the desired (reference) storage voltage V_{ST}^*. Due to the randomness of the load commutations occurring on the voltage bus, it is reasonable to expect that the voltage across the storage capacitor is going to be largely confined to the desired value V_{ST}^*. However, it is possible that a sequence of events or a very large load transient might result in substantial deviation from this value. Thus it is necessary to guarantee that the storage voltage only deviates transiently from the desired value. The following shows that if the control law is modified to the form.

$$D=\frac{V_{ST}^*}{\overline{V_C}+V_{ST}^*}+\overline{I_C} \tag{3}$$

then this will result in the voltage across the storage capacitor being the required (reference) value V_{ST}^*. Immediately after the variations of the bus has been damped, the currents $\overline{I_C}$ and $\overline{I_S}$ will have converged to zero, and therefore $\overline{I_L}$ will also have become zero.

The signal $\overline{V_C}$ can be derived directly from the bus voltage as it is the voltage across the filter capacitor. Alternatively, when the switching frequency is low, the signal $\overline{V_C}$ can be derived from a low-pass filter, fed from the bus voltage. Also, the signal for the capacitor current $\overline{I_C}$ can be estimated from the bus voltage. The control equation then becomes

$$D=\frac{V_{ST}^*}{\overline{V_C}+V_{ST}^*}+\omega_c C_F\frac{s}{s+\omega_C}\overline{V_C} \tag{4}$$

where s is the Laplace operator and ω_c is the corner frequency of filter.

In equation (4), at low frequencies or as $s\rightarrow 0$, the filter transfer function may be approximated as s/ω_c. Thus, the filter capacitor current $\overline{I_C}$ can be easily estimated from the first-order high-pass filter of the equation (4).

The control block diagram by the control law equation (4) can be described as Fig. 3. The capacitor current $\overline{I_C}$ is obtained from the original bus voltage through a first order high pass filter with the corner frequency at 10 kHz. The pole in (4) is introduced to improve the noise immunity of the controller. However, its placement does limit the controller's bandwidth and is a compromise between controller simplicity and robust operation. Nevertheless, the control law expressed by equation (4) is a very attractive proposition because it requires only one voltage sensor; it performs both functions of mitigating the voltage bus transients and maintaining the level of energy stored; it is not computationally intensive even for relatively high switching frequency designs due to its simplicity.

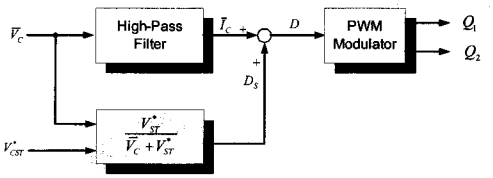


Fig. 3 The control block diagram of the active damper

4. Simulation and Experimental Results

In Fig. 4, the simplified schematic for simulation explains the concept of the active damper system for a DC DPS application. The system is divided into several parts. The first part is an power source V_S, the second part is a simple L-C filter which would normally be part of the power source, the third part is a pulsed power load and the last part is an active damper. Due to the limitations of the laboratory equipment and for the safe operation of the system, the experiments on the prototype system were performed with a pulsed power load of 3 kW. The input supply voltage V_S was chosen at 250 V. A diode blocks reverse current flow into the power supply. The input filter components were L_S=400 mH and C_S=50 μF. The corner frequency of this filter were around 1 kHz to attenuate the rectifier output ripple sufficiently. Two pulsed loads, a resistive load and a step-up converter, have been separately used as a pulsed power load, resulting

in a power load of 3 kW. The pulsed load was activated and deactivated at 90 Hz with a 50% duty ratio.

The complete system has been simulated using the SABER package. In the experiment work, as far as the controller implementation is concerned, a fixed point 32-bit DSP (TMS320F2812) by Texas Instruments has been used to implement the control algorithm. To ensure that both top and bottom MOSFETs never turn on simultaneously, the dead time was chosen to be 1 μs. Also, a voltage transducer LV25-P manufactured by LEM Components was used to measure the DC bus voltage. In this part, the simulation and experimental results are fully compared and discussed. The system performance without and with the active damper are presented

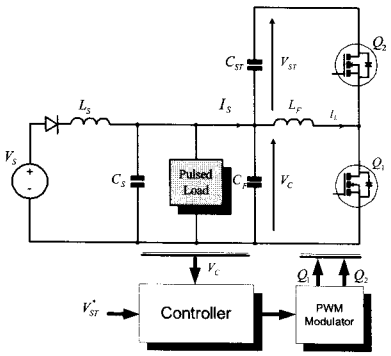


Fig. 4 The schematic diagram of the active damper system for a DC DPS

In Fig. 4, for the easy implementation of the control law equation in software, a difference equation is used. The implementation of control law (4) can be simply expressed by a running average of the input and output data

$$D(n)=\frac{V_{ST}^*(n)}{\overline{V_C}(n)+V_{ST}^*(n)}+\overline{I_C}(n) \tag{5}$$

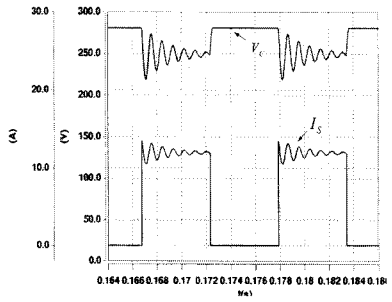
$$\overline{I_C}(n)=2\pi f_c C_f \alpha[V_c(n)-V_c(n-1)]+\gamma\overline{I_C}(n-1) \tag{6}$$

$$\alpha=\frac{1+\gamma}{2},\ \gamma=\frac{\cos\theta_c}{1+\sin\theta_c},\ \theta_c=2\pi f_c/f_s \tag{7}$$

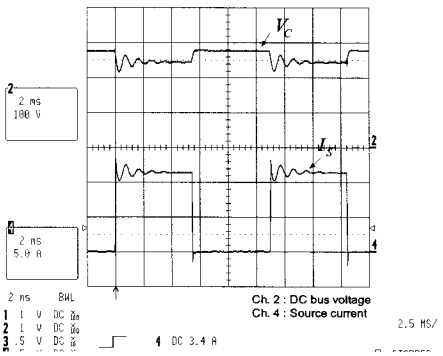
where $V_{ST}^*(n)$, $\overline{V_C}(n)$, and $\overline{I_C}(n)$ are the current voltage sample for the desired capacitive storage voltage, the current DC bus voltage sample, and the current estimated filter capacitor current sample, respectively. $\overline{V_C}(n-1)$ and $\overline{I_C}(n-1)$ are the previous samples for the DC bus voltage and the estimated filter capacitor current. f_c is the corner frequency of the filter and f_s is the sample frequency.

4.1 Simulation and experimental results without the active damper

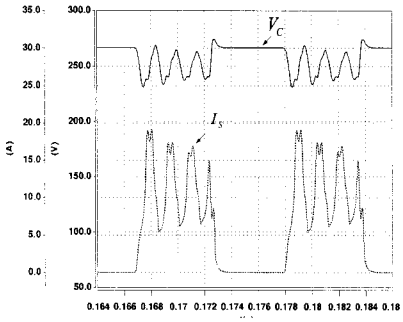
The simulation and experimental results when a resistive load and a converter load are separately connected to a DC DPS are shown in Fig. 5. In the simulation and



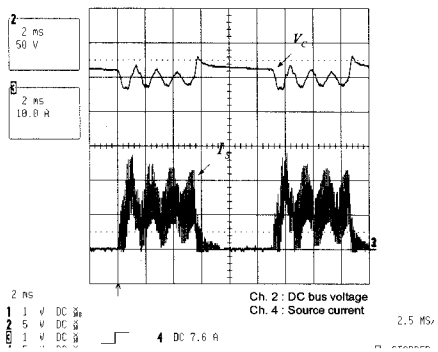
(a) Simulation Results (Resistive Load)



(b) Exprimental Results (Resistive Load)



(c) Simulation Results (Converter Load)



(d) Exprimental Results (Converter Load)

Fig. 5 Simulation and experimental results

experimental results, the large power of load may result in the severe bus transients. Oscillations at 1 kHz, caused by the input filter components L_S and C_S, are observed whenever the resistive load is activated. The voltage

excursions on the bus voltage (nominal 250 V) are between 217 V and 282 V (±13% of steady-state). Moreover, large oscillations at 600 Hz can also be seen whenever the converter load is activated, due to the interaction between the input filter and the load converter filter. The voltage excursions on the bus voltage (nominal 250 V) are between 231 V and 274 V (±10% of steady-state).

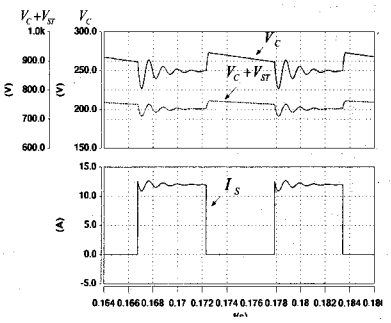
From the above waveforms, although there is a slight difference between the results which could be because of component tolerances, it is clear that the experimental results correspond with the simulation results very well. Also, the pulsed power load may significantly affect the normal operations of the other loads and result in instability of the DPS. Furthermore, if the load power increases more, transients on the bus will be more increased.

4.2 Simulation and experimental results with the active damper

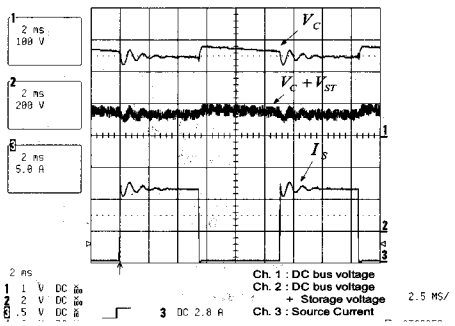
The simulation and experimental results when a resistive load and converter are connected to the DC DPS are shown in Fig. 6. Although oscillations are observed, from the above results, the voltage transients are considerably smaller and better damped than those without the active damper. The voltage excursions on the bus voltage (nominal 250 V) are between 229 V and 271 V (±8% of steady-state) in the resistive load. Also, the bus voltage variations (nominal 250 V) are between 239 V and 260 V (±8% of steady-state) in the converter load.

The reason for the more severe turn-off transient in the experimental case is likely to be due to the extra delays, etc. introduced by the real components compared to be idealised devises used in the Saber simulation. This, in turn, causes the real active damper to have a poorer rate of response to the turn-off transient. Thus, there are small differences between the simulation and experimental results which could be because of the component tolerances of the load converter and active damper. From the above results, compared with the simulation results, the experimental results are a little worse. However, although these differences exist between the simulation and experimental results, the simulation results are very similar to the experimental results. Therefore, it is clear that the experimental results match the simulation results very well.

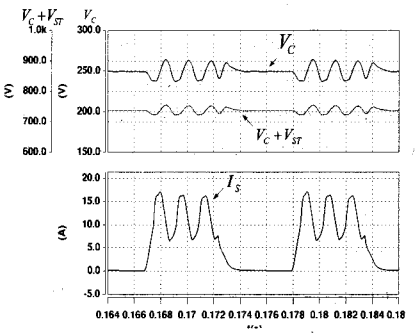
Compared to those without the active damper, the voltage bus transients are very much mitigated, and the stored energy level is maintained by the proposed active damper and controller. Thus, the above simulation and experimental results indicate that the total energy stored in the reduced storage capacitor is used more efficiently during bus transient mitigation. This may alleviate the need to use a large (pressurised) electrolytic capacitor in the active damper system. Also, the results shows the proposed controller has excellent performance. The proposed control principle is thus validated and the practicality of the controller demonstrated.



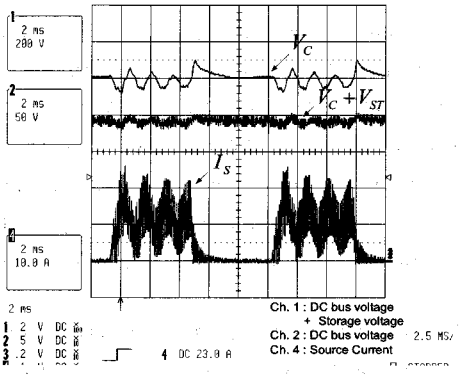
(a) Simulation Results (Resistive Load)



(b) Exprimental Results (Resistive Load)



(c) Simulation Results (Converter Load)



(d) Exprimental Results (Converter Load)

Fig. 6 Simulation and experimental results

5. Conclusion

This paper has presented an active damper system with a built-in bidirectional DC/DC converter with reduced capacitive storage. The total energy stored in the reduced capacitor is used more efficiently during bus transient mitigation. This may eventually remove the need to use a large (pressurised) electrolytic capacitor in the active damper system. For comparison, with the conventional converter, capacitor with the similar voltage rating would need to have a value of 1 mF - approximately ten times as larger. In addition, a simple controller based on a time domain approach has been proposed and realized by a DSP. The test results show that the proposed approach not only effectively mitigates the bus voltage transients caused by pulsed power loads, but also contributes to the improvement of the power quality and the stability of the power distribution system. The proposed circuit topology and control approach are clearly applicable to systems other than AEV, where critical equipment needs to be protected from bus voltage variations in a dynamic and noisy environment.

감사의 글

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