Effects of Rapid Thermal Annealing Temperature on Performances of Nanoscale FinFETs

M. Sengupta*, S. Chattopadhyay*, and C.K. Maiti**

***Abstract*—In the present work three dimensional process and device simulations were employed to study the performance variations with RTA. It is observed that with the increase in RTA temperature, the arsenic dopants from the source /drain region diffuse laterally under the spacer region and simultaneously acceptors (Boron) are redistributed from the central axis region of the fin towards the Si/SiO2 interface. As a consequence both drive current and peak cut-off frequency of an n-FinFET are observed to improve with RTA temperatures. Volume inversion and hence the flow of carries through the central axis region of the fin due to reduced scattering was found behind the performance improvements with increasing RTA temperature.**

***Index Terms*—FinFET, RTA temperature, volume inversion, cut-off frequency.**

I. INTRODUCTION

As an inevitable consequence of the continuous downscaling throughout the last few decades, conventional complementary-metal-oxide-semiconductor (CMOS) process technology is facing fundamental limits of material and process [1]. Even, application of new channel materials and gate insulator cannot meet all the ITRS projections below 65 nm CMOS technology generation with conventional structures [2,3]. Non-classical structures are emerging as potential solution to these technological roadblocks [4-6]. FinFET (Fig. 1(a)), a promising candidate among the non-classical structures, is making its place by manifesting superior scalability, improved performance, immunity to short channel effects and feasibility to the existing process technology with few mask level modifications [7]. In non-classical architectures, such as FinFET, dopant redistribution inside a 3D structure with feature-size below 65 nm is an important issue because it will govern complex channel profile as well as over all device performance.

FinFETs can be categorized as either double gate (DG) or triple gate (TG) depending upon the top-wall oxide layer thickness. In DG FinFET thick top-wall oxide layer (Fig. 1(b)) electrically isolates the top gate from the channel, where as, in TG FinFET, the oxide layer (Fig. 1(c)) is uniform in the vertical as well as top wall of the fin. They have effective channel width $W_g = 2H_{fin}$ (for DG FinFET) and $W_g = 2H_{fin} + W_{fin}$ (for TG FinFET). For narrow fin widths volume inversion [8] is found to occur in such devices. Volume inversion is a phenomenon in which inversion carriers are not confined near the Si/SiO_2 interface, as predicted by classical device physics, but rather at the center of the fin. The carriers from the volume inversion region experience scattering from the implanted impurities (here it is Boron). These implanted impurities get redistributed with any heat cycle, such as RTA. RTA helps in dopant-activation but simultaneously causes lateral spreading of dopants inside the device. Thus complex three dimensional channel profile and hence the device performance is controlled by RTA. In the present work RTA temperature was varied for a triple gate FinFET, keeping other process and structural parameters intact.

Manuscript received Aug. 13, 2009, revised Oct. 23, 2009.
* Department of Electronic Science, University of Calcutta, Kolkata - 700009, India
** Department of Electronics and ECE, Indian Institute of Technology, Kharagpur - 721302, India
Email: scelc@caluniv.ac.in

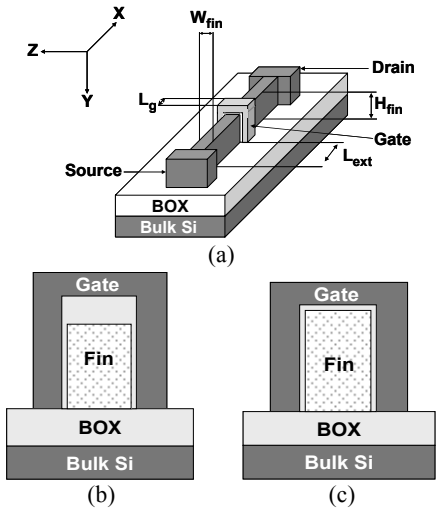


Fig. 1. (a) Schematic of a triple gate FinFET. 2-D cut plane view of (b) DG FinFET and (c) TG FinFET.

II. THREE DIMENSIONAL PROCESS AND DEVICE SIMULATION:

1. 3D Process Simulation

The three dimensional TG FinFET structure was simulated using Taurus^{TM}, a three dimensional process and device simulator from Synopsys [9]. The key process steps used in the simulation are – silicon on insulator (SOI) substrate with 100 nm buried oxide (BOX) and 45 nm silicon layer, 65 nm hard mask (TEOS) deposition, patterning of silicon fin by dry etching, channel implantation with Boron (energy = 20 keV, dose = 4.5 x 10^{13} cm^{-2}), 3 nm gate oxide, 100 nm poly-silicon (phosphorous doping of 10^{20} cm^{-3}) gate deposition, 65 nm hard-mask (TEOS) deposition, patterning of gate by dry etching, deposition of 25 nm nitride spacer, selective epitaxy for raised source/drain of 60 nm, source/drain implantation with arsenic (energy = 50 keV , dose = 3 x 10^{15} cm^{-2}) and junction anneal (RTA) . The process flow is shown Fig. 2.

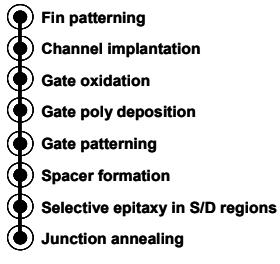


Fig. 2. Simulated process flow for FinFET devices.

2. Benchmarking

The simulated structure was benchmarked using available experimental data [4] of a FinFET with W_{fin} = 20 nm, H_{fin} = 45 nm and L_g = 20 nm and gate oxide thickness (t_{ox}) = 3 nm. The corresponding I_{ds} vs. V_{gs} is shown in Fig. 3. Then the RTA temperature was varied for a 65 nm node [10] FinFET with W_{fin} = 10 nm, H_{fin} = 50 nm, L_g = 25 nm and t_{ox} = 1.1 nm. Device simulation includes quantum confinement effect, band-gap narrowing effect, low and high field mobility and recombination effects. Threshold voltage was extracted according to the convention mentioned in [4].

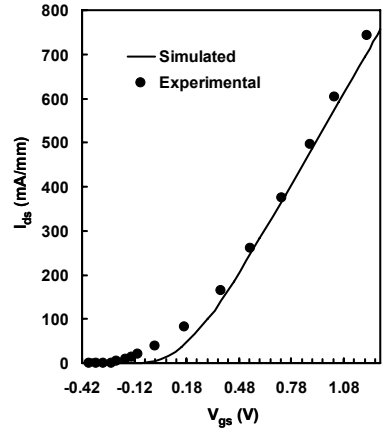


Fig. 3. Calibrated transfer characteristics at drain to source voltage of 1.2 V.

III. RESULTS AND DISCUSSION

Fig. 4 shows the net doping profiles along the channel at various RTA temperatures. It is observed from Fig. 4 that donors (Arsenic) from the source/drain region diffuse laterally under the spacer (L_{ext} region).

This decreases effective channel length ($L_{ch} = L_g + 2L_{ext}$). Lateral diffusion of dopants is more probable to create underlap than overlap region.

Fig. 5(a) shows acceptor (Boron) doping concentration profile from the top SiO_2/Si interface to the bottom Si/BOX interface of the fin at the middle of the vertical plane equidistant from source and drain at various RTA temperatures. It is observed from the figure that the acceptor doping was not varied significantly with the increase in annealing temperature around the top Si/SiO_2 interface. It also shows that the acceptor doping concentration is higher in the lower half of the fin as

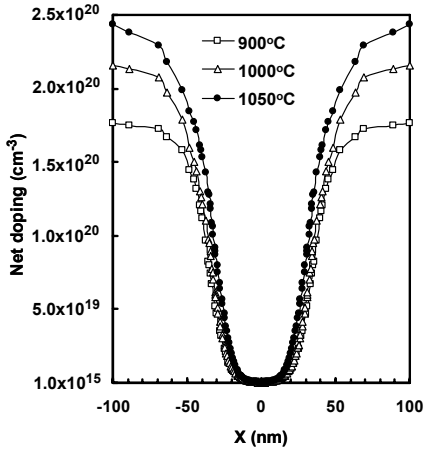
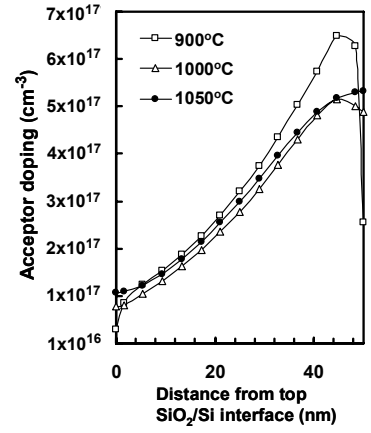
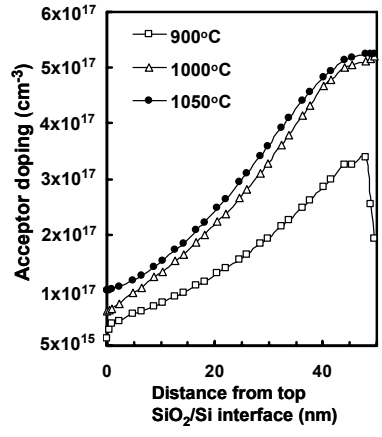


Fig. 4. Net doping profiles along channel at various RTA temperatures. The corresponding cut-lines were drawn 1 nm below the top Si/SiO_2 interface for all the devices.

compared to the upper half, indicating that the boron diffusion from central-axis region of the fin towards sidewalls is only effective near the bottom Si/BOX interface. It is also observed that the acceptor doping level increases at the top interface with the increase in RTA temperature. However, it decreases from the top interface towards the bottom interface for 1000°C and 1050°C in comparison to 900°C annealing temperature. The observation gives a design space for such devices. If the device is designed for allowing maximum current near the bottom interface then dopant activation should be carried out at 900°C. On the other hand, if the designer wants majority of the current to flow near the top interface then activation annealing should be carried out at 1000°C or 1050°C. As a consequence, there may be a variation of mobility and transconductance from top towards the bottom interface. However, as the output characteristics are the overall measure of such variations, there will not be any impact on the device output parametric values. This could be verified from the current – voltage characteristics (Fig. 6(a) and (b)). Fig. 5 (b) shows similar variation of acceptor (Boron) doping concentration profile near the one of the vertical Si/SiO_2 interface. Fig. 5(b) indicates that the acceptor doping level increases near the vertical Si/SiO_2 interface with the increase in the RTA temperature. So, it is clearly observed from these figures that the acceptor doping concentration is higher at the middle of the fin than near the sidewall Si/SiO_2 interface at lower RTA temperature. Now, as the RTA temperature is gradually increased,



(a)



(b)

Fig. 5. Acceptor doping profile from top Si/SiO_2 interface to bottom Si/BOX interface at various RTA temperature (a) at the middle of the gate, (b) 0.5 nm away from the sidewall Si/SiO_2 interface. The corresponding cut-lines were drawn at a vertical plane equidistant from source and drain.

acceptor doping at the middle of the fin starts to decrease and simultaneously acceptor doping near vertical Si/SiO_2 interface starts to increase. It implies that with increase of RTA temperature the acceptors diffuse laterally from middle of the fin towards the sidewalls. This redistribution can be explained using the theory of diffusion. According to Fair's model of diffusion the Boron is assumed to diffuse exclusively through vacancy mechanism. The extrinsic diffusivity of boron is given by

$$D_x = D^0 + D^+ \left[\frac{p}{n_i} \right] \tag{1}$$

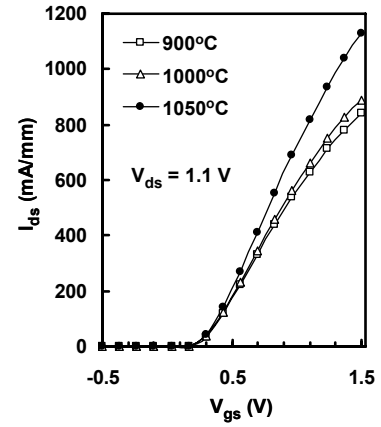
where p is the hole concentration, n_i is intrinsic concentration ($n_i = \sqrt{N_c N_v} \exp\left(-E_g / 2V_t\right)$: E_g is the bandgap

of pure silicon, N_c and N_v are the density of states in the conduction band and valance band and thermal voltage $V_t = kT/q$ where k is the Boltzmaan's constant, q is the magnitude of electrical charge on the electron and T is the temperature in Kelvin). Now, $D^0\left(=0.76\exp(-3.46/kT)\ \text{cm}^2\ \text{s}^{-1}\right)$ and $D^+\left(=0.23\exp(-3.46/kT)\ \text{cm}^2\ \text{s}^{-1}\right)$ are the coefficient of boron-neutral-point defect pair and boron-positively-charged point defect pairs (where 3.46 in the exponential part is the activation energy in eV) [11]. Boron has a tetrahedral radius of 0.82 nm vs. 1.18 nm for silicon. Thus Boron acts as a fast diffuser. From equation (1) it can be seen that the diffusivity of the boron increases with the increase in temperature. Thus with the increase in RTA temperature the diffusivity of the boron increases and they diffuse from central-axis region of the fin towards sidewalls.

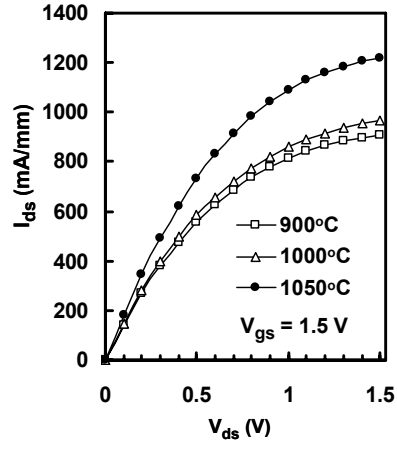
Similar behavior of acceptors was observed near the top Si/SiO_2 interface with respect to the horizontal plane at the middle of the fin. Thus it may be summarized that acceptor impurities diffuses from the central-axis region of the fin to outwards with the increase in RTA temperature. With the increase in RTA temperature the volume inversion [8] was found to occur inside the fin.

Fig. 6 (a) and (b) shows I_{ds} *vs.* V_{gs} and I_{ds} *vs.* V_{ds} plots respectively at various RTA temperatures. It is indicative from Fig. 6 (a) and (b) that the drain current increases with increase in RTA temperature which may be attributed to the increased no of activated donor (Arsenic) dopants and shortening of the effective channel length (L_{ch}) by the lateral diffusion of the donors. The increase in the drain current may also be attributed to the volume inversion. As more number of acceptors move from central-axis- region of the fin towards the Si/SiO_2 interface with increasing RTA temperature, scattering becomes less in the central-axis region of the fin, hence the carriers from the volume/bulk inversion region reinforce drain current with increasing RTA temperature.

Fig. 7 shows the potential variation in between two vertical gates at various RTA temperatures. It can be observed from Fig. 7 that the potential is lowered with the increase in RTA temperature. The separation between the two consecutive potential curves is less near the Si/SiO_2 interface and more at the central-axis region of the fin. It implies that the lowering of the potential is much more in the central-axis region of the fin than at the interface.



(a)



(b)

Fig. 6. (a) Transfer characteristics and (b) output characteristics are shown as a function of RTA temperatures.

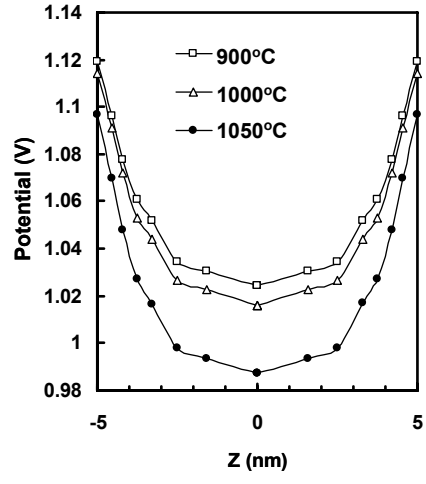


Fig. 7. Potential variation between two vertical Si/SiO_2 interfaces of TG-FinFET at various RTA temperatures. The corresponding cut-lines were drawn 1 nm below the top Si/SiO_2 interface in a cut-plane equidistant from the source and drain. Vgs and V_{ds} are kept at 1.0 and 1.1 V respectively.

The general expression of threshold voltage incase of a TG FinFET [12] is given by

$$V_{TH} = V_{FB} + 2\psi_B + \frac{qN_A}{C_{OX}}\frac{W_{fin}}{3} \quad (2)$$

where, V_{FB} is the flat band voltage, ψ_B is the value of the potential at the body of the fin, C_{ox} is oxide capacitance and N_A is acceptor doping concentration.

Fig. 8 shows the variation of threshold voltage with RTA temperature. It shows a small reduction of threshold voltage with the increase in RTA temperature. It has been shown that the acceptors from the lower half of the fin are redistributed towards the sidewall interfaces with the increase in RTA temperature. The threshold voltage of the FinFET has been extracted at a constant current of 10^{-7} A from drain current – gate voltage (I_{ds} *vs.* V_{gs}) characteristics (Fig. 6 (a)). The drain current has been observed to increase with increasing annealing temperature. It should be noted that the current is the net flow of carriers across the channel and therefore, the variation of acceptor doping concentration from the top towards bottom interface is insignificant in estimating such net currents. The threshold voltage may be higher near the bottom interface since this region has higher acceptor density and hence less surface potential for a given gate bias. Moreover, the acceptor doping concentration near the bottom has been observed to be reduced with increasing annealing temperature (see Fig. 5 (a), (b)). Thus, the little reduction of threshold voltage with annealing temperature is attributed to the increase of acceptor doping concentration with the increase of annealing temperature.

Fig. 9 shows the variation of total gate capacitance with gate voltage at various RTA temperatures. It can be observed from Fig. 9 that total gate capacitance at any fixed gate voltage, increases with RTA temperature below the gate voltage of 1.2 V. This increase may be attributed to the decrease in depletion layer thickness with increase in acceptors near Si/SiO_2 interface, as given by the following equation [13].

$$x_d = \sqrt{\frac{2\varepsilon_{Si}\psi_s}{qN_A}} \quad (3)$$

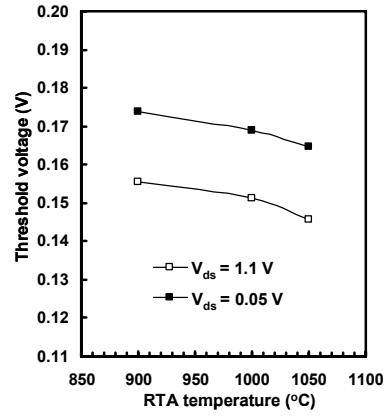


Fig. 8. Variation of threshold voltage with RTA temperature.

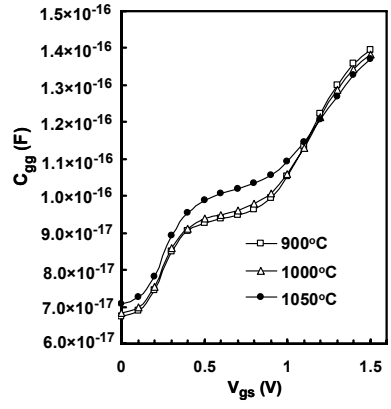


Fig. 9. Variation of total gate capacitance (C_{gg}) with gate to source voltage (V_{gs}) at different RTA temperatures. The drain to source voltage is kept at 1.1 volt.

where, ε_{Si} is the permittivity of the Si, ψ_s is the surface potential and q is the electronic charge.

Cut-off frequency [5] of a FinFET is defined as

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (4)$$

where, g_m is the transconductance and C_{gg} is total gate capacitance of the device. The above equation clearly indicates that cutoff frequency increases with the increase in g_m and decrease with the increase in C_{gg}.

Fig. 10 shows the variation of cut-off frequency with drain current at various RTA temperatures. It is indicative from Fig. 10 that peak cut-off frequency increases with the increase in RTA temperature. Increase in RTA temperature drives the acceptors towards the Si/SiO_2 interface and carriers experience less scattering

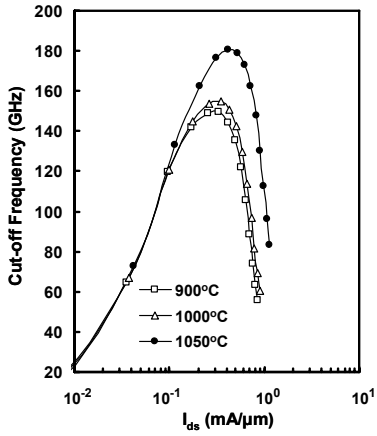


Fig. 10. Plot of cut-off frequency vs. drain current.

in the region away from the Si/SiO_2 interface. Consequently the central-axis region of the fin offers higher mobility and higher transconductance. Total gate capacitance and transconductance both increase with RTA temperature but the increment rate of transconductance is higher than that of the total gate capacitance. Thus increase in the cut-off frequency with increasing RTA temperature may be attributed increase of transconductance.

IV. CONCLUSIONS

FinFET has a non-planer structure and complex channel profile which is influenced by RTA temperature. Increase in RTA temperature drives acceptors from the central-axis region of the fin towards the Si/SiO_2 interface. The drive current increases with the increase in RTA temperature, through volume inversion due to the increase in mobility in the central-axis region of the fin as well as due to shortening of channel length by the lateral diffusion of Arsenic dopants under the spacer region. Decrease in threshold voltage with increasing RTA temperature is attributed to simultaneous increase in Boron doping concentration near the Si/SiO_2 interface and decrease in potential (ψ_B). The increase in cutoff frequency with increasing RTA temperature is attributed to the increase in transconductance due to reduced scattering in the central-axis region of the fin. From the obtained results in the considered temperature region it is observed that 1050 ^oC annealing temperature provides higher transconductance, mobility and higher cut-off frequency.

REFERENCES

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur and H.-S. P. Wong, "Device scaling limits of Si MOSFET's and their application dependencies," *Proc. IEEE*, Vol.89, pp.259–288, Mar., 2001.

[2] B. Yu, H. Wang, A. Joshi, Q. Xiang, E. Ibok, and M. -R. Lin, "15 nm gate length planar CMOS transistor," in *Int. Electron Devices Meeting Tech. Dig.*, 2001, pp.937–939.

[3] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi and M. Bohr, "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors," in *Symp. VLSI Technology Dig. Tech. Papers*, 2000, pp.174–175.

[4] M. Nawaz, W. Molzer, P. Haibach, E. Landgarf, W. Rosner, M. Stadele, H. Luyken and A. Gencer, "Validation of 30 nm process simulation using 3D TCAD for FinFET devices," *Semicond. Sci. Technol.*, Vol.21, pp.1111-1120, Jul., 2006.

[5] A. Kranti and G. A. Armstrong, "Comparative analysis of nanoscale MOS device architechtures for RF applications," *Semicond. Sci. Technol.*, Vol. 22, pp.481-491, Mar., 2007.

[6] A. Kranti and G. A. Armstrong, "Performance assesment of nanoscale double- and tripple-gate FinFETs", *Semicond. Sci. Technol.*, Vol.21, pp.409-421, Feb., 2006.

[7] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios and R. Chau, "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," *Symp. on VLSl Tech*, pp.133-134, June, 2003.

[8] L. Ge and J. G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs," *IEEE Trans. Electron Devices*, Vol.49, pp.287-294, Feb., 2002.

[9] Taurus Process™ and Taurus Device™ Simulators, Version. X-2005.10, Synopsys Inc.

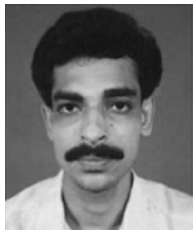
[10] ITRS 2008 , http://www.itrs.net/

[11] R. Kinder, F. Schwierz, P. Beno and J. Gebner, "Simulation of boron diffusion in Si and strained SiGE layers," *Microelectron Jour.*, Vol.38, pp.576-582, Apr., 2007.

[12] C.W. Lee, S.R.N Yun, C.G Yu, J.T. Park and J.P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid state Electron.*, Vol.52, pp.505-510, Jan., 2007.

[13] J.P. Colinge and C.A. Colinge, *Physics of Semiconductor Device*. California, U.S.: Kluwer Academic Publishers, 2006.

Mridul Sengupta received the B.Sc. degree (Hons.) in Physics from University of Calcutta, Kolkata, in 2005 and M.Sc. degree in Electronic Science from Department of Electronic Science, University of Calcutta, Kolkata, in 2007, respectively. He worked as Jounior Project Assistant (JPA) in time bound research project at the Department of Electronics and ECE, Indian Institute of Technology, Kharagpur during 2007 to 2009. He is currently pursuing the Ph.D. degree in the Department of Electronic Science, University of Calcutta, Kolkata. His research focuses on analysis, design and physical modeling of nanoscale Multiple Gate Devices, such as Double and Triple Gate FinFET devices.



Sanatan Chattopadhyay received the B.Sc. degree (Hons.) in physics and the M.Sc. degree in electronics science from the University of Calcutta, Calcutta, India, in 1992 and 1994, respectively, and the Ph.D. degree from the University of Jadavpur, Calcutta, in 1999. From 1999 to 2001, he was a Post-Doctoral Fellow at the Singapore–Massachusetts Institute of Technology (MIT) Alliance, Singapore, before joining the University of Newcastle-upon-Tyne, Newcastleupon-Tyne, U.K. Currently he is working as a faculty in the Department of Electronic Science, University of Calcutta, India. His current research interests include the fabrication and characterization of strained Si/SiGe MOSFETs, nano-scale CMOS, low resistive silicides/germanides for contact metallization in very large scale integration, and growth and characterization of ultrathin dielectric gate materials.

C. K. Maiti received the B. Tech. and M. Tech. degrees in Applied Physics and Radio- Physics and the Ph. D. degree in Electronics from the University of Calcutta and IIT Kharagpur in 1972, 1974 and 1984, respectively. From 1984 to 1990, he was an Assistant Professor. From 1990 through 1999, he served as an Associate Professor and was promoted to Professor in 1999 in the Department of Electronics and Electrical Communication Engineering, IIT-Kharagpur. He has published four books in the Silicon-Germanium and strained Silicon area. He has also served as the Guest Editor for the Special Issues on Silicon-Germanium of Solid-State Electronics (November 2001 issue) and Heterostructure Silicon (August 2004 issue). His current research interests include Microelectronics, Silicon Heterostructures, Technology CAD and Internet Laboratory Development.