RF CMOS Power Amplifiers for Mobile Terminals

Ki Yong Son, Bonhoon Koo, Yumi Lee, Hongtak Lee, and Songcheol Hong

Abstract— **Recent progress in development of CMOS power amplifiers for mobile terminals is reviewed, focusing first on switching mode power amplifiers, which are used for transmitters with constant envelope modulation and polar transmitters. Then, various transmission line transformers are evaluated. Finally, linear power amplifiers, and linearization techniques, are discussed. Although CMOS devices are less linear than other devices, additional functions can be easily integrated with CMOS power amplifiers in the same IC. Therefore, CMOS power amplifiers are expected to have potential applications after various linearity and efficiency enhancement techniques are used.**

Index Terms—**CMOS, linearity, power amplifier (PA), transmission line transformer**

I. INTRODUCTION

Traditionally, high speed circuits including RF power amplifiers (PAs) are implemented using compound semiconductor technologies, such as GaAs and InGaP heterojunction bipolar transistors. The development of CMOS technology is improving the high-frequency characteristics of CMOS active devices; this improvement may lead to development of a single-chip transceiver. This cost-effective solution is a requirement of the RF front-end in mobile electronic devices.

However, lossy substrates, low quality factors, and low breakdown voltages of CMOS active devices cause problems when using them in RF PAs. To overcome these obstacles, a PA structure based on the transmission line transformer has been developed [1-9]. The transmission line transformer is used for impedance transformation and output voltage combining. CMOS PAs have the advantage that various functions can be added to enhance their linearity and efficiency.

In this paper, recent progress in CMOS PAs for mobile terminals is reviewed. First, the switching mode PAs are presented with the various transformer structures. Then, the design challenge in linear PAs is outlined. CMOS PAs are expected to have potential applications after various linearity and efficiency enhancement techniques are used.

II. CMOS SWITCHING MODE POWER AMPLIFIERS

1. Overview of CMOS Switching Mode PAs

Many of the previously reported watt-level CMOS PAs are switching mode amplifiers. They use active devices as switches, so they can minimize the power dissipation of active devices. In switching mode PAs, output power is not dependent on input power, so they are used in constant envelope modulation schemes and polar transmitters. In terms of P_{out} - P_{in} relationship, they operate at the saturated output power level, so they can have high efficiency. In addition, watt-level output power is achieved with the aid of the on-chip voltage combining structure for handset applications.

In the design of CMOS PAs, the cascode structure is used to overcome the low breakdown voltage of CMOS devices, the differential structure is used to reduce the effects of bonding wires, and a slab inductor is used for transmission line transformer, to reduce power loss.

Manuscript received Aug. 5, 2009; revised Sep. 26, 2009.
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea
E-mail : moulinrouge@kaist.ac.kr

2. Transmission Line Transformer

CMOS active devices have low breakdown voltages, and this characteristic limits the output power of the amplifier. Therefore, impedance transformation is required to transform the external 50-Ω impedance to a smaller load impedance. This transformation requires 1:N impedance transformation, which can be achieved using multiple 1:1 transmission line transformers (Fig. 1).

In real implementations, several types of on-chip power combiner have been proposed for CMOS PAs (Fig. 2). The distributed active transformer, which has circular geometry, introduced a fully integrated watt-level CMOS PA [1]. The 'figure 8' power combiner minimizes cancellation of the internal flux so that better coupling and efficiency are achieved [2]. The tournament-shaped power combiner solves the feed-line coupling problem [3]. The parallel power combining transformer also gives another configuration for on-chip power combing [4].

The quasi-four-pair structure (Fig. 3) [5] uses a novel configuration of the cascode structure to increase output power. Two common-gate transistors are connected to one common-source transistor. The additional common-gate transistor provides multiple amplification paths in the power stage. Thus, by forming a differential pair with this configuration, plural output combining can be accomplished using one-differential common-source pair in the power stage. It can increase the impedance transforming ratio and the number of the differential pairs under ideal voltage combining. Thus, additional pairs of combining in the output stage can increase output power. The circuit constitution for the driving power stage is the same as the two-pair structure. Accordingly, the four-pair structure provides both high output power capability and simple implementation.

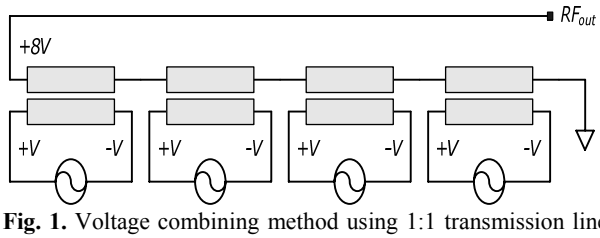


Fig. 1. Voltage combining method using 1:1 transmission line transformer.

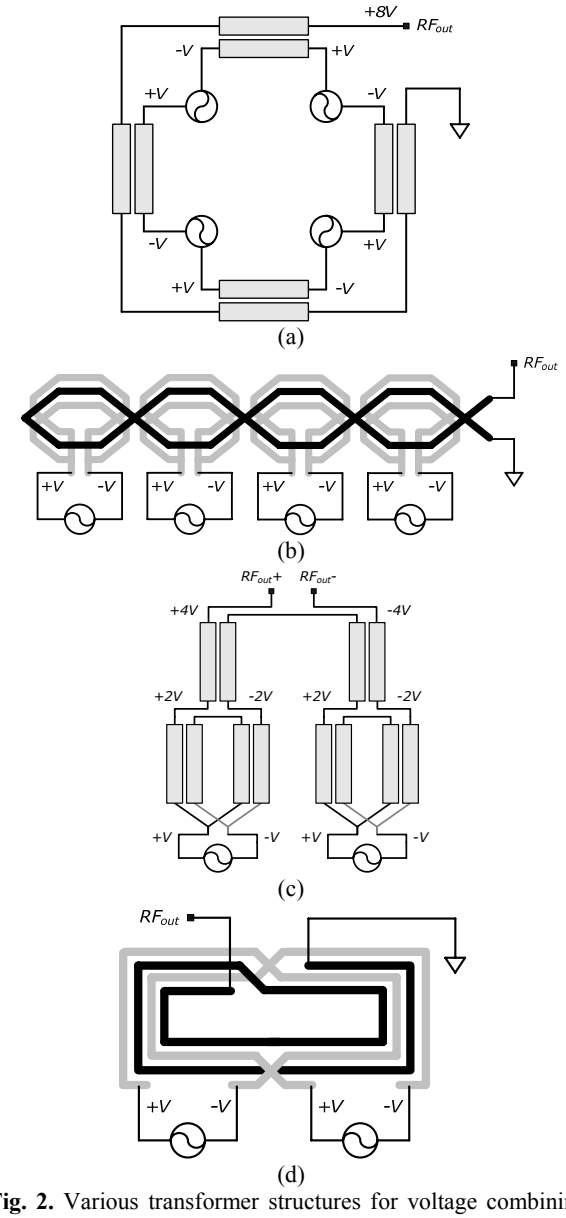


Fig. 2. Various transformer structures for voltage combining. (a) distributed active transformer [1], (b) figure '8' transformer [2], (c) tournament-shaped power combiner [3], (d) power combining transformer [4].

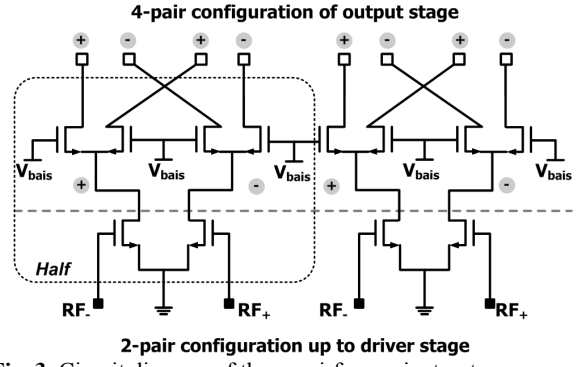


Fig. 3. Circuit diagram of the quasi-four-pair structure.

3. Improving Efficiency in the Low Power Region

Two characteristics should be considered in PAs for polar transmitters. Dynamic range of the output power should be achieved with a given range of supply voltage. Efficiency in the low output power region is also important. Usually, efficiency is fairly high near maximum output power, but low at low output power.

To increase efficiency in the low power region, dual-mode PA architectures have been proposed [6-8].

In the stage-convertible PA [6] (Fig. 4), a driver stage functions as a driver amplifier of a power stage in high power mode. The power generated in the power stage is much higher than in the driver stage, thus most power is generated in the power stage in the high power mode. In the low power mode, the driver stage functions as the power stage because the power stage is turned off and the output power of the driver stage is transmitted to a power combiner. The efficiency could be increased because dc power loss in the power stage is eliminated when the PA operates in low power mode.

When the PA operates in high power mode, the maximum output power is 32 dBm and PAE is 40% (Fig. 5). Theoretically, the dynamic range of a conventional class-E amplifier is ~ 16.4 dB, while the supply voltage varies from 0.5 to 3.3 V. However, in the stage-convertible PA, the dynamic range of the high-power mode is extended to nearly 20 dB, because the input power of the power stage also decreases when that of the driver stage decreases. To activate the low-power mode, the power stage is turned off by an external signal. Due to the high load impedance of the low-power mode, the efficiency in a low output power region is increased. The auto-switching technique [6] is realized using a self-biased cascode structure in the power stage. In the low output power region, the input power of the power stage

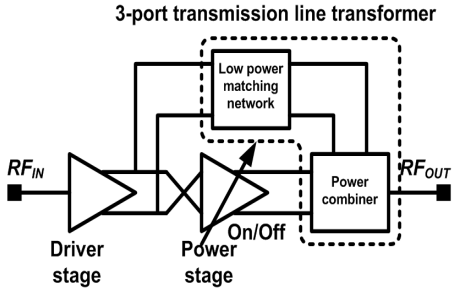


Fig. 4. Stage-convertible structure [6].

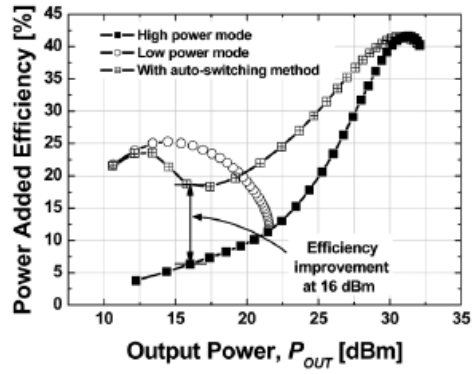


Fig. 5. Measurement results of the stage-convertible structure [6].

is decreased. Therefore, the contribution of the power stage is decreased and the contribution of the driver stage that has a higher load impedance is increased. Thus, the power and driver stages are always turned on. The mode of the PA is changed automatically and smoothly with V_{DD} (Fig. 5). This is due to the self-biased cascode structure of the power stage.

In a dual-primary transformer [7] (Fig. 6), the ports of the inner primary part are connected to a power stage for the high power mode, and the ports of the outer primary part are connected to a driver stage for the low power mode. In the high power mode, if the current I flows from P11 to P12, the current that flows through the secondary part is $I/2$, because it surrounds the primary part. If the output voltage of each PA is $+V$ and $-V$, the voltage drop between RF_{OUT} and ground is $4V$. Thus the impedance transform ratio is 8, because RF_{OUT} is connected to the external 50-Ω load; the equivalent impedance connected with the PA is 6.25 Ω. In the low power mode, the secondary part can be considered as two subcomponents, one that adjoins the outer primary part and the other that is located away from the outer

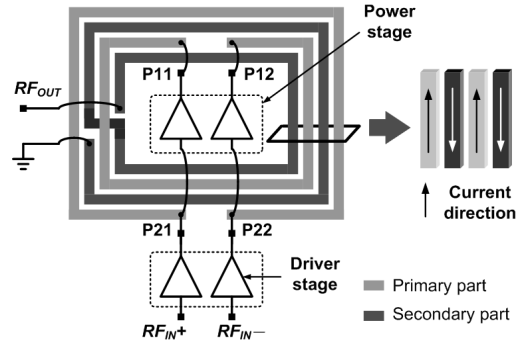


Fig. 6. A dual-primary transformer.

primary part. The magnetic coupling between the primary and secondary parts, which is located away from the outer primary part, is expected to be very weak. If I flows from P21 to P22, the current that flows through the secondary part is almost the same as I, and the voltage drop of RF_{OUT} is $2V$; the equivalent impedance connected with the PA is 25 Ω. Thus, the low power mode and the high power mode have different output impedances. Therefore, the dual-primary transformer can be used to increase the efficiency in the low-power region of a PA. Additionally, the power stage is programmed to be turned on or turned off automatically according to the variable supply voltage. As V_{DD} decreases, the contribution of the power stage to the output power decreases, and the contribution of the driver stage to the output power increases. Thus, the high power mode becomes dominant when V_{DD} is high, and the low power mode becomes dominant when V_{DD} is low.

The efficiency versus output power was measured while a supply voltage varies from 0.5 to 3.3 V (Fig. 7); the mode of the PA changes automatically and smoothly according to the V_{DD}.

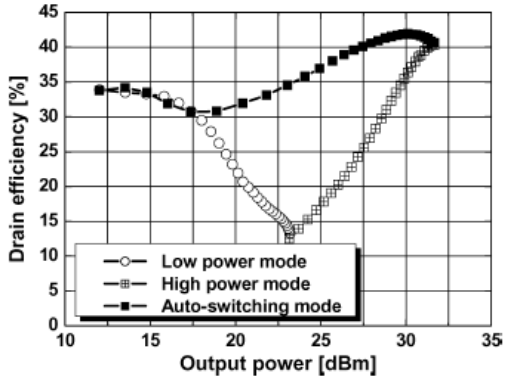


Fig. 7. Measurement results of the power amplifier with a dual-primary transformer [7].

III. CMOS LINEAR POWER AMPLIFIERS

1. Overview of CMOS Linear Power Amplifiers

In contrast with switching mode PAs that operate at saturated output power level, linear PAs operate at back-off power level to insure linear amplifications. The signal of the nonconstant envelope modulation cannot be amplified near the saturated level without serious signal distortion.

The design strategies for CMOS linear PAs are not much different from those used in switching PAs. The cascode structure is used to overcome the low breakdown voltage of CMOS devices, and the differential structure is used to reduce the effects of bonding wires [9].

The major difference is that the trade-off between linearity and efficiency is more severe in linear PAs than in switching mode PAs.

The maximum output power at which the linearity requirements are met is called ‘maximum linear output power’, or simply ‘linear output power’. The linearity requirements are defined as a measure of Adjacent Channel Leakage Ratio, Error Vector Magnitude, or other factors, according to the wireless standards. These measures of linearity are simulated and measured using modulated signals; the spectrum of the WCDMA signal is distorted after amplification (Fig. 8).

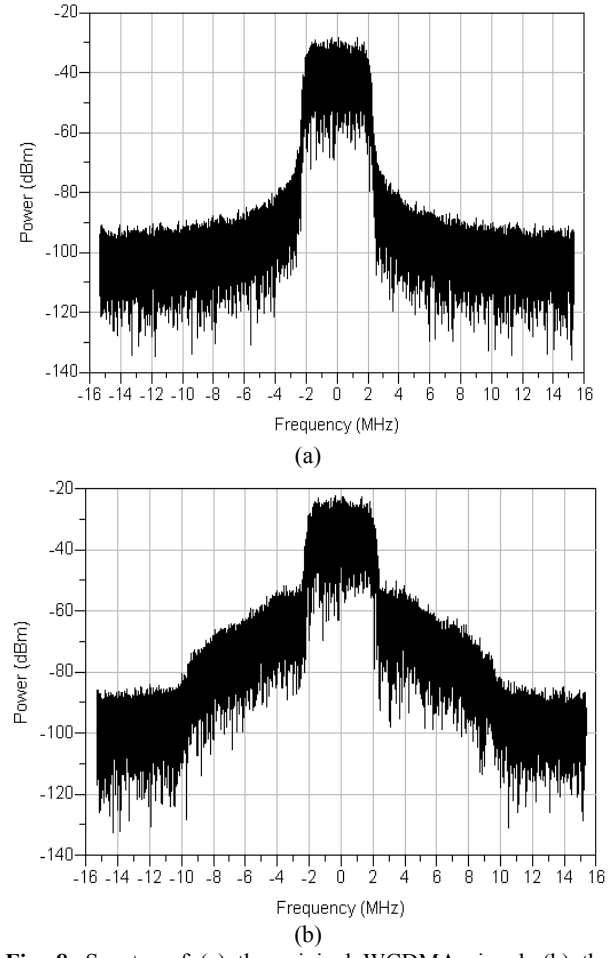


Fig. 8. Spectra of (a) the original WCDMA signal, (b) the distorted signal.

The two-tone measurement is another approach to check the linearity of a PA. The modulated signal is approximated as a two-tone signal whose tone spacing is same with its bandwidth. In two-tone measurement, the third-order intermodulation distortion terms are major concerns.

Meanwhile, the linearity of a PA is related to the dc characteristics of the active device. The cascode structure is used to overcome the low breakdown voltage of CMOS devices, but degrades linearity compared with the common-source structure (Fig. 9). The common-source amplifier has a smaller knee voltage than the cascade structure, and this characteristic is important in maintaining large-signal linearity. However, the common-source amplifier sustains lower supply voltage than the cascode structure.

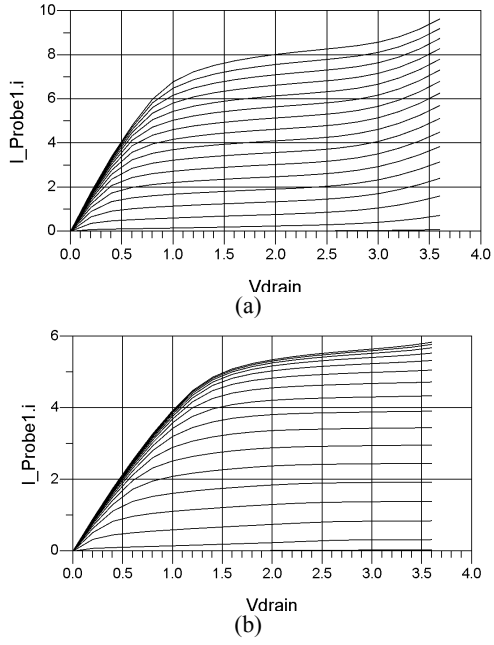


Fig. 9. dc characteristics of (a) common-source structure, (b) cascode structure with the same device size.

2. Linearization Techniques in CMOS Power Amplifiers

Linear PAs for mobile applications can be implemented with modern CMOS technology. CMOS PAs can achieve large output power by using large transistors and by combining the output powers of unit amplifiers. As the size of power transistors increases, the linearity improves at a given power level, but the efficiency decreases.

To increase the maximum linear output power while maintaining good efficiency, linearization techniques have been developed. PAs with these linearization techniques can use smaller transistors for the same output power, thus satisfying linearity requirements and improving the efficiency at the maximum linear output power. The linearization techniques of CMOS PAs are categorized as either device-level, circuit-level, or system-level.

1) Device-level linearization : An RF PA is a large-signal circuit, which means that the input signal cannot be regarded as a small perturbation around a given bias point. Therefore, the circuit parameters change according to input power. Among the circuit parameters, the input capacitance has a major effect on the linearity of large-signal circuits. The deep n-well structure of NMOS reduces distortions caused by nonconstant gate-source capacitance [10]. Also, capacitance compensation using a PMOS device is widely used in CMOS PAs [11, 12]. The gate-source capacitance of PMOS has the opposite slope to that of NMOS with repect to the gate bias. Therefore, connecting the gate of PMOS to the gate of NMOS compensates for the variation of gate-source capacitance of NMOS, and makes the total input capacitance constant.

One of the most effective ways to increase the large signal linearity of a CMOS PA is to use the back gate effect. The threshold voltage change of the power transistor due to the body effect by both input RF signal and envelope signal enlarges the linear amplification region (Fig. 10).

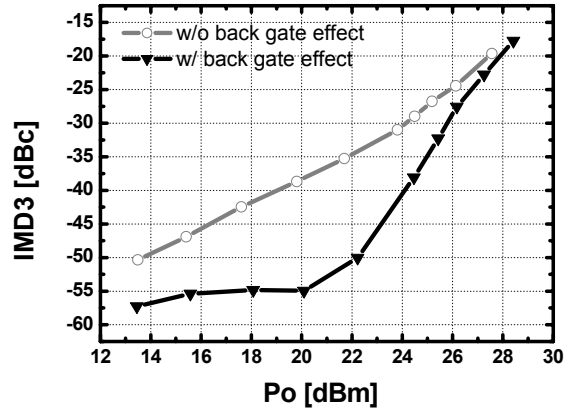


Fig. 10. The measured intermodulation distortion of a power amplifier with and without the back gate effect.

2) Circuit-level linearization : Analysis of CMOS devices [13] led to the design of a PA with second harmonic termination at both drain and source [14, 15]. Series connection of the on-chip capacitor and the bonding wire makes a short path for second harmonics at the drain and source, which reduces distortions.

Parallel sub-amplifiers with different bias conditions can cancel each other's gain/phase variations. This method is widely used. In one proposed design [20], the phase variations of two amplifiers have opposite directions as input power increases. The distortions from the two amplifiers cancel each other, and this minimizes the AM-PM distortion of the PA.

3) System-level linearization : The nonlinear behavior of a PA can also be corrected by system compensation techniques such as feed-forward and predistortion. However, the system-level approach is usually less suitable for PAs in mobile terminals, because it requires several additional blocks including a signal processing component.

3. Efficiency Enhancement Techniques in the Low Power Region

Most of the operation of linear PAs occurs at an output power level that is much less than the maximum linear output power. Therefore, to increase battery lifetime, the efficiency of PAs in the low power region must be improved.

The efficiency of a PA is increased by reducing the dc current in the low power region. Turning off some members of multiple pairs of amplifiers makes the active devices smaller, and hence reduces dc current. Parallel amplification structures have been developed [16-19] (Fig. 11). In these structures, the boundary of the operating mode is important. As input power increases, the next amplifier should be turned on before the linearity characteristic fails to meet the target specification.

The Doherty PA (Fig. 12(a)) is also used to increase low power efficiency. Although the topology has been mainly developed for base station PAs, CMOS Doherty PAs have been designed for use in mobile terminals [20-23]. A Doherty PA consists of carrier/peak amplifiers and quarter-wave transformers. In a CMOS Doherty PA, the quarter-wave transformer and delay line are implemented as lumped element networks to reduce die size. For driving quadrature input signals, various phase shift networks have been designed, including an on-chip quadrature hybrid [20], a delay line [21], and a poly-phase circuit [22].

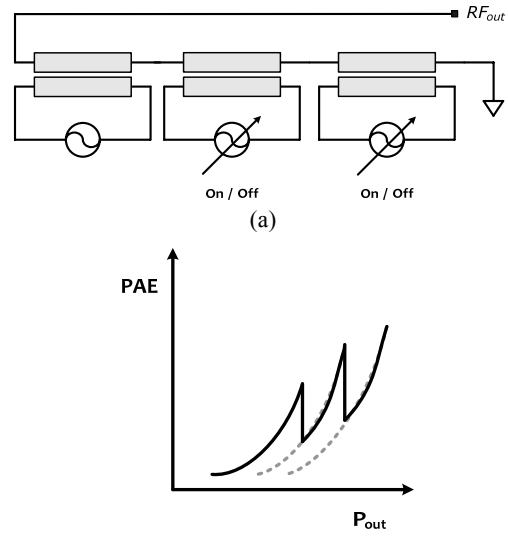


Fig. 11. Power amplifier with parallel amplification. (a) a conceptual diagram, (b) Power-added efficiency (PAE) vs. output power (P_{out}).

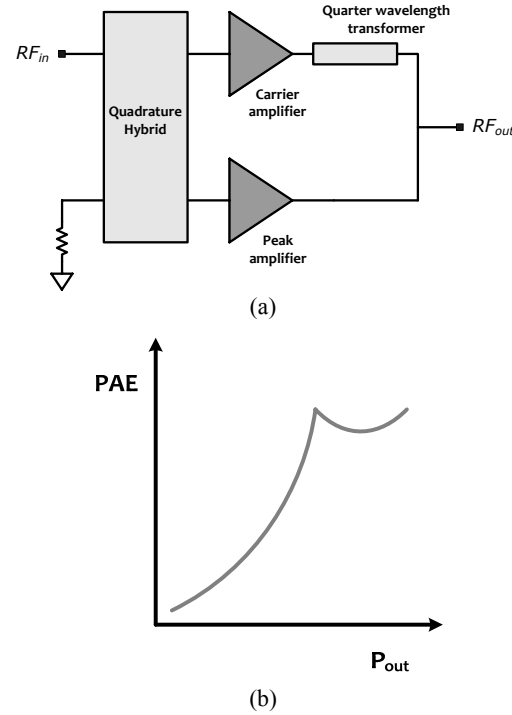


Fig. 12. Doherty power amplifier. (a) a conceptual diagram, (b) Power-added efficiency (PAE) vs. output power (P_{out}).

Usually, in a Doherty PA, the carrier amplifier is biased at class AB, and the peak amplifier is biased at class C. Therefore, the peak amplifier is off in the low power region. The load impedance of the carrier amplifier is twice the optimum impedance so that it reaches saturated output power before the peak amplifier is turned on. Therefore, another peak appears in the back-off region in the efficiency graph (Fig. 12(b)). In the high power mode where the peak amplifier is also on, the load impedances of the carrier and peak amplifiers are changed toward their optimum value according to the magnitude of the current in the peak amplifier.

IV. SUMMARY

Recently, CMOS PAs have been improved to efficiently amplify constant envelope signals. Linearization and power control structure should be applied to implement CMOS linear PAs with reasonable efficiency.

Some obstacles for implementing RF PA using CMOS technology exist. To overcome the low breakdown voltage of CMOS devices, the cascode structure is used. The differential topology compensates for the absence of the via process in CMOS technology. A slab inductor which has low loss should be used in designing the power combiner. Also, transmission line transformers are widely used to combine the output power of multiple pairs of amplifiers.

Although CMOS devices are less linear than other devices, additional functions can be easily integrated with CMOS PAs in the same IC. Therefore, CMOS PAs are expected to have potential applications after various linearity and efficiency enhancement techniques are used.

ACKNOWLEDGMENTS

This work was supported by a Korea Science and Engineering Foundation (KOSEF) grant funded by the Korean Government (MEST) through the Intelligent Radio Engineering Center at Information and Communications University (ICU) in Korea.

REFERENCES

[1] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371-383, Mar. 2002.

[2] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu, and A. M. Niknejad, "A 5.8 GHz 1 V linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1054-1063, May 2008.

[3] C. Park, D. H. Lee, J. Han, and S. Hong, "Tournament-shaped magnetically coupled power-combiner architecture for RF CMOS power amplifier," *IEEE Trans. Microw. Theory Tech*., vol. 55, no. 10, pp. 2034-2042, Oct. 2007.

[4] K. H. An, O. Lee, H. Kim, D. H. Lee, J. Han, K. S. Yang, Y. Kim, J. J. Chang, W. Woo, C.-H. Lee, H. Kim, and J. Laskar, "Power-combining transformer techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064-1075, May 2008.

[5] H. Lee, C. Park, and S. Hong, "A quasi-four-pair class-E CMOS RF power amplifier with an integrated passive device transformer," *IEEE Trans. Microw. Theory Tech*., vol. 57, no. 4, pp. 752-759, Apr. 2009.

[6] C. Park, Y. Kim, H. Kim, and S. Hong, "A 1.9-GHz CMOS power amplifier using three-port asymmetric transmission line transformer for a polar transmitter," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 2, pp. 230-238, Feb. 2007.

[7] C. Park, J. Han, H. Kim, and S. Hong, "A 1.8-GHz CMOS power amplifier using a dual-primary transformer with improved efficiency in the low power region," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no, 4, pp. 782-792, Apr. 2008.

[8] D. H. Lee, C. Park, J. Han, Y. Kim, S. Hong, C.-H. Lee, and J. Laskar, "A load-shared CMOS power amplifier with efficiency boosting at low power mode for polar transmitters," *IEEE Trans. Microw. Theory Tech*., vol. 56, no. 7, pp. 1565-1574, July 2008.

[9] S.-H. Baek, C. Park, and S. Hong, "A fully integrated 5-GHz CMOS power amplifier for IEEE 802.11a WLAN applications," *Journal of Semiconductor Technology and Science*, vol. 7, no. 2, pp. 98-101, June 2007.

[10] J. Kang, D. Yu, Y. Yang, and B. Kim, "Highly

linear 0.18-μm CMOS power amplifier with deep n-well structure," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1073-1080, May 2006.

[11] C. Wang, M. Vaidyanathan, and L. E. Larson, "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1927-1937, Nov. 2004.

[12] C. Lu, A.-V. H. Pham, M. Shaw, and C. Saint, "Linearization of CMOS broadband power amplifiers through combined multigated transistors and capacitance compensation," *IEEE Trans. Microw. Theory Tech*., vol. 55, no, 11, pp. 2320-2328, Nov. 2007.

[13] S. Kang, B. Choi, and B. Kim, "Linearity analysis of CMOS for RF application," *IEEE Trans. Microw. Theory Tech*., vol. 51, no, 3, pp. 972-977, Mar. 2003.

[14] J. Kang, J. Yoon, K. Min, D. Yu, J. Nam, Y. Yang, and B. Kim, "A highly linear and efficient differential CMOS power amplifier with harmonic control," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1314-1322, June 2006.

[15] J. Kang, A. Hajimiri, and B. Kim, "A single-chip linear CMOS power amplifier for 2.4 GHz WLAN," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 208-209.

[16] A. Shirvani, D. K. Su, and B. A. Wooley, "A CMOS RF power amplifier with parallel amplification for efficient power control," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 684-693, June 2002.

[17] P. Reynaert and M. S. J. Steyaert, "A 2.45-GHz 0.13-μm CMOS PA with parallel amplification," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 551-562, Mar. 2007.

[18] G. Liu, P. Haldi, T.-J. K. Liu, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600-609, Mar. 2008.

[19] K. H. Ahn, D. H. Lee, O. Lee, H. Kim, J. Han, W. Kim, C.-H. Lee, H. Kim, and J. Laskar, "A 2.4 GHz fully integrated linear CMOS power amplifier with discrete power control," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 7, pp. 479-481, July 2009.

[20] M. Elmala, J. Paramesh, and K. Soumyanath, "A 90-nm CMOS Doherty power amplifier with minimum AM-PM distortion," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1323-1332, June 2006.

[21] J. Kang, D. Yu, K. Min, and B. Kim, "A ultra-high PAE Doherty amplifier based on 0.13-μm CMOS process," *IEEE Microw. Wireless Compon. Lett*., vol. 16, no. 9, pp. 505-507, Sep. 2006.

[22] N. Wongkomet, L. Tee, and P. R. Gray, "A +31.5 dBm CMOS RF Doherty power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2852-2859, Dec. 2006.

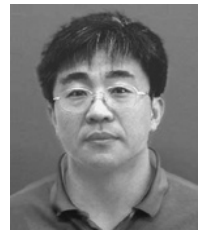
[23] L.-Y. Yang, H.-S. Chen, and Y.-J. E. Chen, "A 2.4 GHz fully integrated cascode-cascade CMOS Doherty power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 3, pp. 197-199, Mar. 2008.

Ki Yong Son received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2005 and 2007, respectively, where he is currently pursuing the Ph.D. degree. His research interests include CMOS power amplifier design for mobile applications.

Bonhoon Koo received the B.S. degree and passed the M.S. degree in electrical engineering in 2006 and 2008, respectively, from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea, where he is currently pursuing the Ph.D. degree. His research interests include CMOS RF amplifiers and transmitter systems.

Yumi Lee received the B.S. degree in electrical engineering and computer science in 2006, from Kyungbook National University, Daegu, Republic of Korea, and the M.S. degree in electrical engineering in 2008 from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea, where she is currently pursuing the Ph.D. degree. Her research interests include CMOS RF amplifiers and transmitter systems.

Hongtak Lee received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea, in 2006 and 2008, respectively, where he is currently pursuing the Ph.D. degree. His research interests include CMOS RF amplifiers and transmitter systems.



Songcheol Hong received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, Republic of Korea, in 1982 and 1984, respectively. He received the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1989. In May 1989, he joined the faculty of Dept. Electrical Engineering and Computer Science at Korea Advanced Institute of Science and Technology (KAIST), in Korea. He held short visiting professorships at Stanford University, Palo Alto and Samsung Microwave Semiconductor, USA in 1997. His research interests are microwave integrated circuits and systems including power amplifiers for mobile communications, miniaturized radar, millimeter-wave frequency synthesizers and novel semiconductor devices.