Power Amplifiers and Transmitters for Next Generation Mobile Handsets

Jinsung Choi, Daehyun Kang, Dongsu Kim, Jungmin Park, Boshi Jin, and Bumman Kim

Abstract—**As a wireless handset deals with multiple application standards concurrently, RF transmitters and power amplifiers are required to be more power efficient and reconfigurable. In this paper, we review the recent advances in the design of the power amplifiers and transmitters. Then, the systematic design approaches to improve the performance with the digital baseband signal processing are introduced for the next generation mobile handset.**

Index Terms—**Transmitters, power amplifiers, CMOS analog integrated circuits, wireless communication**

I. INTRODUCTION

As the recent wireless communication standards such as mobile-WiMax and 3GPP long-term evolution (LTE) employ the orthogonal frequency-division multiplexing (OFDM) technique for spectral efficiency, the handset power amplifiers have to accommodate higher peak-to-average power ratio (PAPR) than present standards, such as EDGE, CDMA, and WCDMA. To amplify the high PAPR signals, the general class-AB power amplifier operates at a large backed-off power region, where the efficiency is very low. Thus, there have been many researches to improve the efficiency at those region [1- 26].

At the same time, due to the relentless cost pressure of the modern consumer market, wireless industry is pushing more functions to be integrated into a single mobile unit. As the power amplifier is co-integrated with other portions of the transceiver, the significant performance improvement can be achieved by utilizing the baseband signal processing. For its low cost and high level of integration availability, CMOS becomes an elusive goal.

This paper reviews the recent researches on the RF power amplifiers and transmitters. Section II shows the power amplifier research trends and describes the enhanced design techniques. In Section III, the systematic design approaches integrating the transmitter architecture into a design consideration of the power amplifiers for high efficiency and high level of integration are presented. Section IV provides some challenges remained for the design of the power transmitters.

II. RECENT RESEARCH TRENDS FOR RF PAS AND TRANSMITTERS

The recent research results on RF PAs and transmitters are listed in Fig. 1. (Many other important research publications are omitted in here only due to the limited space.) Based on this table, we found that the RF PAs in CMOS technologies are very hot issue and close to the realization in market. The difficulty in generating high output power on a lossy substrate is almost solved, and the linear amplification with high efficiency is already available for some applications [2, 11, 15, 23]. Also, there have been many efforts to improve efficiency of the PA at a low power region. The technology direction of the RF PAs is illustrated in Fig. 2. In [1, 2, 20], they utilize different size of power cells for a low power region and high power region. At the low power region, the small size power cell generates the low output power with the high load impedance, resulting in high efficiency at the low power region. At the high power

Manuscript received Aug. 1, 2009; revised Sep. 26, 2009.
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Year	Ref.	Techniques	Technologies	Application	Pout	PAE	Gain	Etc
2005	[1]	Device switching	SiGe HBT	WCDMA	25.9	31	6	8%@0dBm
2005	[2]	EER	CMOS	GSM/EDGE	23.8	22		EVM=1.7%
2006	[3]	Device switching	SiGe HBT	WCDMA	26	27	18.5	5%@0dBm
2006	[4]	Doherty	GaAs HBT	WLAN	22.5	21.3	21.5	
2006	[5]	Class-AB	CMOS	1-tone	20.2	18.9	35	
2007	[6]	Class-AB,pre-distortion	GaAs HBT	WCDMA	26.8	50		Iq=20mA
2007	[7]	Doherty + Average bias tracking	GaAs HBT	CDMA	28	43.3	28	29.2%@16dBm
2007	[8]	Average bias tracking	CMOS+HBT	WCDMA	25			13.67%@0dBm
2007	[9]	Class-AB	GaAs HBT	CDMA	28	42	26.7	2.4V operation
2007	[10]	Envelopetracking	SiGe BiCMOS	WLAN	20	28	11	off-chip DPD
2008	[11]	Load-shared PA (DA at low power)	CMOS	1-tone	32	35.6	30	30%@16dBm
2008	[12]	Average bias tracking	LDMOS-based MOS	1-tone	36.7	60		
2008	[13]	Class-AB/F	GaAs HBT	CDMA	28	38.9	30	
2008	[14]	Envelope tracking	LDMOS-based MOS	WCDMA	27	46		
2008	[15]	Average bias tracking (Power Mixer)	CMOS	WCDMA	25.7	26.5		Bad linearity
2008	[16]	EER	CMOS+HBT	CDMA	28	32		
2008	[17]	Doherty	GaAs HBT	WLAN	24	31.5	26	
2008	[18]	Digitalpre-distortion		Mobile-WiMax				Estimated power overhead for DPD=22mW
2008	[19]	Envelopetracking	CMOS+HBT	WCDMA	28	45		
2008	[20]	Device switching	HBT	CDMA	28	40.5		15.4%@16dBm
2009	[21]	Optimum Doherty	GaAs HBT	WiBro	26	40.2	23	16%@18dBm, 12%@16dBm
2009	[22]	Envelope tracking	CMOS+HBT	EDGE	27.8	45	29.4	
				WCDMA	29	46	27.8	
				Mobile-WiMax	23.9	34.3	27.9	17.5%@18dBm, 13%@16dBm
2009	[23]	Class-AB	CMOS	Mobile-WiMax	22.7	12.4		6%@18dBm, 4%@16dBm
2009	[24]	Envelope tracking Doherty	CMOS+HBT	WiBro	24.2	38.6	24.6	23%@18dBm, 17%@16dBm
2009	[25]	Broadband class-F	HBT	1-tone	30	48	25	Bandwidth=300MHz
2009	[26]	Digital PA	SOI CMOS	EDGE	21.8	38.1		16.4% CDMA average efficiency
				WCDMA	21.7	38.2		
				Mobile-WiMax	15.3	22		

Fig. 1. Recent research publications for RF power amplifiers.

region, the large size power cell generates high output power with the appropriate load impedance. The switching of power cells is performed according to the wanted average output power level. Therefore, this device switching technique improves efficiency of the power amplifier at the low average output power region.

There is another well known technique improving the efficiency at the low average output power region, the average bias tracking technique. In this technique, the base/gate or collector/drain biases of the power amplifier are adjusted according to the average output power level. Usually, the base/gate bias tracking is easily employed for its small power handling characteristic, while the collector/drain bias tracking has a burden for the design of high efficiency power converter. While the device switching technique usually switches between two power cells for the simplicity and low loss, the average bias tracking technique presents continuous improvement according to the average power level. However, these techniques do not increase the efficiency at the high average output power region, unattractive to the high PAPR signals.

To enhance efficiency of the power amplifier for the high PAPR signal, the load modulation and bias tracking techniques according to the instantaneous output power levels have been developed. The device switching technique according to the instantaneous power level is accompanied with the load modulation technique.

At the low output power region, the carrier power cell sees the high load impedance of $2R_{opt}$ and generates output power of $P_{out}/4$ with high efficiency. As the power increases, the peaking power cell starts to be turned on and generates output power. At the same time, the load

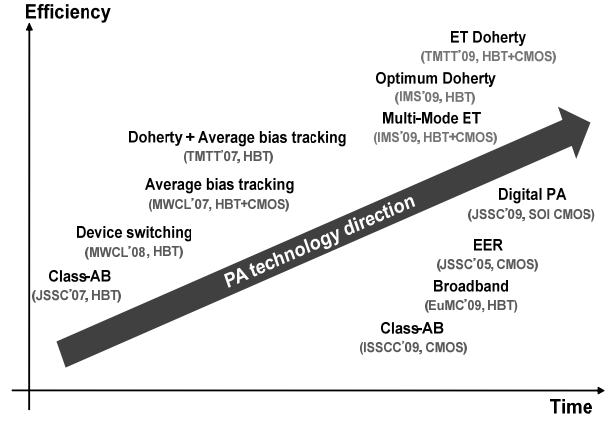

Fig. 2. Recent PA technology direction based on Fig. 1.

impedance seen by the carrier power cell is reduced. At the maximum output power, finally, both the carrier and peaking power cells see the same load impedance of R_{opt} and generate the same output power of $P_{out}/2$. It is described in Fig. 3. As the load modulation occurs according to the instantaneous input power level, it presents very high efficiency for the high PAPR signals. The amplifier employing this kind of load modulation technique is named Doherty amplifier after its inventor. In the early design stage of Doherty amplifier, the output matching network for the load modulation is realized with off-chip lumped elements, resulting in high cost and large size [7]. Recently, there are some advances integrating overall matching network on a chip [4], enhancing the efficiency of each power cell with a harmonic tuned load [17], and optimizing the load modulation characteristic with an optimum input power dividing [21]. One of the remaining important issues for the Doherty amplifier is the wideband operation. It is very difficult because the load modulation is performed by the frequency-dependent transmission line.

The instantaneous bias tracking of the power amplifier is usually performed by modulating the supply voltage of the power amplifier, and it is called as polar modulator. In the polar modulator, I/Q signals are converted to the envelope and phase signal, and the RF up-converted phase signal is applied to the input of the power amplifier while the envelope signal is applied to the supply of the power amplifier. That is, the envelope and phase information are combined at the power amplifier as shown in Fig. 4-(a). For its envelope-less (constant envelope) characteristic of the RF up-converted phase signal, the power amplifier operates in a saturated region so that the high efficiency is achieved with assumption of highly efficient supply modulator.

The high efficiency supply modulator is the key element in the design of the polar modulator. However, its design is very difficult for its trade-off relationship between the linearity and the efficiency. The wideband linear modulator presents low efficiency, while the high efficiency switching modulator has the limited bandwidth and the switching ripple at the output. Recently, many researchers have tried to combine the advantage of two modulators, the hybrid switching amplifier [10, 16].

In the hybrid switching amplifier, the linear modulator acts as an independent voltage source, while the switching modulator works as a dependent current source. The current flowing from the linear modulator is sensed, and the switching state of the switching modulator is determined according to the magnitude and the polarity of the sensed current. As most of the current is provided by the highly efficient switching modulator, it shows very high efficiency with a good linearity and wide bandwidth, which are achieved by the wideband linear modulator. As the operation of the supply modulator is independent of the operating radio frequency of the power amplifier, it is very promising solution for the multi-mode/multi-band transmitter.

Even its high efficiency and reconfigurability, however, there are some technology-limited factors in the design of the polar modulator architecture. First, the CORDIC processor converting I/Q signal to the polar signal consumes too much power for the wide bandwidth signal, so the benefit coming from the polar modulated power amplifier is lost. Moreover, the limited loop bandwidth of the phase-locked loop (PLL), which is used to up-convert the phase signal with low phase noise, is not available for wide bandwidth signals. There is another nonlinearity-related issue in the polar modulator architecture. Even at the small envelope signal, the input power level of the power amplifier is still optimized for the highest envelope level, so that there is a power leakage at the output. It degrades the linearity of the power amplifier and the additional power consuming pre-distortion technique is required.

The increasing bandwidth of the communication standards requests the wideband phase modulator, and there have been many researches on them [27-30]. However, their bandwidth are still limited up to a few MHz while the bandwidth of the phase information is more than 100 MHz for the 10 MHz OFDM signals, so that the traditional I/Q modulator is recently employed again for RF up- conversion

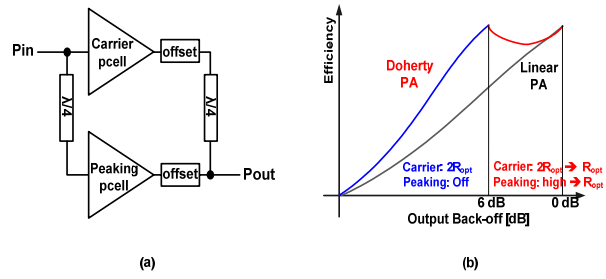

Fig. 3. (a) Block diagram of Doherty PA and (b) operation principle.

[31]. Then, instead of decomposing the signal into the envelope and the phase using the power hungry CORDIC processor, the simple envelope detector is used and the I/Q signals are up-converted as usual. The input of the power amplifier is not a constant envelope signal any more, so that the linear power amplifier is required. In [13], the class-AB/F power amplifier is introduced for high efficiency and linearity. It employs the harmonic-tuned load for efficiency enhancement and the class-AB bias is used for the linearity. In [22], the polar transmitter employing the I/Q modulator and the class-AB/F power amplifier is presented, whose block diagram is shown in Fig. 4-(b). To avoid the nonlinear distortion below the knee region, the envelope signal is shaped. They also introduce a new hybrid switching amplifier enabling the multi-mode RF transmitter. The operation of the multi-mode supply modulator is based on the programmable hysteretic com-parator, whose hysteresis window size is proportional to the signal bandwidth. It achieves the highest efficiencies ever reported for EDGE/WCDMA/

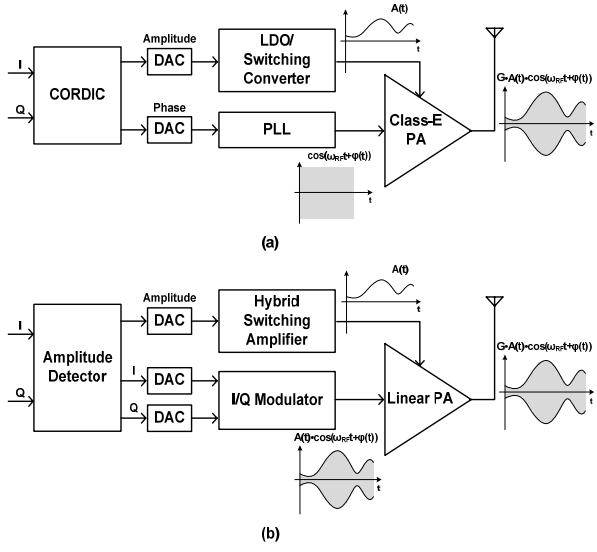

Fig. 4. Block diagram of (a) conventional polar transmitter and (b) advanced polar transmitter – envelope tracking PA [22].

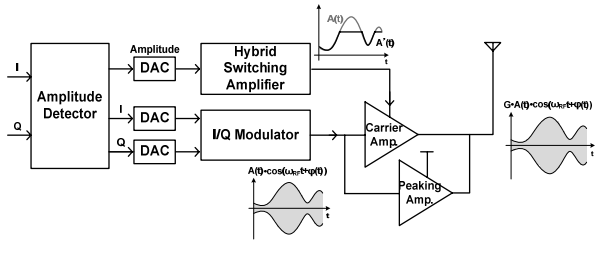

Fig. 5. Block diagram of envelope tracking Doherty PA [24].

Mobile-WiMax with good linearity. In [24], they extend the application of the bias tracking technique to the Doherty amplifier as shown in Fig. 5, and achieve very high efficiency at the broad output power region.

III. Systematic Design Approaches of RF Power Transmitters

As mentioned before, the traditional polar transmitter has a difficulty in wideband operation, so the I/Q based approach is widely employed. However, although the conventional I/Q modulator based transmitter presents the wide bandwidth capability, the wide dynamic range, and the low noise characteristic even at the receiver band [31], it consists of many analog/RF circuits whose portion is only 20% of the overall SoC area. It requires additional mask and layers and results in high cost. Moreover, the analog/RF circuits should be re-designed for every process, which is very time and energy consuming work considering the recent fast design cycle. As a result, there are many movements to the digital-RF transmitter, and the RFDAC-based transmitter is very attractive. It extends the concept of the DAC to the RF region by dividing the conventional Gilbert mixer into the multiple mixing cells, whose inputs are digital bits representing the baseband signal. In each mixing cell, the 1 bit data pulse stream is up-converted to RF by LO signals. Compared to the general high speed DAC, it has an advantage of clock jitter masking; in every transition edge of the data, the LO voltage is lower than the threshold voltage, so that the mixing cell is turned off. Thus, the jitter in the clocked data does not show up at the output of mixing cells. In [33], the 10 bit I/Q signals are segmented into 6 bit MSBs and 4 bit LSBs to reduce the number of unit cells from 1023 to 78. It enhances the matching property between cells and reduces the LO driving power. The characteristic of the analog/RF and digital-RF transmitter is summarized in Fig. 6.

In [34], the residue amplification technique is used to compensate the quantization noise, and this architecture significantly reduce the number of mixing cells, while there is one linear path always turned on. Moreover, by increasing the size of current source of each cell, the mixing DAC itself generates Watt-level output power in a standard digital CMOS technology. In [26], the digital polar power amplifier in Silicon-on-Insulator CMOS

	I/Q Modulator	Closed loop polar Tx	Mixing DAC	Digital polar PA
TX Chain	DAC, BB filter, BB VGA, Mixer, Frequency synthesizer, RF VGA, PA	DAC, BB filter, Supply modulator, Frequency synthesizer, RF VGA, PA	Frequency synthesizer & Mixing DAC, PA	DAC, Frequency synthesizer, RF VGA, multiple PA cells
Noise (RX band noise, DAC sampling noise, external digital spurs)	BB filter & frequency synthesizer	BB filter & frequency synthesizer, limited to narrow BW (EDGE)	Digital filter & high resolution bits	High resolution bits, but no solution to sampling noise
Dynamic Range	BB & RF VGA	Supply modulator & RF VGA	Bias current of mixing DAC	PA cell on/off & RF VGA
Bandwidth	Good	Poor (by PLL BW)	Good	Poor (by PLL BW)
Power Efficiency	Not bad	Good	Depend on coding	Good for PA itself, But overall efficiency depends on coding
Reconfigurability	Complex analog tuning circuits	More flexible but still analog tuning circuits	Easily reconfigurable with digital functions	Easily reconfigurable with digital functions

Fig. 6. Summary of analog/RF and digital-RF transmitter [26, 31-33].

technology is introduced. The high efficiency is achieved by turning on and off unit PA cells according to the instantaneous wanted output power level. To reduce the complexity and power loss, the 10 bit envelope signal is segmented into 7 bit MSBs and 3 bit LSBs, and MSBs are thermometer-coded while the LSBs are binary-coded, resulting in total 130 unit PA cells.

Now, as presented in Fig. 7, power amplifiers are co-integrated with transmitters, and the significant performance improvement is achieved by utilizing the digital baseband signal processing. These digitally-assisted architectures simplify the complex transmitter chain through the digital function, and can be easily reconfigurable for any kinds of signals such as EDGE, WCDMA and WiMax.

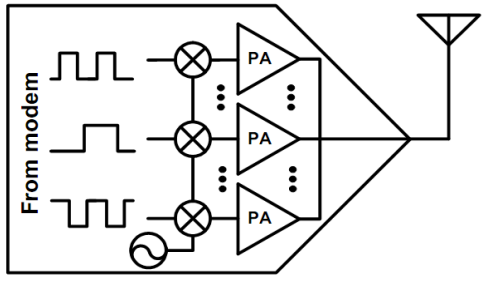

Fig. 7. All digital transmitter architecture.

IV. CHALLENGES

While the digital-RF power transmitter has achieved the goal in efficiency very fast, there are some remaining issues for the linearity. The in-band linearity is achieved by increasing the number of bits and the experimental results in [26,33,34] show very good in-band signal-to-noise ratio (SNR). However, the clock-based design of the digital-RF system generates a lot of digital spur and sampling noise at the out-of-band. The digital noise can be filtered out with the frequency specific RF filter, but it is not an appropriate choice for the multi-mode and multi-band transmitter. Therefore, that filter should be also reconfigurable and the digital-like approach is encouraged.

Also, to realize the multi-mode/multi-band transmitter, the power amplifier should support multiple frequency bands from 800 MHz to 3 GHz for various wireless communication systems. It is very difficult to achieve such a broad bandwidth with high gain and efficiency. Recently, [25] have achieved 300 MHz bandwidth for the class-F topology in GaAs HBT technology, and [35] presents more than 30% efficiency over 3 GHz bandwidth through the transformer-based output matching in SiGe HBT technology.

V. CONCLUSIONS

This paper reviews the recent research on power amplifiers and transmitters, and explores the systematic design approach for the enhance performance of the power transmitter through the digital baseband signal processing. The digital-RF power transmitter on a digital CMOS technology is easily reconfigurable and enables the multi-mode operation. Moreover, it integrates the power amplifier into the transmitter, and all-digital power transmitter with high efficiency can be achieved. There are some challenges for the realization; the out-of-band noise and the broadband power amplifier.

ACKNOWLEDGMENTS

This work was supported by the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korean government (MOST) (No. R01-2007-000-20377-0). This research was supported by the Ministry of Knowledge Economy, Korea, under the ITRC (Information Technology Research Center) support program supervised by the IITA (Institute of Information Technology Advancement) (IITA-2009-C1090-0902-0037).

This work was sponsored by ETRI SoC Industry Promotion Center, Human Resource Development Project for IT SoC Architect.

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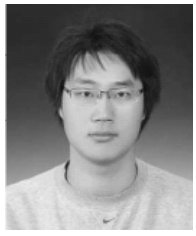

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