Introduction to Industrial Applications of Low Power Design Methodologies

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Abstract—**Moore's law has driven silicon technology scale down aggressively, and it results in significant increase of leakage current on nano-meter scale CMOS. Especially, in mobile devices, leakage current has been one of designers' main concerns, and thus many studies have introduced low power methodologies. However, there are few studies to minimize implementation cost in the mixed use of the methodologies to the best of our knowledge. In this paper, we introduce industrial applications of low power design methodologies for the decrease of leakage current. We focus on the design cost reduction of power gating and reverse body bias when used together. Also, we present voltage scale as an alternative to reverse body bias. To sustain gate leakage current, we discuss the adoption of high-κ metal gate, which cuts gate leakage current by a factor of 10 in 32 nm CMOS technology. A 45 nm mobile SoC is shown as the case study of the mixed use of low power methodologies.**

Index Terms—**Power gating, reverse body bias, hig h-κ metal gate, low power, leakage current**

I. INTRODUCTION

With successive technology scaling, device feature sizes and supply voltage have shrunk to improve manufacturing cost and power of VLSI circuits. Whereas dynamic power has been reduced due to the supply voltage decrease, leakage current has steeply increased due to threshold voltage (shortly V_t) and feature size scaling down. Hence, leakage current is accepted as a major source in total power dissipation [1], and it is a key to achieve low power design, especially for mobile applications.

Leakage current comprises of different components and mechanisms [2], and thereby different approaches have been proposed to manage leakage current. Industries have preferred the use of multiple low power methodologies [3-5] due to the limit of the exclusive use. For instance, power gating is widely accepted to reduce subthreshold leakage current in idle state of a circuit. However, it gives only little leakage saving when software and input data make a circuit have idle periods shorter than the breakeven time of power gating, which means that there is no chance to cut off leakage current by power gating. Reverse body bias helps to reduce leakage current for the case while it reduces wide spread of leakage current due to process variation across the entire manufactured chips. However, the use of multiple low power methodologies requires large design and area overheads. Moreover, the mixed use can induce another leakage current path; hence it can give smaller improvement of leakage reduction compared to its cost increase. This naturally calls for the reduction of adoption cost in each methodology without compromising the extent of leakage saving.

In this paper, we present the industrial adoption of low power methodologies with a very low overhead. We propose physical design methodologies to reduce area overhead for power gating and reverse body bias followed by silicon measurement results. Also, we discuss control

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method in the mixed use of power gating and reverse body bias to maximize leakage reduction efficacy. Adaptive voltage scaling can be a substitute for reverse body bias, and we compare effect and cost of it to reverse body bias in silicon. Gate tunneling leakage current is known as a dominant component in ultra thin gate-oxide devices, and thus we introduce high-κ metal gate which gives thinner EOT despite of larger physical thickness in 32 nm CMOS technology. We present a case study of 45 nm commercial mobile SoC which utilizes multiple low power methodologies to minimize total power dissipation. The adoption and the verification of low power methodologies are introduced.

II. POWER GATING

1. Concept and Approach

Power gating is one of prominent low power methodologies to reduce idle leakage current and it is widely adopted in industries [3–7]. A power gated circuit is composed of logic block and current switch. pMOS current switch (called header) gates V_{dd} of logic block, and it is turned off to reduce idle leakage current whenever a circuit is expected to be idle in long period. nMOS current switch (called footer) gates V_{ss} of logic block in idle period.

Fig. 1(a) shows a power gated block using header. In a logic block, pMOS and nMOS bodies are connected to virtual V_{dd} (denoted by V_{ddv}) and V_{ss} respectively while body of header is tied to V_{dd}. Since pMOS of header and a logic block have different body potential, there is guaranteed to be enough room between header and logic block for body isolation. P-type bulk is used in our low power CMOS technologies thereby separate n-type well for header enables pMOS body isolation, whereas all nMOS share p-type bulk as common body. Fig. 1(b) shows a power gated circuit using footer. In here, body of all nMOS including footer is connected to V_{ss} because body isolation of footer requires additional mask and manufacturing cost for triple well. Since virtual V_{ss} (shortly V_{ssv}) has positive potential due to voltage drop at footer, logic block experiences speed decrease by reverse bias between its source and body [8].

In physical design, current switch is implemented in multiple instances of small current switch because single large current switch is significant placement burden for

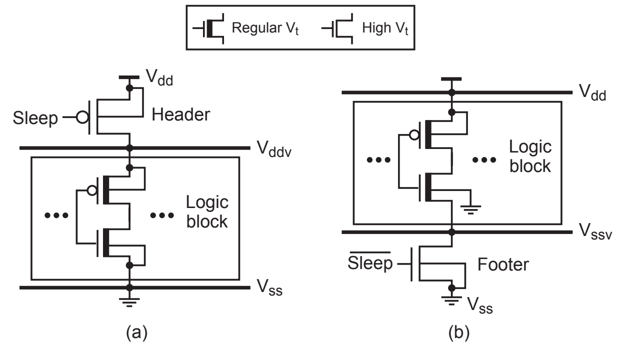


Fig. 1. Power gated blocks using (a) header and (b) footer.

logic cells. Furthermore, it relieves potential fluctuation in virtual power network when multiple switches are distributed over entire logic block. When using header, header cells are placed around logic block with room for the body isolation as denoted by A in Fig. 2. This ring-type placement of header cells enables to adopt power gating in a macro block, and also minimizes placement overhead of a logic block. V_{dd} ring is placed on top of header ring, and it can be connected to V_{dd} pins of header cells without additional routing resource. Since a cell in the middle of logic block has long current path from V_{dd}, it can experience large amount of voltage drop, and thus periodic placement of V_{ddv} strap is required. When using footer, footer cells are evenly distributed across the entire logic block in the array form because it does not require body isolation between logic and footer.

In the wakeup of a power gated block, if all current switches are turned on at the same moment, large saturation current appears through the current switches, and thus it results in large IR drop on top-level V_{dd} networks. Hence, turn-on sequence of header is controlled to sustain turn-on peak current under certain level. Fig. 3(a) illustrates proposed sleep signal network for the peak current management. A part of headers are connected in the form of daisy chain, and thus those headers are turned on one by one. The number of headers in the part is decided by target peak current. This connection sustains turn-on peak current and requires only small design overhead. Other headers are also connected in daisy connection because daisy chain needs smaller routing resource compared to other type connections. Sleep out from last header is used to detect design and manufacturing faults in sleep signal network. Fig. 3(b) illustrates wakeup control of headers. After Sleep pre is de-asserted, the first part of headers starts to

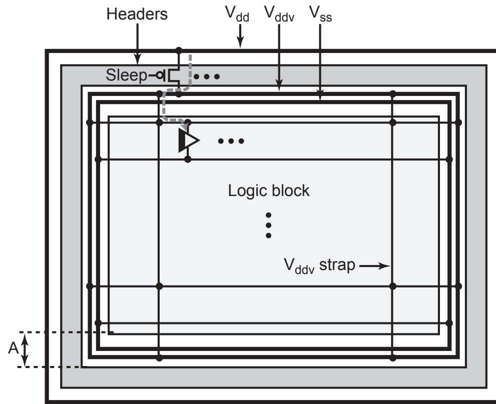


Fig. 2. Power network architecture with header.

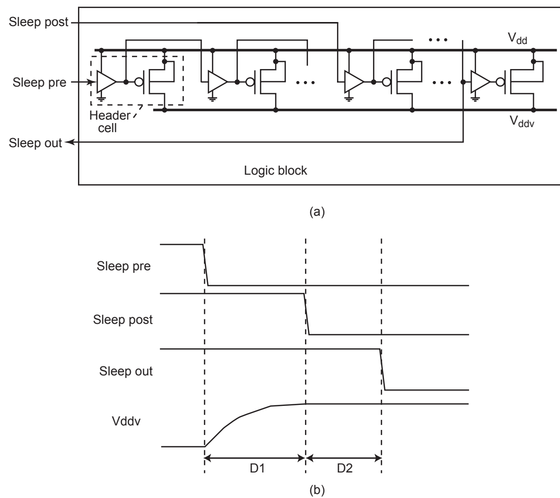


Fig. 3. (a) Sleep signal network for header and (b) its control signals.

be turned on, and then V_{ddv} begins to be restored to V_{dd}. After D1, the other part is turned on. D2 indicates the propagation time of Sleep post. Wakeup delay is defined as sum of D1 and D2.

SRAM for power gating has its internal current switch and separate virtual power network. Since a block can include tens of internal SRAM modules, separate control of internal logic and SRAM relieves engineering cost for sleep signal network. To prevent short circuit current by floated nets [8], isolation cells are inserted at the all output ports of SRAM. When a block goes to sleep mode, SRAM modules are turned off prior to logic part. If a block is required for computation again, a logic part is turned on prior to SRAM modules.

2. Measured Results

To see the standby leakage reduction by power gating, we adopted it to test vehicle in 65 nm low power CMOS technology. The vehicle comprises of CPU core, which handles instructions via eight pipelines at 533 MHz speed, and eight functional blocks, and thus the total number of gate is about 18M cells. The footprint of the SoC is 6950 × 6450 μm^2.

Total leakage current without power gating scheme is 67.8 mA. Power gating was successfully applied to CPU core and each functional block, and thus we can manage leakage current of each block depending on application requirement. This block-level power gating gives more chance to reduce leakage current. When CPU core is power gated in sleep mode, total leakage current decreases by 55.0 mA (decrease by 81%). When the SoC decodes audio files, only CPU core is used, and total leakage current can be cut by 4.7 mA using power gating (decrease by 7%).

III. REVERSE BODY BIASING

1. Concept and Approach

In scaled technologies under 90 nm, variation in transistor parameters results in significant V_t variation, and thus wide spreads of speed and leakage current are observed [9]. Since considerable portion of total chips may be discarded by large leakage current or slow speed, the V_t variation reduces parametric yield. To reduce the yield drop, post-silicon tuning methods, which change speed and leakage current in silicon, have been widely adopted.

Reverse body bias (shortly RBB) [3, 4] is one of efficient post-silicon tuning methods to control active leakage current. Since V_t of transistor is a function of voltage difference between its body and source, reverse body bias reduces leakage current of transistor. Once a chip is measured to detect its leakage current, proper reverse body bias is decided and it is applied to a chip.

Fig. 4 illustrates RBB scheme [10, 11] to manage leakage variation of pMOS. Body bias controller drives body of logic block and memory block. It contains programmable low drop-out and band-gap reference source to reduce supply noise propagation. Lookup table is additionally used to record body bias value for each block. In electrical die sorting step of chips, test instrument measures leakage current of chips, and writes

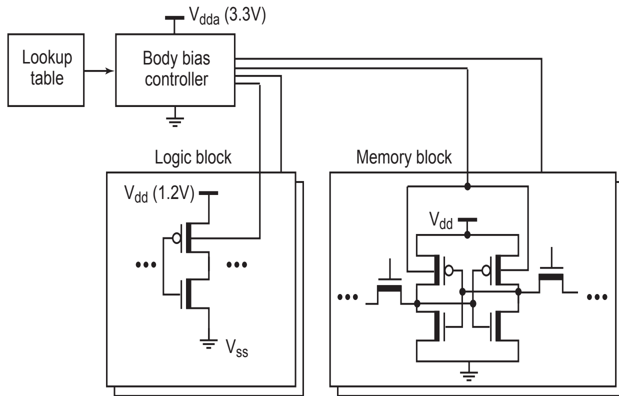


Fig. 4. pMOS body bias control.

proper body bias value into lookup table in one-hot coding in each chip. This post-silicon tuning reduces area overhead by on-chip process monitoring circuits at the cost of silicon test. Process monitor [12] is implemented to see V_t shift in 45 nm low power CMOS technology, and its footprint is 264 × 119 μm^2, which equals to 46K instances of 2-input nand gate. Furthermore, process monitor is to be placed in several locations to compensate on-chip variation effect. Non-volatile memory such as e-fuse or one-time programmable is required to implement lookup table.

In a logic block, standard cells have no pMOS body contact, and instead tap cells are regularly placed for body bias [3]. pMOS body network is built by connecting all tap cells together. Since total body leakage of millions of gates can reach to milli-ampere order by reverse junction leakage current, body network requires IR drop analysis. Area overhead of RBB is estimated in 65 nm low power technology. Body bias controller has size of 381 × 225 μm^2, and it can drive a block of 4M cells. When e-fuse is adopted for lookup table, it occupies area of 75.840 × 10.105 μm^2. Also body network occupies signal routing resource and thus it increases wirelength up to 1.3% in routing congested blocks. In an example of a circuit which is composed of 10M cells and has footprint of 5 × 5 mm^2, RBB is expected to increase area by up to 2.2%. The area overhead is dominated by three body bias controllers and routing congestion.

When RBB is applied to a power gated block, leakage current in sleep mode can significantly increase due to reverse junction leakage current as shown in Fig. 5. In a power gated block of sleep mode, header is a major leakage source. If header has RBB in sleep mode, it has less subthreshold leakage current due to V_t increase. However, enlarged reverse junction leakage current in header and logic block exceeds the subthreshold leakage decrease. To see power gating efficacy decrease, we selected c7552 as a test vehicle. c7552 is one of combinational circuits in ISCAS'85 benchmarks, and it comprises of 1389 regular V_t cells. Leakage saving is one of important factor to show efficacy of power gating, and it is calculated by dividing idle state leakage current with sleep-mode leakage current. As clear in Fig. 6, leakage current saving drops from 22.3 to 12.7 times depending on body bias. Hence, zero body bias is preferred for leakage saving in sleep mode of a power gated block. When a logic block is required for computation again, header is turned on and body bias controller starts to generate body bias. Until body bias is ready, power management unit prohibits the usage of the logic block. The rump-up time for proposed body bias controller is 40 μsec in the worst condition.

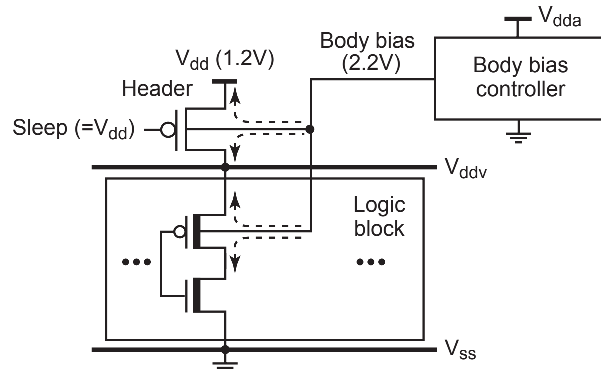


Fig. 5. Body leakage current of a power gated block in sleep mode.

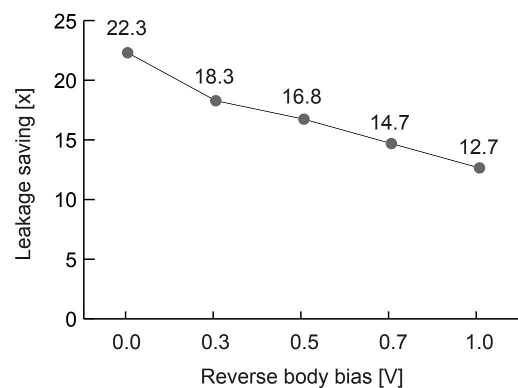


Fig. 6. Leakage saving of power gating in different reverse body biases.

2. Measured Results

32-bit mobile SoC in 65 nm low power CMOS technology was used as a test vehicle to show the effect of RBB on leakage current. The SoC contains 32-bit CPU core of 580 MHz target speed, and it provides various I/O and external memory connectivity. The SoC comprises of total 5.9M cells and target leakage current spec is 23 mA. For RBB in pMOS, the body bias controller and lookup table are integrated into the SoC as shown in Fig. 4. In CPU core, internal cache is not driven by body bias controller, hence we reduces leakage current of only logic cells using RBB. For peripherals, logic cells and internal memories are connected by the single body bias network, and further leakage saving is expected.

To see the efficacy of RBB, we configured the lookup table in the body bias controller for different body bias values, and then we measured speed and leakage of circuits in a wafer. Both items were measured in 25 °C by electrical die sorting equipment. Fig. 7 shows leakage and speed reductions in CPU core by body biases of -1.0 V and -0.5 V. Average leakage reduction by -1.0 V body bias is 10.6% at the cost of speed reduction by 2.5%. The maximum leakage reduction is 13.4%. When body bias is -0.5 V, average leakage and speed reductions are 6.9% and 1.7% respectively. By selectively applying reverse body bias, we can sustain leakage current under a certain level. In our design goal, RBB increases the number of good dies by 9.9%.

Fig. 8 shows leakage current profiles fitted in normal distribution curve for CPU core and top-level block. In top level, which means all digital parts except but CPU core, leakage reduction is 24.5% by body bias of -1.0 V.

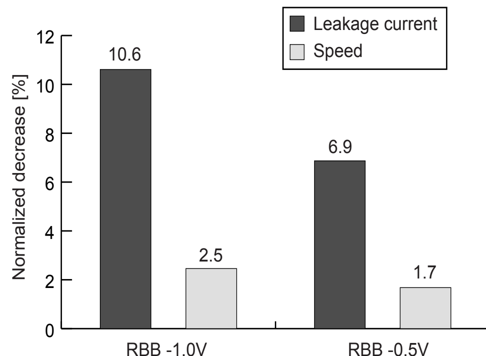


Fig. 7. Leakage and speed decreases by pMOS reverse body bias in CPU core.

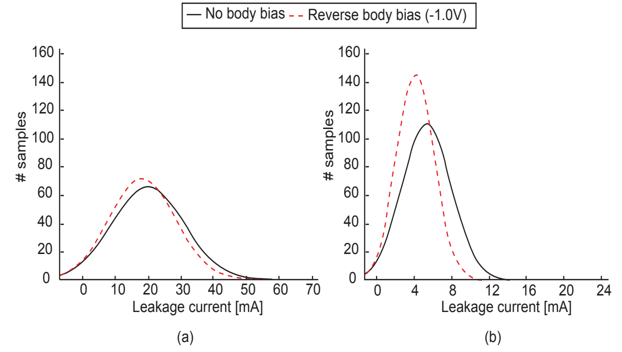


Fig. 8. Leakage current profiles in (a) CPU core and (b) top-level block.

CPU core shows less leakage reduction compared to top-level block because ABB is applied to only logic whereas it ABB is applied to both memory and logic in top-level block. As is clear in Fig. 8, RBB reduces the spread of the distribution. In CPU core, the standard deviation diminished from 10.7 to 9.9, and in top level, it is reduced from 3.2 to 2.5.

IV. Adaptive Voltage Scaling

Adaptive voltage scale (shortly AVS) has been used to manage leakage current [4, 13] because leakage current is a function of its supply voltage. Since supply of a circuit can be decided in silicon respect to leakage current requirement, AVS is an alternative to RBB thereby we compared AVS to RBB in terms of leakage current effect and design cost. To see the efficacy of AVS, we used 32-bit microprocessor as test vehicle in 45 nm low power CMOS technology. It is a RISC processor and handles instructions in five-stage pipeline. The micro-processor comprises of 700K cells and its foot print is 648 × 1021 μm^2. Fig. 9 shows silicon measure data of speed and leakage current.

When supply voltage is lowered down by 100 mV, leakage current decreases by 34.4% at the cost of speed

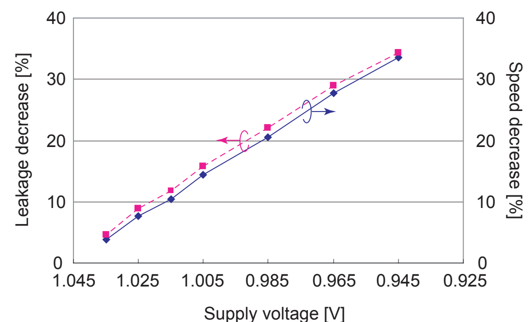


Fig. 9. Leakage and speed decreases with different supply voltages.

reduction of 33.6%. In RBB of 45nm node, body bias of -0.5 V reduces leakage current by 17.2% at the cost of speed reduction of 5.9%. AVS manages leakage current with voltage drop, which means that it relieves design overhead of a programmable voltage regulator. Since AVS is transparent in physical design, it is superior to RBB for area and engineering effort, but its speed drop is larger than RBB at the same leakage reduction.

V. HIGH-κ METAL GATE

Very thin equivalent gate oxide under 1 nm induces explosive increase of gate tunneling current and exacerbates process variation [14]. Hence, replacing SiO_2 with high-κ insulator is required to continue process scaling beyond 45 nm technology.

Fig. 10 shows gate tunneling current in three commercial CMOS technologies. Devices with gate oxide of SiO_2 shows fast rise of gate leakage current in scaling down. In 32 nm node, high-κ metal gate transistor, which uses high-κ insulator, is employed so as to manage gate tunneling current. Hence, gate tunneling current is cut off by 90% compared to conventional gate oxide in 32 nm node, and it is even less than 45 nm node by 33% whereas I_{ds} continues to increase. Due to the rise of I_{ds}, delay of logic cell has been shortened in scaling down. 2-input nand gate was selected to see delay comparisons between 45 nm and 32 nm nodes, and delay decreases by 26%.

Subthreshold leakage current increases by 31% in 32 nm node and it becomes more dominant leakage source. Hence, low power techniques to reduce subthreshold leakage are still useful and important. Also, due to the process variation, statistical design methodologies are adopted in leakage estimation [15] and timing analysis

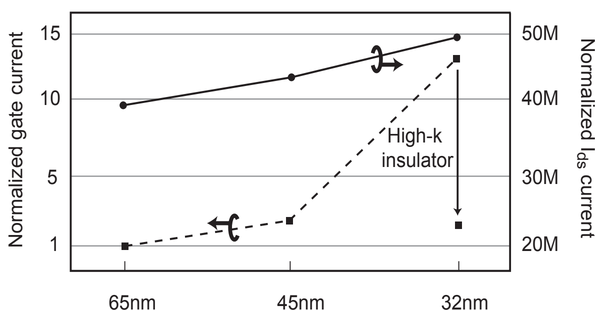


Fig. 10. Reduction of gate tunneling current using high-κ and metal gate.

[16]. Process-tolerant circuit techniques might be used [17, 18] to reduce functional failure.

VI. CASE STUDY: LEAKAGE REDUCTION IN 45 NM COMMERCIAL MOBILE SOC

In this section, we describe commercial mobile SoC for smartphone and its low power design methodologies. As many functions converged in a mobile device, mobile microprocessor requires high performance CPU core and digital/analog blocks for various functions. Especially, smartphone requires powerful multimedia processing, 3-D graphic support, and network packet processing for internet without compromising communication processing. Hence, we designed commercial mobile SoC comprising of 32-bit CPU core of 800 MHz, dedicated 3-D graphic processor, high-definition multimedia encoder/decoder, and various interfaces for input/output devices. This SoC is fabricated in 45 nm low power CMOS technology of triple well and eight metal layers for signal routing.

1. Design Overview

Fig. 11 shows floorplan of the mobile SoC. The mobile SoC contains seven sub-blocks and top-level logic cells, and it contains total 40M logic cells as placed in 7300 × 7300 μm^2 area. 32-bit CPU core contains 512KB L2 cache and it is connected to functional blocks via 32-bit-width bus of 200 MHz. MFC block supports decoding and encoding of high quality video up to 1080p definition in 30 frames per second. 3-D block processes 20M triangles per second while it can handle 2-D images.

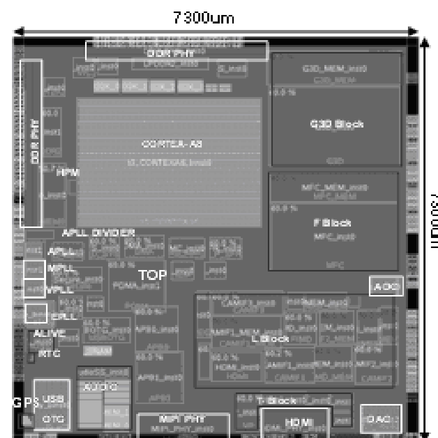


Fig. 11. Floorplan of 45nm low power mobile SoC.

Display, peripheral, and memory control blocks provide connectivity with various external screens, I/Os, memory devices respectively. Power gating and RBB were successfully used to manage leakage current. Seven sub-blocks adopt independent pMOS power gating proposed in Section II. All digital blocks are connected to body bias controller in Section III, and thus we can control V_t of each chip to sustain idle leakage current under 20-mW design goal.

2. Application and Verification of Low Power Design Methodologies

Power gating requires low power rule checking due to current switches and isolators. Isolators are required at the output of a power gated block to prevent short circuit current [8]. At the start and the end of physical design, we run rule check for the entire circuit. The rules are defined to detect missing isolators and invalid connection for current switches. Since we do not utilize retention flip-flops for seven sub-blocks, sub-block loses its state whenever going sleep mode. CPU core, 3-D, and display blocks contain large internal SRAM modules, and thus we adopt state-retention SRAM modules to reduce state restoration delay. We carefully decided sizes of current switches, and built virtual power networks to meet IR drop restriction. We checked post-layout speed in consideration of delay increase by the IR drop, and confirmed that static IR drop always meets the IR drop restriction in final design. Also, conventional verifications are performed for electrical rules, design rules, and more.

We control pMOS body to reduce leakage current by RBB. Body bias controller for pMOS in 45 nm technology has 381 × 225 μm^2 footprint. Body bias controller delivers bias via body bias network and regularly placed tap cells. We estimated total body leakage current across the entire chip, and analyzed IR drop with tap cells. Tap cell is used as uniform body bias source whose magnitude is calculated by dividing the estimated leakage with the number of tap cells.

VII. CONCLUSIONS

In this paper, we have introduced industrial applications of low power design methodologies in nano-meter scale technologies. To reduce design and area overhead of power gating, power network architecture and sleep signal network have been proposed. The proposed power gating saves leakage current up to 81% in 65 nm SoC. RBB reduces average and spread of leakage current in the entire chips. We have focused implementation scheme for low design and test engineering costs, and we have discussed control scheme of RBB in power gated circuits. In a 65 nm test vehicle, RBB shows average leakage reduction by 24.5% when applied to logic and memories. Since voltage scaling also reduces active leakage current, it has been compared to RBB, and silicon data shows that voltage scaling gives less leakage reduction at the smaller design cost. To manage gate leakage current, we have introduced industrial 32 nm high-κ metal gate device which replaces conventional device of SiO_2 gate dielectric. The use of multiple low power design and verification methodologies has been introduced in the case study of 45 nm commercial mobile SoC.

REFERENCES

[1] S. G. Narendra and A. Chandrakasan, *Leakage in nanometer CMOS technologies*, New York: Springer-Verlag, 2005.

[2] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicronmeter CMOS circuits," *IEEE*, Vol.92, No.2, pp.305–327, Feb., 2003.

[3] L. T. Clark, M. Morrow, and W. Brown, "Reverse-body bias and supply collapse for low effective standby power," *IEEE Trans. Very Large Scale Integr. (VLSI)*, Vol.12, No.9, pp.947–956, Sep., 2004.

[4] M. Nomura, Y. Ikenaga, K. Takeda, Y. Nakazawa, Y. Aimoto, Y. Hagihara, "Delay and power monitoring schemes for minimizing power consumption by means of supply and threshold voltage control in active and standby modes," *IEEE J. Solid-State Circuits*, Vol.41, No.4, pp.805–814, Apr., 2006.

[5] G. Gammie, A. Wang, M. Chau, S. Gururajarao, R. Pitts, F. Jumel *et al.*, "A 45nm 3.5G baseband-and-multimedia application processor using adaptive body-bias and ultra-low-power techniques," in Proc. *Int. Solid-State Circuits Conf.*, Feb., 2008, pp.258–259.

[6] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, “A 1-V power supply high-speed digital circuit technology with multiple threshold-voltage CMOS,” *IEEE J. Sold-State Circuits*, Vol.30, No.8, pp.847–854, Aug., 1995.

[7] S. V. Kosonocky, M. Immediato, P. Cottrell, and T. Hook, “Enhanced multi-threshold (MTCMOS) circuits using variable well bias,” in *Proc. Int’l Symposium on Low Power Electronics and Design*, Aug., 2001, pp.165–169.

[8] H.-O. Kim, Y. Shin, H. Kim, and I. Eo, “Physical design methodology of power gating circuits for standard-cell-based design,” in *Proc. Design Automat. Conf.*, July, 2006, pp.109–113.

[9] S. Borkar, T. Kamik, S. Narendra, J. Tscanz, A. Keshavarzi, and V. De, “Parameter variations and impact on circuits and microarchitecture,” in *Proc. Design Automat. Conf.*, June, 2003, pp.338–342.

[10] B. Choi and Y. Shin, “Lookup table-based adaptive body biasing of multiple macros,” in *Proc. Int’l Symposium on Quality Electronic Design*, March 2007, pp.533–538.

[11] J.Y. Choi, H.-S. Won, Y. Shin, J. Seomun, and B. Choi, “Lookup table based adaptive body biasing of multiple macros,” Korea patent 10-0817058-0000, Mar. 2008.

[12] L. L. C. Hsu, G. Frankowsky, and O. Wienfurtner, “Dynamic DRAM refresh rate adjustment based on cell leakage monitoring,” U.S. patent 6483764 B2, Nov., 2002.

[13] T. Chen and S. Naffziger, “Comparison of adaptive body bias (ABB) and adaptive supply voltage (ASV) for improving delay and leakage under the presence of process variation,” *IEEE Trans. Very Large Scale Integr. (VLSI)*, Vol.11, No.5, pp.888–899, Oct., 2003.

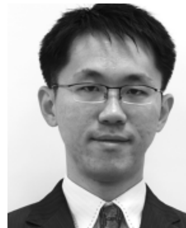
[14] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, “High-k/Metal-gate stack and its MOSFET characteristics,” *IEEE Electron Device Letters*, Vol.25, No.6, pp.408–410, June, 2004.

[15] R. Rao, A. Srivastava, D. Blaauw, and D. Sylbester, “Statistical analysis of subthreshold leakage current for VLSI circuits,” *IEEE Trans. Very Large Scale Integr. (VLSI)*, Vol.12, No.2, pp.131–139, Feb., 2004.

[16] H. F. Jyu, S. Malik, S. Devadas, and K. Keutzer, “Statistical timing analysis of combinational circuits,” *IEEE Trans. Very Large Scale Integr. (VLSI)*, Vol.1, No.2, pp.126–137, June, 1993.

[17] J. Jeong, S. Paik, and Y. Shin, “Statistical mixed V_t allocation of body-biased circuits for reduced leakage variation,” in *Proc. Asia South Pacific Design Automat. Conf.*, Jan., 2008, pp.629–634.

[18] L. Pileggi, H. Schmit, A. J. Strojwas, P. Gopalakrishnan, V. Kheterpal, A. Koorpaty, C. Patel, V. Rovner, and K. Y. Tong, “Exploring regular fabrics to optimize the performance cost trade-off,” in *Proc. Design Automat. Conf.*, June 2003, pp.782–787.



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