Mixed CT/DT Cascaded Sigma-Delta Modulator

Kye-Shin Lee

Abstract—**A mixed CT/DT 2-1 cascaded ΣΔM which includes a first stage CT ΣΔM and a second stage mismatch insensitive two-channel time-interleaved DT ΣΔM is proposed. With this approach, the advantages of both CT and DT ΣΔMs including high speed operation, inherent anti-aliasing filter, and good coefficient matching can be achieved. The two-channel time-interleaved ΣΔM used in the second stage alleviates the speed constraints of the DT ΣΔM, whereas enables better matching between the analog and digital filter coefficients compared to CT ΣΔMs.**

Index Terms—**Cascaded sigma-delta modulator, con tinuous-time, discrete- time, time-interleaved, high speed, matching**

I. INTRODUCTION

Nowadays, emerging telecom standards such as IEEE 802.11, WiMax, Zigbee, and 3G+ require wider signal bandwidth beyond the 10 MHz range for the Analog-to-Digital Converter (ADC) whereas maintaining 60 dB to 70 dB signal-to-noise ratio (SNR). So far, sigma-delta modulators (ΣΔMs) have been widely used for telecom applications owing to their power and area efficiency compared to other ADC architectures. However, it is difficult to achieve wider signal bandwidth with single-loop ΣΔMs even though high order or multi-bit techniques are used. Cascaded ΣΔMs can be a good solution for this problem, since higher order noise shaping is enabled by simply combing low order loop filters [1,2]. As a result, high SNR can be achieved with even low oversampling rate (OSR) with improved stability compared to single-loop high order ΣΔMs. For high speed applications, continuous-time (CT) ΣΔMs are preferred over discrete-time (DT) ΣΔMs due to good power efficiency. However, CT cascaded ΣΔMs suffer from mismatch between the analog and digital filter coefficients, since they rely on absolute value of the integrated *RC* components which can vary in the order of 20% due to process variations [2]. In order to overcome this problem, CT cascaded ΣΔMs usually require additional calibration or self tuning circuitry [3]. On the other hand, DT cascaded ΣΔMs using switched-capacitor (SC) circuits have better matching for the filter coefficients, since they are determined by capacitor ratios. Usually, the matching between capacitor ratios is in the order of 0.1% to 1%. However, DT ΣΔMs are not suitable for high sample rate operation due to high speed limitation of the sampling switches and op-amps. So, far several works using mixed CT/DT ΣΔM architecture have been proposed [4–6].

This paper presents a mixed CT/DT 2-1 cascaded ΣΔM. In this scheme, the sampling rate of the entire modulator can be determined by the first stage CT ΣΔM, since the internal circuitry of the second stage time-interleaved DT ΣΔM operates at half of the sampling rate, which enables high speed operation. In addition, matching between the analog loop filter and digital noise shaper coefficients can be improved with respect to all CT cascaded ΣΔMs. Furthermore, the power efficiency of the proposed architecture will still be preserved even though a DT ΣΔM is used in the second stage due to the relaxed speed constraints of the first order two-channel time-interleaved ΣΔM which can be implemented using only one op-amp and two quantizers.

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II. PROPOSED ARCHITECTURE

Fig. 1 shows the block diagram of the proposed mixed CT/DT 2-1 cascaded ΣΔM which includes the first stage CT ΣΔM, second stage two-channel time-interleaved DT ΣΔM, and the digital noise shaper. The equivalent *z*-domain expression of the first stage output y_1 is given by

$$Y_1(z) = z^{-2} \cdot X(z) + (1 - z^{-1})^2 \cdot \varepsilon_1(z) \tag{1}$$

where ε_1 is the quantization error of the first stage. The second stage takes $-\varepsilon_1$ as the input which is down sampled to u_2 and u_1, and further processed to generate the two time-interleaved outputs y_{22} and y_{21}. Furthermore, y_{22} and y_{21} are multiplexed to obtain the final second stage output y_2 which corresponds to

$$Y_2(z) = -z^{-2} \cdot \varepsilon_1(z) + (1 - z^{-1}) \cdot \varepsilon_2(z) \tag{2}$$

where ε_2 is the quantization error of the second stage. Overall, by combing the first stage output with the second stage output after passing through the digital noise shaper, and scaling by factor k ($k > 1$), the final output of the mixed CT/DT 2-1 cascaded ΣΔM becomes

$$Y_T(z) = z^{-4} \cdot X(z) + (1/k) \cdot (1 - z^{-1})^3 \cdot \varepsilon_2(z) \tag{3}$$

1. Two-Channel Time-Interleaved ΣΔM

The two-channel time-interleaved ΣΔM used in the second stage is obtained by transforming the conventional first order ΣΔM into its two-channel time-interleaved structure. Assuming the second stage is a conventional first order ΣΔM, the integrator output $p(n)$ with transfer function $H(z) = z^{-1}/(1 - z^{-1})$ is given by

$$p(n) = p(n-1) + u(n-1) - y_2(n-1) \tag{4}$$

where u is the input and y_2 is the output. Replacing the $p(n\text{-}1)$ term with $p(n\text{-}1) = p(n\text{-}2) + u(n\text{-}2) - y_2(n\text{-}2)$, Eq. (4) can be rewritten as

$$p(n) = p(n-2) + [u(n-1) + u(n-2) - y_2(n-1) - y_2(n-2)]. \tag{5}$$

Now, the two-channel time-interleaved form of $p(n)$ can be obtained by replacing n with $2n$. That is

$$p(2n) = p(2n-2) + [u(2n-1) + u(2n-2) - y_2(2n-1) - y_2(2n-2)] \tag{6}$$

where $u(2n\text{-}1)$ and $u(2n\text{-}2)$ are the down sampled version of the input $u(n)$, and $y_2(2n\text{-}1)$ and $y_2(2n\text{-}2)$ are the two time-interleaved outputs. Furthermore, the input-output relationship between the two-channel time-interleaved ΣΔM and the conventional ΣΔM are given as

$$u_2(n) = u(2n+1) \tag{7a}$$

$$u_1(n) = u(2n) \tag{7b}$$

$$y_{22}(n) = y_2(2n+1) \tag{7c}$$

$$y_{21}(n) = y_2(2n) \tag{7d}$$

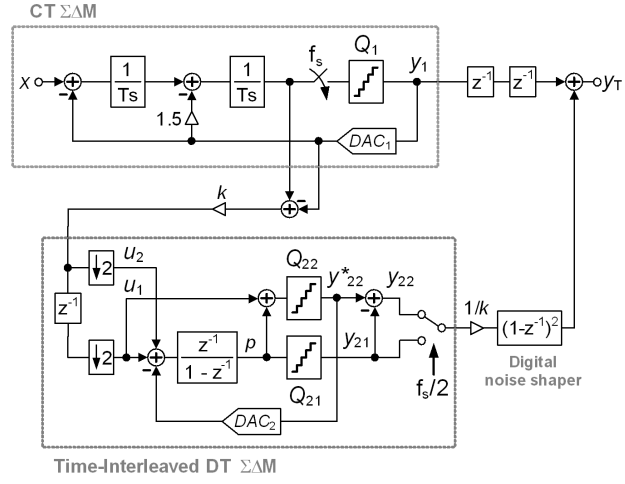

Fig. 1. Block diagram of the proposed mixed CT/DT 2-1 cascaded ΣΔMs.

The first time-interleaved output $y_{21}(n)$ can be obtained by directly quantizing Eq.(6), which is the first time-interleaved integrator output set. That is

$$y_{21}(n) = Q_{21}[\, p(2n)\,] \tag{8}$$

where Q_{21} represents the bottom quantizer of the second stage. However, quantizing the next time-interleaved integrator output set $p(2n+1) = p(2n) + u(2n) - y_2(2n)$, to generate output $y_{22}(n)$ is problematic. In this case, the actual SC implementation is not feasible, since the output of the bottom quantizer Q_{21} will be directly

connected to the input of the upper quantizer Q_{22}, where the two quantizer outputs $y_{22}(n)$ and $y_{21}(n)$ should be generated at the same time. Instead, an incomplete term $p^*(2n+1) = p(2n) + u(2n)$ which does not contain the output term $y_2(2n)$ is used as the input of Q_{22}. This term can be rewritten as

$$p^*(2n+1) = p(2n+1) + y_2(2n). \quad (9)$$

Noticing $y_{22}(n) = Q_{22}[\, p(2n+1)]$, and using Eq.(7d), the quantization of Eq.(9) leads to an incomplete output term $y^*_{22}(n)$ that can be rewritten as

$$y^*_{22}(n) = Q_{22}[\, p^*(2n+1)] = y_{22}(n) + y_{21}(n). \quad (10)$$

As a result, the complete output $y_{22}(n)$ can be obtained by subtracting $y_{21}(n)$ from output $y^*_{22}(n)$. Furthermore, since $y^*_{22}(n)$ is the sum of the two complete outputs, this can be directly used as the global feedback signal. Finally, using poly-phase decomposition [7], the second stage output can be written as

$$Y_2(z) = -z^{-2} + [\, z^{-1} \cdot \varepsilon_{12}(z^2) + \varepsilon_{11}(z^2)] + (1 - z^{-1}) \cdot [\, z^{-1} \cdot \varepsilon_{22}(z^2) + \varepsilon_{21}(z^2)] \quad (11)$$

where ε_{12} and ε_{11} are the down sampled version of ε_1, and ε_{22} and ε_{21} is the quantization error of Q_{22} and Q_{21}, respectively. The above Eq. (11) is equivalent to Eq. (2).

The two-channel time-interleaved structure of the first order ΣΔM can be obtained by combining Eq. (6), (8), and (10). In addition, as derived, the output of the second quantizer Q_{22} can be directly used as the global feedback signal. This single integrator single feedback architecture significantly reduces the mismatch involved with multi-path time-interleaved ΣΔMs whereas maintains the power efficiency, since the actual circuit can be implemented using only one op-amp and two quantizers.

2. Mismatch Analysis

The two-channel time-interleaved DT ΣΔM used in the second stage is robust to path mismatch due to its single feedback path and single integrator architecture, similar to the second order ΣΔM proposed in [8]. For the 2-1 cascaded ΣΔM, the following relationship should be satisfied to completely cancel out the first stage quantization error ε_1 at the final output y_T

$$z^{-2} \cdot NTF_1(z) = STF_2(z) \cdot (1 - z^{-1})^2 \quad (12)$$

where $NTF_1(z)$ and $STF_2(z)$ represents the first stage noise transfer function and the second stage signal transfer function, respectively. If CT ΣΔMs are used for the first and second stage, there will be mismatch between analog loop filter $NTF_1(z)$ and digital noise shaper $(1 - z^{-1})^2$, as well as between $STF_2(z)$ and $(1 - z^{-1})^2$ due to huge RC component variations. Both mismatches contribute to inter-stage quantization noise leakage which will degrade the performance of the cascaded ΣΔM [2]. However, for the proposed mixed CT/DT cascaded ΣΔM, by replacing the second stage with the mismatch insensitive time-interleaved DT ΣΔM, $STF_2(z)$ becomes nearly ideal, which reduces the mismatch between $STF_2(z)$ and $(1 - z^{-1})^2$.

Therefore, although the mismatch between the first stage analog loop filter $NTF_1(z)$ and the digital noise shaper $(1 - z^{-1})^2$ still exists, since a CT ΣΔM is used in the first stage, the overall leakage will be considerably reduced with respect to all CT cascaded ΣΔMs due to improved matching between $STF_2(z)$ and $(1 - z^{-1})^2$.

3. Effect of Clock Jitter and Excess Loop Delay

Clock jitter and excess loop delay are the two main non-idealities that critically degrade the performance of CT ΣΔMs, since in CT ΣΔMs, charge is transferred at a constant rate over a certain clock period. Therefore, the charge loss from the timing error can be a large portion of the total charge. Clock jitter is similar to adding a random phase modulation at the output bit stream of the modulator, which eventually increases the in-band noise floor by high frequency noise folding [9]. Fig. 2 shows the clock jitter modeling for CT ΣΔMs, where the jitter induced noise $E_j(z)$ is added to the DAC output, and $J(z)$ represents the timing error [10]. The jitter was assumed as white Guassian noise. For the proposed CT/DT cascaded ΣΔM, the second stage DT ΣΔM is not affected by the jitter, however this will not give much benefit, since the overall performance will be mainly determined by the CT first stage. In addition, since CT ΣΔMs with

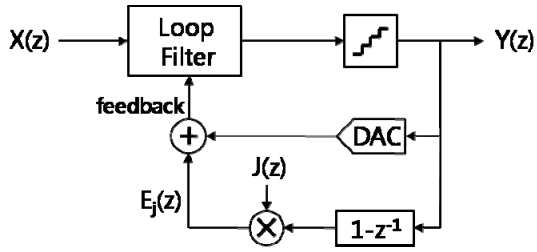

Fig. 2. Clock jitter modeling for CT ΣΔMs.

high sampling rate (> 100MHz) generally use internal PLLs instead of directly using external clocks, the clock jitter will be proportional to the PLL phase noise. Therefore, reducing the PLL phase noise which requires more power consumption can minimize the clock jitter. Moreover, clock jitter can be reduced by using multi-bit quantizers and NRZ DACs.

Excess loop delay is the delay between the quantizer clock and DAC output. Ideally, the DAC output responds immediately to the quantizer clock edge, however in reality, the transistors in the comparator latch and DAC cannot switch instantaneously [11]. Fig. 3 shows the concept of the excess loop delay. Similar to the clock jitter case, only the CT first stage of the proposed CT/DT cascaded ΣΔM will be affected by excess loop delay. However, the excess loop delay of the first stage CT ΣΔM will lead to inter-stage coefficient k mismatch for the cascaded ΣΔM. Moreover, when multi-bit quantizers are used, excess loop delay can increase due to the additional DEM circuitry added to the output of the feedback DAC. In addition, excess loop delay can cause instability to the loop filter, since it eventually reduces the feedback pulse. As a result, for the proposed CT/DT cascaded ΣΔM, loop delay compensation schemes such as [12, 13] can be included in the CT first stage, whereas the DT second stage does not require additional loop delay compensation.

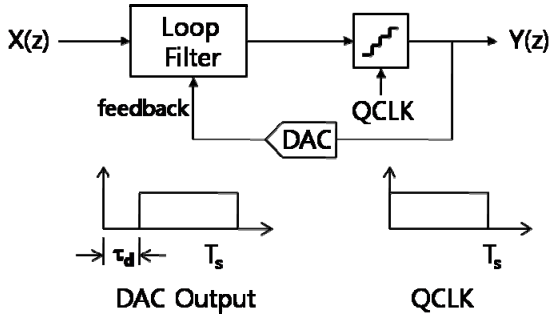

Fig. 3. Concept of excess loop delay in CT ΣΔMs.

III. SIMULATION RESULTS

The performance of the proposed mixed CT/DT 2-1 cascaded ΣΔM is verified through behavioral level simulations using *Simulink* [14]. Fig. 4 shows the ideal output spectrum with inter-stage coefficient k = 2. The sampling rate f_s was set to 400 MHz, where the internals blocks of the DT ΣΔM operates at 200 MHz. The high speed operation of the mixed CT/DT ΣΔM is enabled by the CT first stage and the time-interleaved DT second stage which operates at half of the sample rate $f_s/2$, whereas still maintaining the overall sample rate of the cascaded ΣΔM to f_s. As a result, SNDR of 83.7 dB can be achieved within signal bandwidth of 10 MHz using 5-level quantizers for Q_1, Q_{12}, and Q_{22}.

Fig. 5 shows the SNDR versus input amplitude, where (i) represents the ideal performance of the 2-1 cascaded ΣΔM without any mismatch. For both (ii) and (iii), ±20% and ±1% coefficient mismatch was added to the CT ΣΔM and DT ΣΔM, respectively. This mismatch value can be generally observed in nowadays deep sub-micron CMOS technologies. Results show the proposed mixed CT/DT 2-1 cascaded ΣΔM is less sensitive to coefficient mismatch than the all CT cascaded ΣΔM.

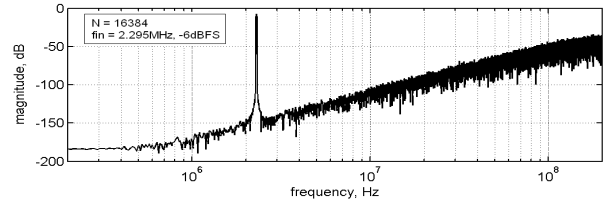

Fig. 4. Output spectrum of the proposed CT/DT cascaded ΣΔMs.

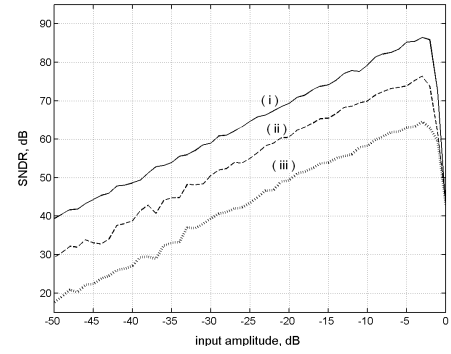

Fig. 5. SNDR versus input amplitude.
(i) 2-1 cascaded ΣΔM without mismatch
(ii) Mixed CT/DT 2-1 cascaded ΣΔM with mismatch
(iii) All CT 2-1 cascaded ΣΔM with mismatch

Fig. 6 shows the SNDR distribution with random coefficient mismatch for the proposed CT/DT cascaded ΣΔM and the all CT cascaded ΣΔM. In this case, coefficient mismatch of CT ΣΔM was varied up to ±20% assuming an *RC* component variation. For the DT ΣΔM, coefficient mismatch of ±1% was included for all cases. As shown from the result, SNDR degradation of the proposed CT/DT cascaded ΣΔM is less than all CT cascaded ΣΔM with coefficient mismatch. This can be explained by Eq. (12). The all CT cascaded ΣΔM will have mismatch between $NTF_1(z)$ and $(1 - z^{-1})^2$ as well as $STF_2(z)$ and $(1 - z^{-1})^2$, whereas the proposed CT/DT cascaded ΣΔM will have better matching between $STF_2(z)$ and $(1 - z^{-1})^2$. The reason for the all CT cascaded ΣΔM showing slightly higher SNDR than the proposed CT/DT cascaded ΣΔM around 0% coefficient mismatch is due to the ±1% mismatch that is already included in the second stage DT ΣΔM.

Fig. 7 is the SNDR degradation with clock jitter. SNDR degradation is the difference between the ideal SNDR and SNDR with jitter. The jitter amount was varied by changing the *rms* value of the random timing error $J(z)$, relative to the sampling period T_s (= $1/f_s$). It is shown that the SNDR degradation of the proposed CT/DT cascaded ΣΔM is slightly less than the all CT cascaded ΣΔM. This is because the DT second stage of the proposed ΣΔM is not affected by clock jitter, however the benefit is only around 1dB. Fig. 8 shows the SNDR degradation with excess loop delay τ_d. The abrupt SNDR degradation indicates the ΣΔM is under unstable condition where the output is oscillating. Results show the SNDR degradation of the proposed CT/DT cascaded ΣΔM is large with respect to the all CT cascaded ΣΔM with loop delay up to 35%. However, beyond 35%, SNDR degradation of the proposed ΣΔM is less than the all CT cascaded ΣΔM. This shows the stability of the proposed CT/DT cascaded ΣΔM is better than the all CT cascaded ΣΔM with excess loop delay.

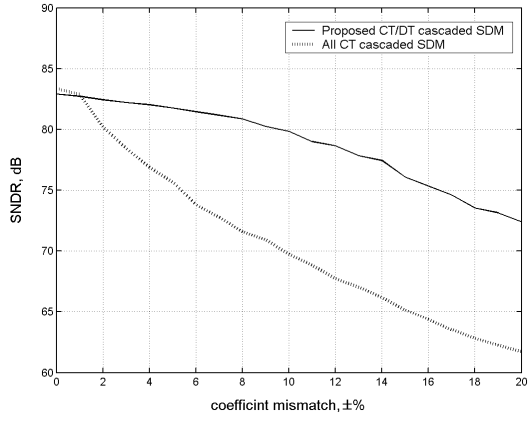

Fig. 6. SNDR versus random coefficient mismatch.

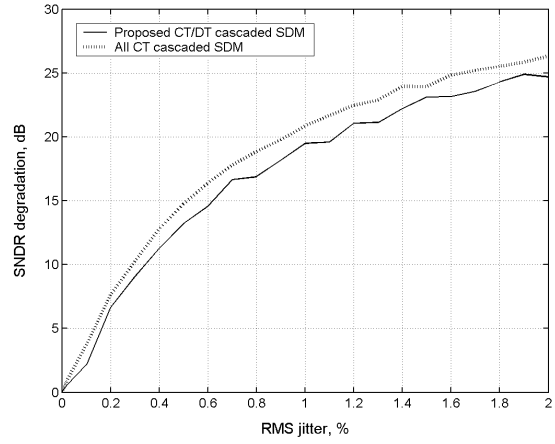

Fig. 7. SNDR degradation versus clock jitter.

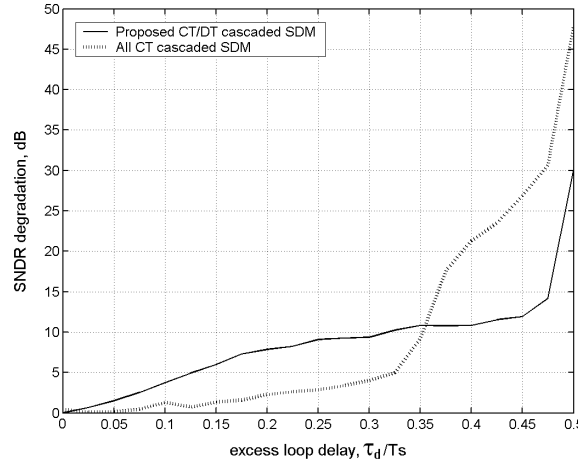

Fig. 8. SNDR degradation versus excess loop delay.

IV. CIRCUIT IMPLEMENTATION ISSUES

The proposed mixed CT/DT 2-1 cascaded ΣΔM includes the first stage CT ΣΔM, second stage two-channel time-interleaved DT ΣΔM, and digital noise shaper. The CT ΣΔM can be implemented using active-*RC* or G_m-*C* integrators [15, 16], whereas the DT ΣΔM can be realized with SC circuitry. Furthermore, in order to reduce the design complexity, one of the time-interleaved DT ΣΔM input sampler branch can be

removed. This does not degrade the performance of the time-interleaved ΣΔM as far as the OSR is larger than the number of channels [8]. Fig. 9 shows the concept of input sampler simplification where a gain of 2 is applied to the input, in order to compensate the loss of removing one branch.

Fig. 10 is an actual circuit implementation example of the proposed mixed CT/DT 2-1 cascaded ΣΔM with input sampler simplification. A single-ended schematic is shown for simplicity. The CT ΣΔM which operates at f_s is realized with two active-*RC* integrators, where the *RC* time constant sets the integrator coefficient. DAC_{11} and DAC_{12} are used to realize the first and second feedback around the 5-level quantizer Q_1. The two-channel time-interleaved DT ΣΔM is realized using one SC integrator, where clock-1 and clock-2 are the two phase non-overlapping clocks that operate at $f_s/2$. In addition, the first stage quantization error $-\varepsilon_1$ is applied to the integrator input and the summing circuit which generates the input signal of Q_{22}. The inter-stage gain k can be changed by adjusting the capacitor ratios. Furthermore, inverting and non-inverting switch configurations are combined to invert the sign of the quantization error ε_1 which is used at the input of the second stage SC integrator and the summing circuit. The remaining blocks including the delay, adder, MUX, and noise shaper which process the output of the quantizers can be implemented with digital standard cells.

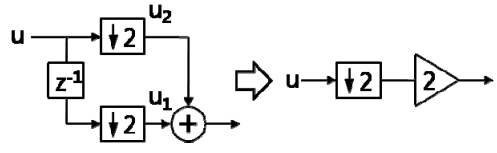

Fig. 9. Input sampler simplification for the second stage DT ΣΔM.

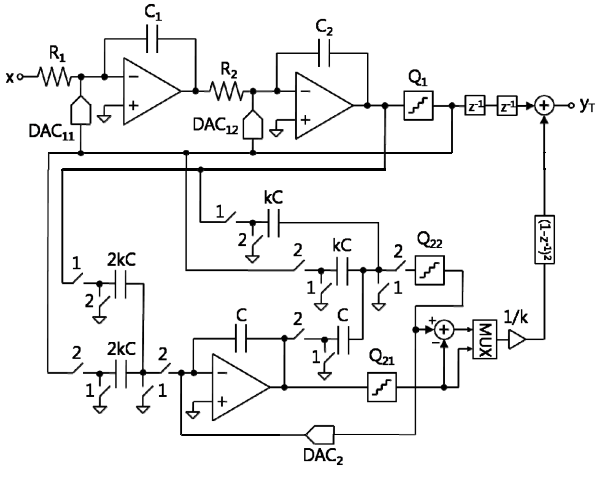

Fig. 10. Circuit implementation example.

V. CONCLUSIONS

A mixed CT/DT 2-1 cascaded ΣΔM is presented. This architecture is able to achieve high speed operation whereas matching between the analog and digital filter coefficient can be improved with respect to all CT cascaded ΣΔMs. Simulation results showed the proposed mixed CT/DT cascaded ΣΔM has less performance degradation with clock jitter than the all CT cascaded ΣΔM. However, with excess loop delay, the proposed architecture showed more performance degradation with respect to the all CT cascaded ΣΔM, yet the proposed ΣΔM showed better stability. Furthermore, the power efficiency of the proposed architecture will still be preserved even though a DT ΣΔM is used in the second stage, and the calibration or tuning scheme can be much more simplified, since it can be localized to the CT first stage. Overall, the proposed ΣΔM can be widely used as the ADC for emerging new telecom applications.

ACKNOWLEDGMENTS

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