Design of a Reliable Broadband I/O Employing T-coil

Seok Kim, Shinae Kim, Goeun Jung, Kee-Won Kwon, and Jung-Hoon Chun

Abstract—**Inductive peaking using T-coils has been widely used in broadband I/O interfaces. In this paper, we analyze technical effects and limitations of the T-coil, and discuss several methods that can overcome these restrictions and improve the practicality of the T-coil. In particular we also propose and verify a circuit topology which can further extend bandwidth beyond the limit that conventional T-coil can achieve, and transfer 20 Gb/s data without noticeable distortion.**

Index Terms—**Inductive peaking, T-coil, ESD, high-speed interface, reliability**

I. INTRODUCTION

Recently, the speed of chip-to-chip interface exceeds 5-10 Gb/s due to development of data links such as PCIe Gen2/3, XAUI and HyperTransport™, and memory links like GDDR5, XDR2, and DDR4. Subsequently, a signal bandwidth is severely affected by the I/O capacitance. To compensate the signal loss due to the I/O capacitance, high sensitivity receivers and/or equalizers need to be employed. To avoid this additional cost and power consumption, it is desirable to reduce the I/O capacitance. Among many components of the I/O capacitance, the capacitance associated with ESD protection devices has a considerable portion because it should provide reasonable ESD tolerance. The size of ESD protection devices need to be reduced without sacrificing ESD tolerance [1]. However, to meet the ESD requirements such as 2 KV HBM (Human Body Model) and 500 V CDM (Charged Device Model), it is not easy to reduce the capacitance of conventional ESD protection devices down to ~0.4 pF. In addition to ESD protection devices, the parasitic capacitance of metal lines, active devices, On-Die-Termination (ODT) etc. contributes to the total I/O capacitance; therefore, it is challenging to keep the I/O capacitance budget below 1 pF.

Since it is not easy to physically reduce the capacitance of devices and metal lines, there have been efforts to electrically hide them. For the broad band applications, several approaches have been proposed during the past few years. Kleveland et al. [2] demonstrated the distributed ESD protection system as shown in Fig. 1. The four segments of ESD protection devices and the CPW (coplanar waveguide) compose an artificial transmission line with the characteristic impedance the same as the source and RF input impedance; thereby avoiding the impedance discontinuity due to a large single capacitance of the conventional ESD protection device. The CPW should be designed to obtain the desired characteristic impedance:

$$Z_o = \sqrt{\frac{L_{CPW}}{C_{ESD} + C_{CPW}}} \tag{1}$$

Where L_{CPW} and C_{CPW} are the inductance and the capacitance of the CPW, respectively. The ESD protection structure in Fig. 1 is likely to have a non-uniform conduction issue; a large current is shunted by only the first few segments close to the I/O pad [1, 3]. Another drawback of this ESD protection scheme is its huge size because it needs the long CPWs between the segments to achieve a sufficient inductance. For example, the demonstrated structure in [2] is 0.35 mm ~ 1.4 mm long, and

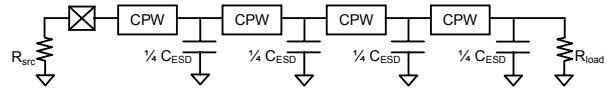

Fig. 1. Four-segment distributed ESD protection.

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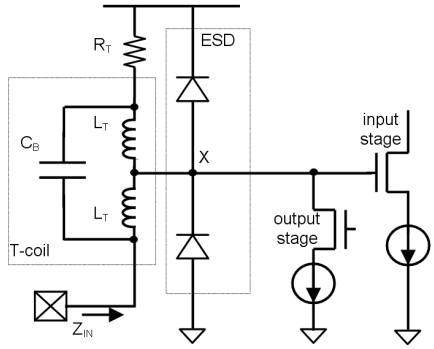


Fig. 2. T-coil network.

its application would be limited to the ICs with a few high-speed interfaces.

As an alternative solution, the T-coil depicted in Fig. 2 has been used in part of ESD protection structures [4, 5]. The T-coil network has the shunt-series inductive peaking structure which has been commonly used in microwave engineering [6]. Galal et al. [7] demonstrated that the T-coil network can provide a return loss of -20 dB at 10 GHz with negligible mid-band loss. However, the ESD test results show that HBM stress tolerance is only 800~1000 V although it has an ESD protection device as large as 1.2 pF.

In this paper, first, we discuss technical effects and limitations of the conventional T-coil structure, and suggest a proper optimization strategy to achieve better reliability and practicality. We also present several design solutions which can further extend bandwidth beyond the limit of the conventional T-coils.

II. ANALYSIS OF CONVENTIONAL T-COILS

Let's first look at the conventional T-coil illustrated in Fig. 2. With proper choice of L_T, C_B and the coupling coefficient (k) between two inductors with respect to R_T and the capacitance at the node X (C_X), Z_{IN} can be held as same as R_T over a wide frequency range.

Under the conditions given by (2)-(3), it can be proved that $Z_{IN} = R_T$ at all frequencies [5, 8].

$$C_B = \frac{C_X}{4}\left(\frac{1-k}{1+k}\right) \tag{2}$$

$$L_T = \frac{R_T{}^2 C_X}{2(1+k)} \tag{3}$$

Fig. 3 shows the simulated input return loss (S11) and signal transmission coefficient (S21) with and without T-coil. Here, C_X is 1 pF, and C_B, L_T are determined according to (2) and (3). Without the T-coil (no inductive peaking), S21 falls below -3 dB at 6.3 GHz. But 3-dB bandwidth extends to 8.7 GHz with the T-coil. Also S11 exceeds -10 dB around 2 GHz without inductive peaking but with T-coil it remains lower than -40 dB at frequencies over 10 GHz; showing perfect matching characteristics.

Fig. 4 shows the impacts of L_T, C_B variation on S11 and S21 at 10 GHz. Although both L_T and C_B are deviated from the values calculated from (2), (3) by 20%, S11 is still better than -10 dB. The variation of C_B does not affect S21 around 10 GHz. However, S21 is relatively sensitive to the variation of L_T. This observation suggests that the conventional T-coil design method with

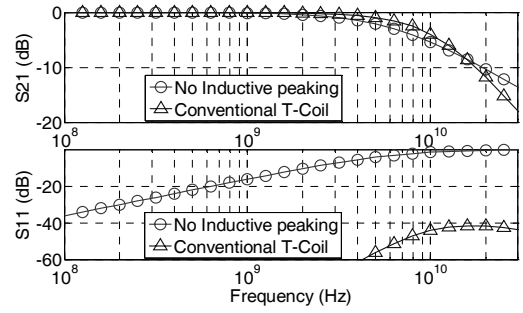


Fig. 3. S21 and S11 of I/O with the conventional T-coil.

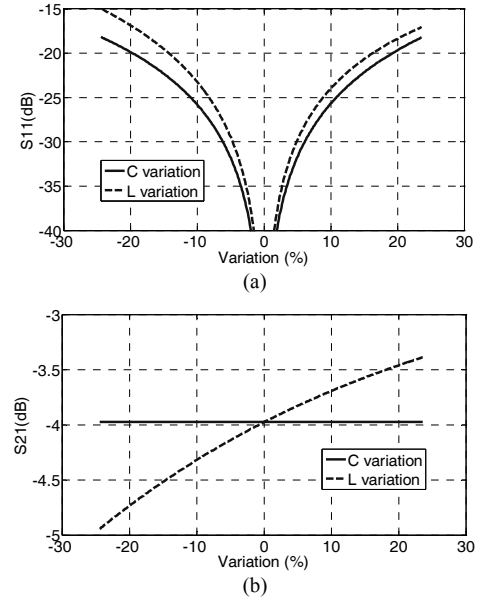


Fig. 4. The impacts of L_T, C_B variation on (a) S11 and (b) S21 at 10 GHz.

(2) and (3) are rather focused on the perfect matching in terms of S11. However, with varying L_T and C_B we can further improve the signal transmission characteristics while still keeping the very low return loss. These issues are explained in detail in Section 4.

Besides this optimization, several other issues should be addressed to adopt the T-coil in broadband applications. The on-chip inductors generally occupy large areas on the top metal layers that are supposed to be used for power delivery. For example, in [5] two cross coupled 1nH inductors have 85 μm×85 μm area. Large inductors may deteriorate not only area efficiency but also power integrity. Therefore, the T-coil cannot be used in applications with a number of high-speed I/O pins unless this large area problem is resolved. Another issue is the reliability problem of the T-coil itself. In the ESD protection scheme shown in Fig. 2, the on-chip inductors are involved in the ESD current path. The series resistance of the T-coils may cause low ESD immunity, and the abrupt turning at each corner of the T-coil layout could be vulnerable under ESD conditions [9]. Furthermore, in case I/O circuits dissipate large current during normal operation, T-coils can be damaged by electromigration as well. To prevent the EOS/ESD damage on the T-coil, wider metal layers should be used and it leads to even larger inductor size.

In the following section, we discuss how to improve the reliability of T-coils and reduce its area.

III. Realization of Reliable and Compact T-coils

Fig. 5 and Fig. 6 show design examples of reliable and compact T-coils. The structure in Fig. 5 is similar to a conventional planar transformer. In this structure, two thick metal lines (M8 and M9) are running in parallel, however, they are electrically shorted. Using two metal layers, the width of metal is reduced by half while keeping the same sheet resistance, and then the area can get smaller accordingly. The center tap and the bridges in the middle of the T-coil are formed with 3 metal layers to survive EOS/ESD stresses. Fig. 6 shows a stacked structure which has two inductors in different layers. One inductor is formed with M8 and the other one is with M9. The coupling coefficient, k between them can be tuned by shifting the center of one inductor with reference to that of the other. For the stacked T-coil, as changing the direction of rotation, we can obtain a negative sign of the coupling coefficient. With the negative k we can further extend bandwidth even though the inductor size is smaller than the conventional T-coil. A drawback of this design is that it can not meet the perfect matching condition. However, it is possible to maintain the return loss lower than -10 dB up to 10 GHz, adjusting L_T, C_B, and k.

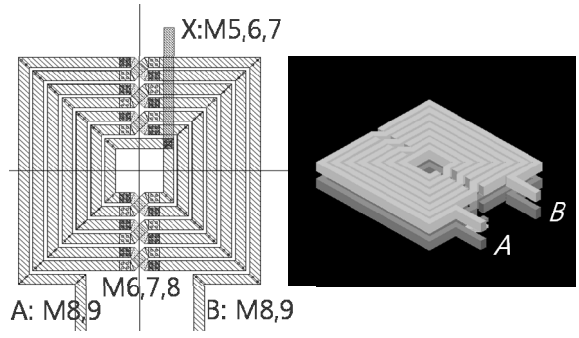


Fig. 5. A planar inductor with multiple layers.

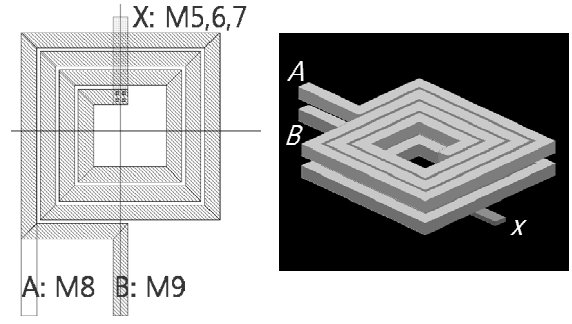


Fig. 6. A stacked inductor with negative coupling coefficient.

Fig. 7 explains another method that minimizes the size of T-coil and optimizes the circuit characteristic. The ESD protection circuit is divided into ESD1 which is directly attached to the I/O pad and ESD2 at the node X. It can reduce both C_X and L_T in (2) and (3), which means that the bandwidth close to that of the conventional T-coil can be realized with smaller inductance. Though the capacitance of ESD1 which cannot be canceled by T-coil might affect the matching characteristic, it is not supposed to be a major issue because the contribution of ESD1 (0.2 pF) to the total capacitance (~1.0 pF) is relatively small. When the capacitance of ESD1 is around 0.2 pF, it is easy to get S11 less than -10 dB at 10 GHz.

Fig. 8 illustrates S21 of topologies described from Fig. 5 to Fig. 7. To compare the area efficiency of the three

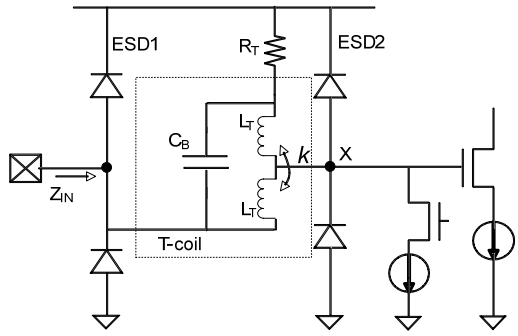


Fig. 7. T-coil with split HBM diodes (ESD1 and ESD2).

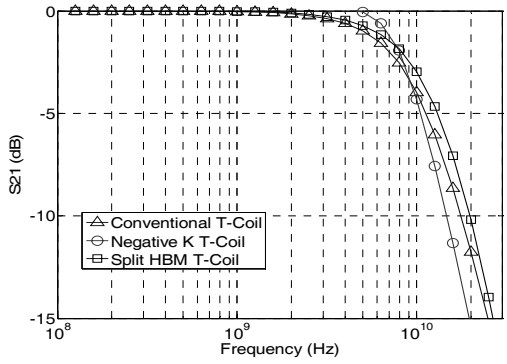


Fig. 8. S21 of -k, split ESD, conventional T-coil.

structures, the 3-dB bandwidth is set to 8.7 GHz in all cases, and the total I/O capacitance values are also identical. While S11 is not shown, it is kept below -10 dB up to 10 GHz. As summarized in Table 1, the stacked T-coil with negative *k* (Fig. 6) requires half the inductance than the conventional T-coil. The split ESD structure can also achieve the same bandwidth with 25% smaller inductance comparing to the conventional T-coil. Fig. 9 shows the layout of the test chip with I/O structures with two different T-coil implementations. Tcoil1 is the stacked inductor with negative k and Tcoil2 is the planar inductor. The test chip is built using a 9-Metal (2 thick metal) 90 nm CMOS process.

Table 1. Parameter values of three different T-coil structures in Figs. 5-7

	-k	split ESD	Conventional T-coil
k	-0.5	0.5	0.5
L_T	**0.4 nH**	**0.6 nH**	**0.8 nH**
C_{load}	1.0 pF	Total: 1.0 pF (ESD1:0.2 pF, C_X including ESD2:0.8 pF)	1.0 pF

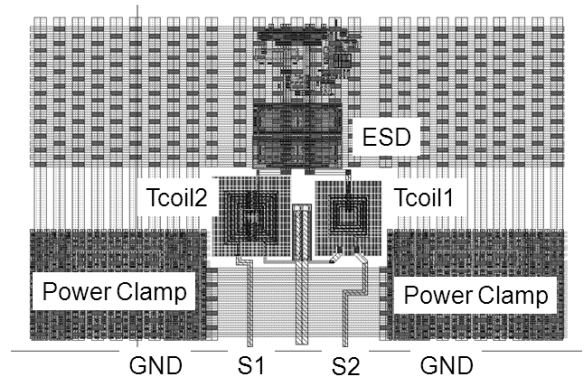


Fig. 9. Layout of the test circuit.

IV. IMPROVEMENT OF T-COIL TOPOLOGY

As stated above, the conventional T-coil is rather focused on suppressing the input reflection. In the I/O with the conventional T-coil (Fig. 2), low frequency signals can reach the node X without a loss, but extremely high frequency signals are directly transferred to R_T through C_B, and the signal strength at the node X is determined by L_T, k, and the capacitance at the node X. In other words, at very high frequencies the input reflection is still very low because Z_{IN} is always close to R_T. However, S21 which represents the signal transmission from the pad to the internal circuit can be degraded. This implies that the actual expansion of bandwidth may not be large enough in terms of the signal transmission, although the input impedance is perfectly matched to the characteristic impedance of the channel. Fig. 3 makes this point clear, showing that S21 decreases by more than 5 dB while the return loss is below -40 dB at 10 GHz.

To solve this signal degradation problem, the node Y in Fig. 10 is connected to the internal circuit which was attached to the node X in the conventional topology. A large capacitance of the ESD circuit is still at the node X, but now the node Y is associated with the capacitance of the internal circuits. Although this I/O structure cannot offer the perfect input matching because of capacitance at the node Y, the input reflection is considerably mitigated comparing to that without T-coil. That is, S11 can still be maintained below -10 dB up to 10 GHz. Because high frequency signals can reach the node Y, the reduction of S21 is noticeably slowed when frequency is over 10 GHz as shown in Fig. 11.

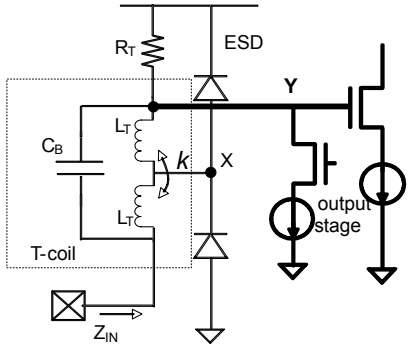


Fig. 10. Modified T-coil connection for better signal transmission.

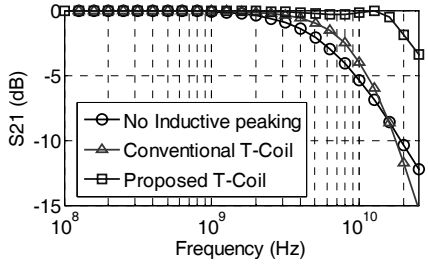


Fig. 11. S21 of the conventional and proposed T-coils.

Fig. 12 shows time delay (Td) variation as a function of frequency. The Td variation should be minimized for signals to be transferred without distortion. Below 20 GHz the Td variation of the proposed T-coil is similar to or less than the variation of the conventional T-coil. However it rapidly increases around 15 GHz. As summarized in Table 2, the degradation of S21 is less than 3 dB up to 35 GHz, but the actual bandwidth is limited to 10-15 GHz due to the variation of Td.

Eye diagrams of Fig. 13 clearly show the advantage of the improved T-coil connections. Fig. 13(a) is for the 20 Gb/s signal at the node X in Fig. 2, and Fig. 13(b) shows the signal at the node Y in Fig. 10. With the conventional T-coil, the voltage margin at the center is reduced

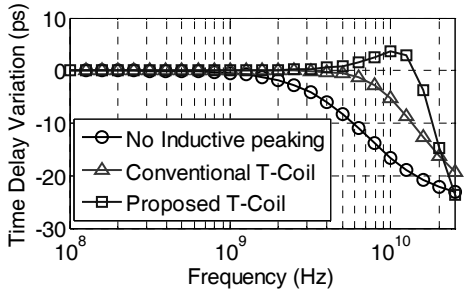
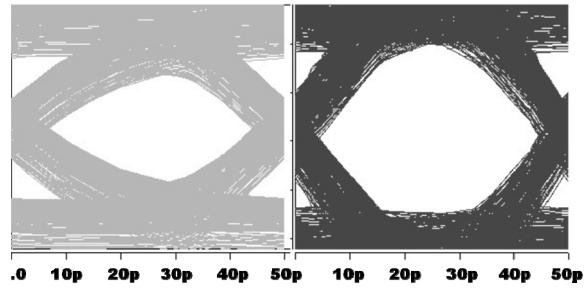


Fig. 12. Time delay (Td) variation vs. frequency.

Table 2. 3 dB Frequency and Td Variation @ 10 GHz

	3 dB Freq.	TD variation@10 G
No inductor	6.3 GHz	17 ps
Conventional T-coil	8.6 GHz	6 ps
Proposed T-coil	35 GHz	3 ps



(a) Conventional T-coil (b) Modified T-coil

Fig. 13. Eye diagrams at 20 Gb/s.

because of the signal degradation as mentioned earlier. However, with the connections in Fig. 10, the voltage margin is increased by nearly 45%.

V. CONCLUSIONS

This paper proposes methods of improving the practicality of the T-coil and further expanding the I/O bandwidth. The reliable T-coil structures were able to be embodied on a small area. Using multiple thick metal layers in a 90 nm CMOS process, the size of the T-coil can be cut down to 45x45 um^2, while providing >10 GHz I/O bandwidth and >2 KV HBM ESD tolerance. We have also proposed and verified the structure that can fix the signal degradation problem of the conventional T-coil. In the modified T-coil where the internal circuits are connected to the termination resistor, the effect of the capacitive loading at the I/O is effectively cancelled by the T-coil. The data transfer rate faster than 20 Gb/s is possible without considerable signal distortion.

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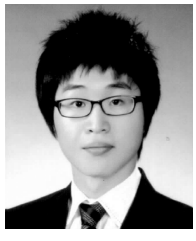

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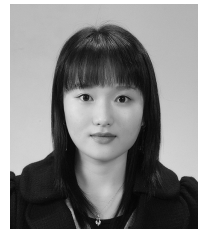

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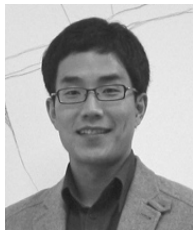

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