

# A 10-bit Current-steering DAC in 0.35- $\mu$ m CMOS Process

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A simulation study of a 10-bit two-stage DAC was done by using a conventional current switch cell. The DAC adopts the segmented architecture in order to reduce the circuit complexity and the die area. The 10-bit CMOS DAC was designed in 2 blocks, a unary cell matrix for 6 MSBs and a binary weighted array for 4 LSBs, for fabrication in a 0.35- $\mu$ m CMOS process. To cancel the accumulation of errors in each current cell, a symmetrical switching sequence is applied in the unary cell matrix for 6 MSBs. To ensure high-speed operation, a decoding circuit with one stage latch and a cascode current source were developed. Simulations show that the maximum power consumption of the 10-bit DAC is 74 mW with a sampling frequency of 100 MHz.

**Keywords:** DAC, Current-steering, Segmented architecture, CMOS symmetrical switching, High-speed

## 1. INTRODUCTION

The pressure to reduce cost in communication devices, such as cable modems and mobile cellular networks, has created a demand for embedded high-speed and high-resolution analog-digital and digital-analog converters. Recently published work on 8- to 14-bit converters[1-4] has focused on high-frequency application. Digital-analog converters (DACs) usually operate at speeds of several hundreds of MS/s at resolutions on the order of 10-14 bits. For such applications, a DAC must not only exhibit a good static linearity in terms of INL and DNL, but it should also maintain that linearity at high speeds in the Nyquist rate. DAC dynamic performance in terms of spurious free dynamic range (SFDR) is limited by the static linearity and is dependent on an architecture-dependent factor.

Current-steering DACs have been favored for high-speed and high-resolution applications because of their ability to drive a resistive load without the need for a buffer. This ability is based on an array of matched current sources which are unary decoded or binary weighted. Architectural variants are the two-stage[5], the interpolated[6], and the segmented architecture[2-4]. For signal processing applications, the segmented architecture is most often used to reduce decoding logic complexity and the overall layout area. It can also allow a reduction in the glitch energy and nonlinearity.

The design presented in this paper is a low-power, high-speed, 10-bit-accuracy, current-steering segmented architecture DAC implemented in a standard twin-well single-poly and four-metal layer in a 0.35- $\mu$ m CMOS process. Two sub-DACs are composed of a unary matrix type and a binary ladder type. The least significant bits (LSB's) steer a binary array, while the most significant bits (MSB's) are thermometer coded and steer a unary array. In section II, we introduce an overview of the DAC architecture. In section III, we present the current cell and switching scheme. And we present the layout and main results in sections IV and V.

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## 2. DAC ARCHITECTURE

To achieve good linearity and a low glitch energy, the number of bits implemented in the binary weighted part of the DAC must be small. In the N-bit binary array, only N current sources are available with variable sizes of bit current. This can lead to a large DNL error and an increased dynamic error in major code transition. For extra n bits in a unary array, however, an n-bit converter can generate  $2^n - 1$  different output codes, and the decoding logic complexity increases significantly. The digital input code is usually converted to a thermometer code that controls the switches. The major disadvantage of a thermometer-coded array is the area, complexity, and power consumption, since for each bit the array requires a current source, a switch, and a decoding circuit. However, there are several advantages for a thermometer-coded DAC versus a binary type. Among them is the fact that the glitch problem can be greatly reduced. The magnitude of a glitch is proportional to the number of switches that are actually switching. So for a small (large) number of signal steps, the glitch is small (large). To get the best architecture for DAC, most current steering DAC is implemented using a segmented architecture with a mixture of the previous binary array and thermometer coded unary array, which is usually divided into two sub-DACs.

Our DAC architecture is shown in Fig. 1. It is a segmented architecture so as to reduce the number of current cells and enhance the miniaturization of the chip area. The DAC is divided into two sub-DACs, which consist of the four least significant bits (LSBs) using binary array current cells and the six most significant bits (MSBs) with thermometer-coded unary array. The advantage of the binary array is the simplicity and small chip area, while a unary array has small dynamic switching errors and good linearity[4]. Each block in the matrix consists of a current cell, a latch, and a decoding circuit. In the first step of the decoding, digital inputs are decoded in the row and column decoder. The selection of the current cell corresponds to the input value of the column and row decoder. Each logic gate in the current cell identifies the matrix type by comparing one decoder signal with the one next to it. If both of the

signals are at a high level, then the current source is turned on.

In this segmented architecture, an optimization of the architecture between dynamic performance versus simplicity, area, and power consumption is applied in “6 M + 4 L” segmentation.

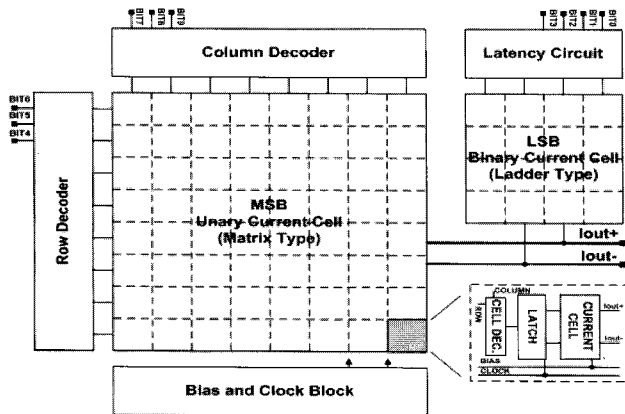


Fig. 1. Block diagram of 10-bit DAC: “6+4” segmentation.

### 3. CURRENT CELL AND SWITCHING SCHEME

The current cell is composed of a differential amplifier and a current source. When a MOS transistor is used as a switch in a conventional current cell[2,3], the controlling signal on the gate can couple through the gate-to-drain capacitance to the output. Since a full-swing wave is normally used as the controlling signal for the MOS switch, a significant amount of charges and large voltage spikes are injected onto the output at each edge of the controlling signal, which leads to excessive noise in the circuit, or the clock-feedthrough effect.

In this current cell, two cascoded transistors in current source are applied to increase the output impedance, and the input signals in transistors  $M_x$  and  $M_y$  are in an opposite logic. For a low-to-high logic transition of the input signal in transistor  $M_x$ , the transistor  $M_x$  forms a channel and then operates in the linear region. When the transistor  $M_x$  is on, the other transistor is off.

In the unary cell matrix for 6 MSBs, the outputs of the current cells are nonuniform because of the error distribution of the current cells along a column or row in the matrix. Large linearity errors in a sequential switching are caused by the accumulation of errors in each current cell. To cancel multiple types of errors, such as a graded error and a symmetrical error, one can apply hierarchical symmetrical switching[7]. With an increase in the digital input, the symmetrical error caused by a current cell is canceled by the current cell selected successively, while the graded error caused by a pair of current cells is canceled by the pair cell selected successively. In the symmetrical switching sequence[8], current cells located symmetrically about the center are turned on. Then a graded error caused by a voltage drop of a certain current cell is canceled by the symmetric current cell. In a conventional symmetrical switching, graded errors are usually canceled at every two increments of digital input. As shown in Fig. 3, our work

uses symmetrical switching because of the relatively small number of bits needed to apply the hierarchical symmetrical switching.

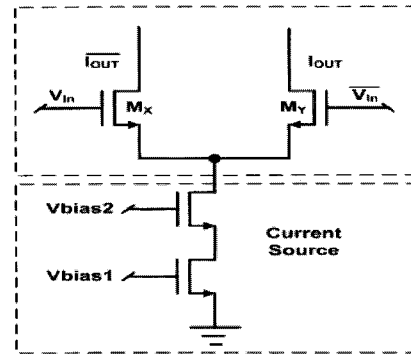


Fig. 2. Current cell with current source and switching transistors.

When the digital input 4 is used in the row or column sequence, graded errors due to current cell 1 and 3 are canceled by those due to current cell 2 and 4. Although hierarchical symmetrical or 2-D centroid switching can be a more effective way to suppress linearity errors, a pre-study of INL by the switching sequence in Fig. 3 indicates the errors to be within 0.5 LSB.

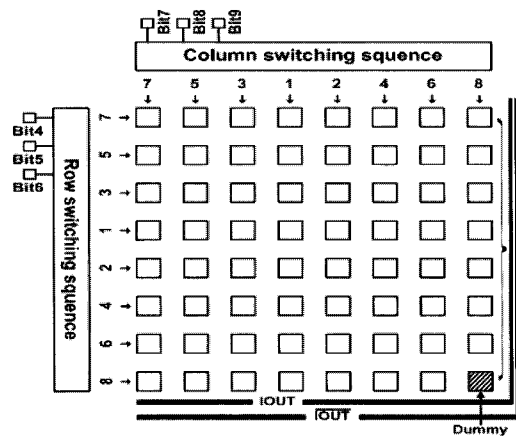


Fig. 3. Switching sequence of the symmetrical switching scheme.

### 4. SIMULATION LAYOUT

In this D/A converter, the power supply for the analog circuits is separated from the block of the digital circuit in order to avoid coupling between the analog output signal and the digital signal. A current cell and its decoder are connected to a latch for suppression of signal skew. N-well of the current cells is separated from the digital circuit to avoid noise. Aluminum interconnection is relatively wide in order to suppress a voltage fluctuation caused by the charge and discharge current from the on-off switching. The interconnection line is also compactly laid out with a symmetric structure.

As the digital code changes from minimum code to maximum code, the corresponding current cell is sequentially steered to output. The common-centroid scheme is used to obtain the switching and to cancel out the graded error. The design of the circuit in Fig. 1 is simulated in a 0.35- $\mu\text{m}$  CMOS technology. The circuit has an area of 1.3  $\text{mm}^2$ .

## 5. RESULTS

### 5.1 Glitch energy

The glitch energy is defined as the energy difference between an ideal and a real transition. During switching, the transient effect of the unary array converter can increase the dynamic nonlinearities. To minimize cell fluctuation, the two switching transistors in the current cell should not be switched off at the same time. Any asymmetry in the output lines of a cell can give rise to a glitch at the DAC output during code transition. High glitch energy usually comes from a major code transition. The code change is the derivative of the signal with respect to time. The derivative of each signal is a sine wave with the same frequency. If all transitions are equal and proportional to the code change, the code transition generates the same amount of glitch energies, and the distortion due to glitches is reduced to zero. If the glitch energy is strictly proportional to the code change, it will not cause any nonlinearity in the output signal. However, not all transitions are equal, and the glitch energy can show a big difference in a major code transition.

Figure 4 shows the glitch energy as the output voltage varies. The maximum glitch energy was found to be approximately 2.2 pV-s by applying this switching sequence, which is almost same result as has been reported in other work[2].

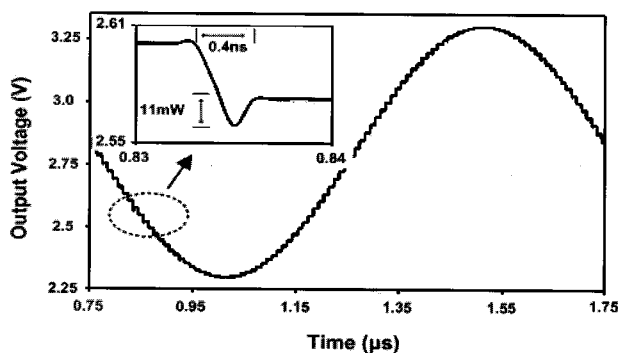


Fig. 4. The analog output and glitch energy with code transition.

### 5.2 DC characteristics and output switching signals

Figure 5 shows the transfer characteristics of the current cell. By lowering the cross-point of the switching signal, the circuit of the current cell makes one switching transistor to be in the conducting state, so that as soon as one of the switching transistors begins to switch on, the complementary transistor begins to switch off. The output current at the crossover point is almost half the current flowing through

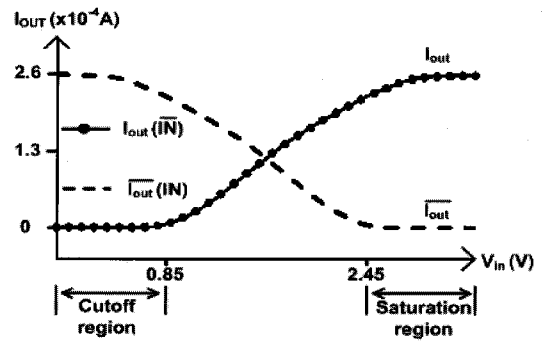


Fig. 5. DC transfer curve of the proposed current cell.

the common source. The transconductance of the current cell, which is the slope of the graph, is supposed to decrease with a higher overdrive voltage in the MOS transistor in the current cell. Both nMOS transistors in the current cell operate mostly in linear region for the range  $V_1 (0.85 \text{ V}) \leq V_{in} \leq V_2 (2.45 \text{ V})$ . Since the cell is symmetric, the rise and fall of the output waveform should be equal. In the other range, one operates in a triode saturation, and the other operates in a cutoff region. The linear range of operation can be extended by operating the transistor in the current cell at a higher overdrive voltage at the expense of reducing transconductance.

The bias current can be increased in order to obtain a higher transconductance. There is a trade-off between the transconductance and the linearity, assuming that the bias current in current source is kept constant. A smaller output current and transconductance can be obtained by decreasing the bias current, while the on-voltage is almost same. The transconductance is approximately 1.1 mA/V.

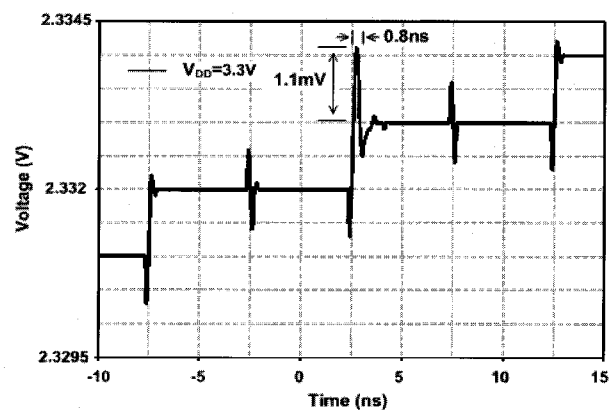


Fig. 6. Code transitions for consecutive code transition.

Figure 6 shows a simulated output signal of code transitions with 10 bits with cell supplies of  $V_{DD} = 3.3 \text{ V}$ . The glitch is known to come from the clock coupling, the digital switching, and the code transition. The glitch related to the clock coupling occurs between two transitions, while the glitch due to the digital switching occurs before each transition. The glitch at the ramp-up step in this figure is associated with the code transition. The maximum glitch energy is found to be 2.2 pV-s. Among the 3 types of glitch,

the glitch due to the code transition is found to be relatively large compared to the other two effects. The asymmetric operation of the current cell can give rise to a glitch during a code transition. The correct switch timing is important because it reduces the voltage variation and the glitch amplitude. The current cell has to be designed to minimize the voltage fluctuations at the drain of the current cell and limit the swing of the switching control.

### 5.3 Linearity and SFDR

The simulation shows DNL and INL in Fig. 7 to be within 0.4 LSB at a sampling speed of 100 MS/s and the maximum power consumption to be 74 mW. Figure 8 shows the corresponding fast Fourier transform (FFT), which was obtained at a 10-MHz sinusoidal input when the DAC was sampled at 100 MS/s. At the same sampling speed with a 100-MHz semi-log scale, the spurious-free dynamic range (SFDR) in Fig. 9 was found to be 57 dB and shown to decrease with increasing frequency. With an increase in the sinusoidal input up to 10 MHz, the simulated SFDR drops to 46 dB. SFDR can depend on the bias current in the current source because it can change the effective threshold voltage in the MOS.

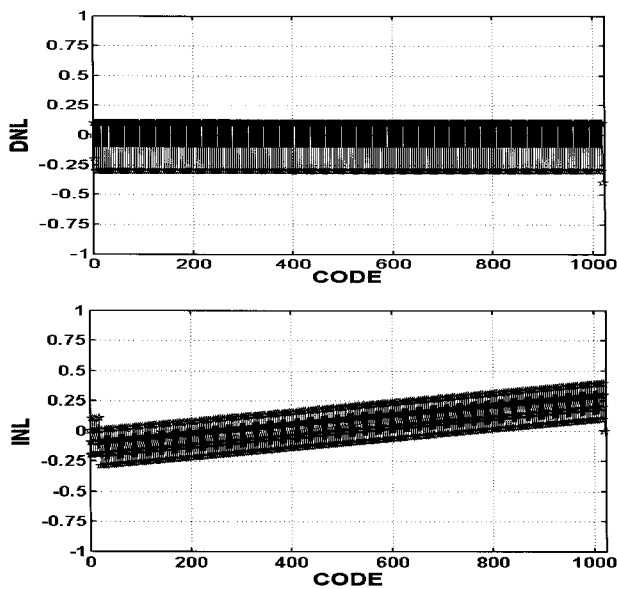


Fig. 7. DNL and INL characteristics.

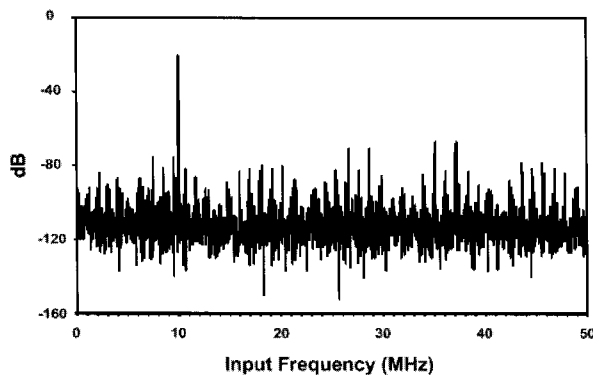


Fig. 8. FFT with variation of input frequency at 100 MS/s.

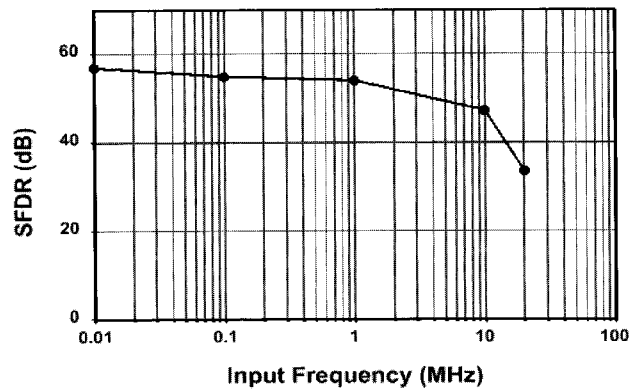


Fig. 9. SFDR as a function of the input frequency at 100 MS/s.

Table 1 compares the characteristics of the simulated results with the characteristics of previously reported high-speed ADCs[2-4]. The table demonstrates that this design achieves low power dissipation and INL with a high resolution and sampling rate.

Table 1. Performance comparison.

	[2]	[3]	[4]	This Design
Year	2001	2007	2006	2009
Technology	0.35 $\mu\text{m}$ CMOS	90 nm CMOS	0.18 $\mu\text{m}$ CMOS	0.35 $\mu\text{m}$ CMOS
Resolution	10 bit	12 bit	10 bit	10 bit
INL/DNL (LSB)	$\pm 0.2/\pm 0.15$	$\pm 0.6/\pm 0.6$	$\pm 0.1/\pm 0.1$	$\pm 0.5/\pm 0.3$
Sampling rate	200 MHz	160 MHz	250 MHz	100 MHz
SFDR/ Input freq.	61.2 dB/ 490 MHz	74 dB/ 975 KHz	60 dB/ 122.5 MHz	68 dB/ 1 MHz
Glitch energy	—	1.9 pV-s	2.64 pV-s	2.2 pV-s
Supply voltage	3.0 V	1.3/2.6 V	1.8 V	3.3 V
Power consumption	110 W	106 mW	22 mW	68 mW
Area	0.35 mm <sup>2</sup>	0.13 mm <sup>2</sup>	0.35 mm <sup>2</sup>	1.3 mm <sup>2</sup>

## 6. CONCLUSION

We designed a 10-b segmented DAC architecture in a 0.35- $\mu\text{m}$  layer CMOS process with single-poly and four-metal. The current-steering CMOS DAC is composed of 2 blocks, which are a unary cell matrix for 6 MSBs and a binary weighted array for 4 LSBs. A conventional current cell and the symmetrical switching sequence are applied in the DAC. Simulations showed that the DNL is controlled to within 0.4LSB at 100 MS/s, and SFDR was shown to be 47 dB at a 10-MHz input frequency. The result indicates that the DAC's performance equals that of other published work [2-4] in terms of linearity, speed, and power consumption.

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