

# Dynamic Characteristics of DC-DC Converters Using Digital Filters

Fujio Kurokawa<sup>†</sup>, Masashi Okamatsu<sup>\*\*</sup>, Taku Ishibashi<sup>\*</sup>, and Yasuyuki Nishida<sup>\*\*\*</sup>

<sup>†\*</sup>Department of Electrical and Electronic Engineering, Nagasaki University, Japan

<sup>\*\*</sup>Graduate School of Science and Technology, Nagasaki University, Japan

<sup>\*\*\*</sup>Department of Electrical, Electronics and Computer Engineering, Chiba Institute of Technology, Japan

## ABSTRACT

This paper presents the dynamic characteristics of buck and buck-boost dc-dc converters with digital filters. At first, the PID, the minimum phase FIR filter and the IIR filter controls are discussed in the buck dc-dc converter. Comparisons of the dynamic characteristics between the buck and buck-boost converters are then discussed. As a result, it is clarified that the superior dynamic characteristics are realized in the IIR filter method. In the buck converter, the undershoot is less than 2% and the transient time is less than 0.4ms. On the other hand, in the buck-boost converter, the undershoot is about 3%. However, the transient time is approximately over 4ms because the output capacitance is too large to suppress the output voltage ripple in this type of converter.

**Keywords:** Buck converter, Buck-boost converter, Digital control, FIR filter, IIR filter, Dynamic characteristics

## 1. Introduction

Switching power supplies has been receiving increasing attention in an effort to save energy and  $C_{O2}$ . Furthermore, in telecommunications systems, data communications systems and so forth, high controllability and monitoring function are required to improve reliability. In this case, digital control is useful because it has the advantage of realizing both control and monitoring tasks.

The digital control circuit is composed of an A-D

converter and a control part which is usually constructed by a ASIC or DSP<sup>[1]-[4]</sup>. In this control circuit, the digital P-I-D control or the digital low-pass filter control algorithm has been programmed. So, these control methods have been reported<sup>[1],[5]-[8]</sup>. However, the output characteristics of these dc-dc converters have never been discussed in detail.

Especially, the relationship between the output characteristics of the digital filter method and the control parameters is unknown.

This paper presents the dynamic characteristics of the basic buck and buck-boost converters with digital filters. After reviewing the fundamental configuration of a digitally controlled dc-dc converter and its operation principle, we analyzed the dynamic characteristics of three types of digital control methods. The comparison of dynamic characteristics of the P-I-D control method, FIR (Finite Impulse Response) filter method and IIR

---

Manuscript received Jan. 31, 2009; revised 20 March 2009

<sup>†</sup>Corresponding Author: fkurokaw@nagaaski-u.ac.jp

Tel:+81-95-819-2553, Fax:+81-95-819-2558, Nagasaki Univ.

<sup>\*</sup>Dept. of Electrical and Electronics Eng., Nagasaki Univ.

<sup>\*\*</sup>Graduate School of Science and Technology, Nagasaki Univ., Japan

<sup>\*\*\*</sup>Dept. of Electrical, Electronics and Computer Engineering, Chiba Institute of Technology, Japan

(Infinite Impulse Response) filter method is examined. Lastly, the dynamic characteristics of the basic buck and buck-boost converters with the most suitable digital filter are considered. The key point of this paper is to describe the possibility of realizing a digitally controlled switching power converter using a DSP.

## 2. Circuit configuration and operation

Fig. 1 shows the block diagram of the proposed digitally controlled dc-dc converter using a DSP. In Fig. 2 they are examined.  $E_i$  is the input voltage,  $e_o$  is the output voltage and  $i_o$  is the output current in these figures.

$T_r$  is the main switch, D is the fly wheel diode, L is the energy storage reactor, C is the output smoothing capacitor and R is the load. The output voltage  $e_o$  is sent to the A-D converter through the anti-aliasing filter and is converted into digital amount  $N_n$ . The relation between the input and output values of the A-D converter is given by equation (1) when it approximately shows the linear expression by considering the width of the quantization to be small.

$$N_n = G_{AD}e_o \quad (1)$$

where n denotes an n-th switching cycle, and the digital amount  $N_n$  is a positive integer number.  $G_{AD}$  is a gain of the A-D converter.

The digital amount  $N_n$  is sent to the DSP. In the DSP, the numerical value  $N_{Ton}$  that corresponds to the on-time interval  $T_{on}$  is calculated.

The relation between the on-time interval  $T_{on}$  and the numerical value  $N_{Ton}$  is shown as follows;

$$\frac{T_{on,n+1}}{T_s} = \frac{N_{Ton,n+1}}{N_{Ts}} \quad (2)$$

where  $N_{Ts}$  is a numerical value corresponding to the switching period  $T_s$  ( $=1/f_s$ ).  $N_{Ts}$  is calculated in the PWM signal generation circuit which is composed of a digital comparator or a counter. According to the relation between the on-time interval  $T_{on}$  and the numerical value  $N_{Ton}$ ,  $T_{on}$  is generated. This  $T_{on}$  regulates the output voltage  $e_o$ .

The numerical value  $N_{Ton}$  of each control method is represented as follows.

### 2.1 P-I-D Control Method

The on-time interval  $N_{Ton}$  of the P-I-D control circuit is represented as follows [9];

$$N_{Ton,n+1} = N_B - K_P(N_n - N_R) - K_D(N_n - N_{n-1}) - K_I \sum(N_n - N_{INT}) \quad (3)$$

where  $K_P$ ,  $K_D$  and  $K_I$  are the proportional, differential and integral coefficients.  $N_B$  is the numerical bias value.  $N_R$  and  $N_{INT}$  are the numerical proportional and integral desired values, these values are shown as follows;

$$N_B = N_{Ts} \left( I + r/R \right) \frac{e_o^*}{E_i} \quad (4)$$

$$N_R = N_{INT} = G_{AD}e_o^* \quad (5)$$

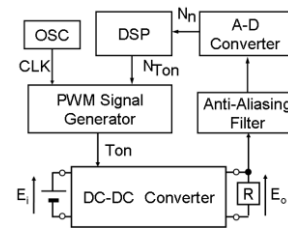
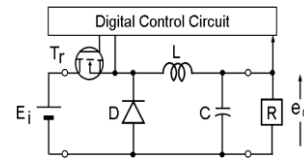
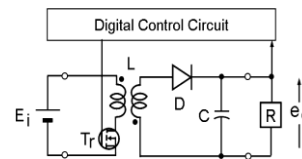


Fig. 1. Block diagram of digitally controlled dc-dc converter using DSP.



(a) Buck dc-dc converter



(b) Buck-boost converter

Fig. 2. Basic dc-dc converters.

## 2.2 FIR Filter Control Method

The on-time interval  $N_{Ton}$  of the minimum phase FIR filter control circuit is represented as follows <sup>[10]</sup>;

$$N_{Ton,n+1} = N_B - \sum_{i=0}^q h_i (N_{n-i} - N_R) \quad (6)$$

where  $h_i$  denotes the digital filter coefficients and  $q$  is the amount of the sampling points.

## 2.3 IIR Filter Control Method

The IIR filter is designed from an analog filter using the double primary conversion. The converted digital filter becomes the second-order IIR filters as shown in the next equation <sup>[11]</sup>.

$$y_n = a_0 x_n + a_1 x_{n-1} + a_2 x_{n-2} - b_1 y_{n-1} - b_2 y_{n-2} \quad (7)$$

where  $a_0, a_1, a_2, b_1$  and  $b_2$  are coefficients of the IIR filter,  $x_n$  is a difference between the digital value  $N_n$  and the desired value  $N_R$ .  $x_n$  is shown in the following equation.

$$x_n = N_n - N_R \quad (8)$$

Then, the on-time interval  $N_{Ton}$  of the IIR filter control circuit is represented by the following equation.

$$N_{Ton,n+1} = N_B - y_n \quad (9)$$

In a usual low-pass filter, a phase delay exists in the high frequency <sup>[10]</sup>. The phase delay sometimes causes unstable phenomena. So, to improve the delay of the phase, the differential element is added in this IIR filter. The stabilization of the dc-dc converter is attempted by this way.

## 3. Dynamic characteristics

### 3.1 P-I-D Control Method

Fig. 3 shows the experimental dynamic characteristics of the buck dc-dc converter with P-I-D control in step change of the load  $R$  from  $50\Omega$  to  $10\Omega$ . The input voltage  $E_i$  is 20V, the desired voltage  $E_o^*$  is 10V, the inductance  $L$  is  $247\mu\text{H}$ , the output capacitance  $C$  is  $940\mu\text{F}$ , and the number  $Q$  of bit of the A-D converter is 8bits, the dynamic range is from 0 to 20V corresponding

to the output voltage of the buck type dc-dc converter, respectively.

The sampling frequency  $f_{\text{smp}}$  in this case is 100kHz corresponding to the switching frequency  $f_s$  of the DC-DC converter. Furthermore, the other circuit parameters are  $f_s=100\text{kHz}$ ,  $N_{TS}=250$ ,  $N_{RP}=N_{RINT}=127$  and  $N_B=124$ . DSP is TMS320VC33. The calculation time of DSP is less than  $4.1\mu\text{s}$ .

The proportional coefficient  $K_P$ , the differential coefficient  $K_D$  and the integral coefficient  $K_I$  are 1.0, 1.0 and 0.01, respectively. The undershoot is over 200mV and the transient time  $T_{st}$  is 4.9ms. In this method, even if  $K_I$  is small and  $K_D$  is large, approximately 160mV is a minimum value <sup>[10]</sup> in the width of the vibration of the output voltage deriving from the limit cycle <sup>[11]</sup>. Therefore, this method is not suitable for the digitally controlled power dc-dc converter.

### 3.2 FIR Filter Control Method

Figure 4 shows the experimental dynamic characteristics in the minimum phase FIR filter control. The circuit parameters are the same as in Fig. 3 except for the data in Table 1.

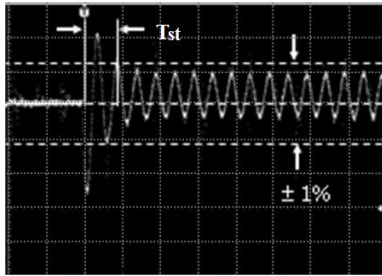
Figure 5 shows the frequency characteristics of the FIR filter corresponding to Fig.4. In this method, the undershoot is over 200mV and transient time  $T_{st}$  is 2.7ms. Although the oscillation deriving from the limit cycle is suppressed, the transient response is not enough.

Table 1 Measured conditions corresponding to Fig. 4

|                              |     |
|------------------------------|-----|
| Passage Area Frequency (kHz) | 5   |
| Transition Area (kHz)        | 15  |
| Passage Area Ripple (dB)     | 0.0 |
| Quantity of Decrement (dB)   | 13  |

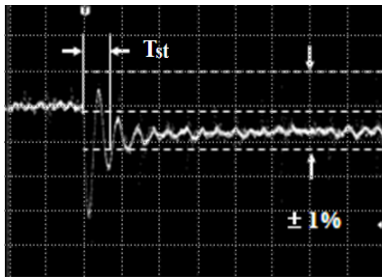
In Condition A through Condition D, gain  $G_2$  and the second cut-off frequency  $f_c$  are assumed to be constant, and the gain  $G_1$  is enlarged. When gain  $G_1$  is enlarged, the first cut-off frequency  $f_a$  or the passing frequency  $f_c$  moves. In this case, it is designed so that  $f_a$  might reach a fixed value. It is seen in these figures that the steady-state error is suppressed because the first gain  $G_1$

is enough high.



Vertical : 100mV/div., Horizontal : 4ms/div.

Fig. 3. Indicial response of digital P-I-D control.



Vertical : 100mV/div., Horizontal : 4ms/div.

Fig. 4. Indicial response of FIR filter method.

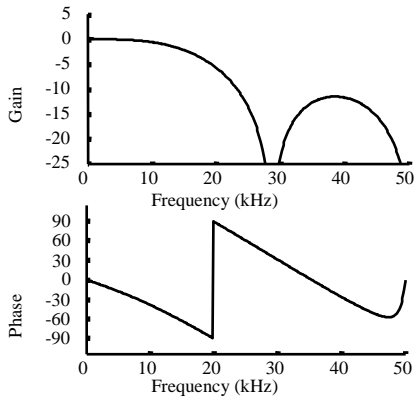


Fig. 5. Frequency characteristics of FIR filter corresponding to Fig.4.

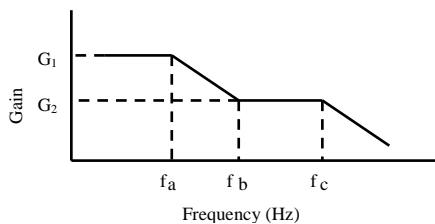


Fig. 6. Definition of parameters in IIR filter.

Table 2 Parameters in each condition

|             | $G_1$ (dB) | $G_2$ (dB) | $f_a$ (Hz) | $f_b$ (Hz) | $f_c$ (Hz) |
|-------------|------------|------------|------------|------------|------------|
| Condition A | 0          | 0          | —          | —          | 1k         |
| Condition B | 10         | 0          | 1          | 2.5        | 1k         |
| Condition C | 20         | 0          | 1          | 9.6        | 1k         |
| Condition D | 40         | 0          | 1          | 97         | 1k         |
| Condition E | 20         | 0          | 1          | 10.3       | 100        |
| Condition F | 20         | 0          | 1          | 9.6        | 10k        |
| Condition G | 40         | 0          | 0.1        | 10         | 10k        |
| Condition H | 40         | 15         | 1          | 10         | 40k        |
| Condition I | 40         | 20         | 1          | 17.5       | 40k        |

The experimental indicial response characteristics of the buck dc-dc converter in Condition A through Condition I are shown in Figs. 8(a) through (i). Moreover, Fig. 8 (d) shows the indicial response in Condition D.

In Figs. 8(a) through (g), the observed undershoot is from 3% to 4% and the observed transient time  $T_{st}$  is large. This numerical data is shown in Table 3. In these figures, the observed undershoot and the observed transient time  $T_{st}$  are not suppressed. However, in Figs. 8(h) and (i), the observed undershoot is less than 2% and the observed transient time  $T_{st}$  is less than 0.4ms as shown in Table 3. Moreover, when derived from the limit cycle suppression is adequate.

Table 3 Dynamic Characteristics of Buck Type Converter

| Condition | Under Shoot(%) | Transient Time(ms) |
|-----------|----------------|--------------------|
| A         | 3.03           | 5.06               |
| B         | 2.89           | 7.04               |
| C         | 3.27           | 7.32               |
| D         | 3.52           | 21.47              |
| E         | 3.92           | 18.05              |
| F         | 2.90           | 2.91               |
| G         | 3.13           | 5.06               |
| H         | 1.76           | 0.34               |
| I         | 1.31           | 0.38               |

In these conditions, gain  $G_1$  and gain  $G_2$  are enlarged, and then the second cut-off frequency  $f_c$  becomes high to maintain stability.  $f_c$  is less than half of the sampling frequency 100kHz. Especially, Condition H has a stable response characteristic compared with that in Condition

I because the second gain is too large under Condition I. Therefore, it is revealed that Condition H has superior characteristics.

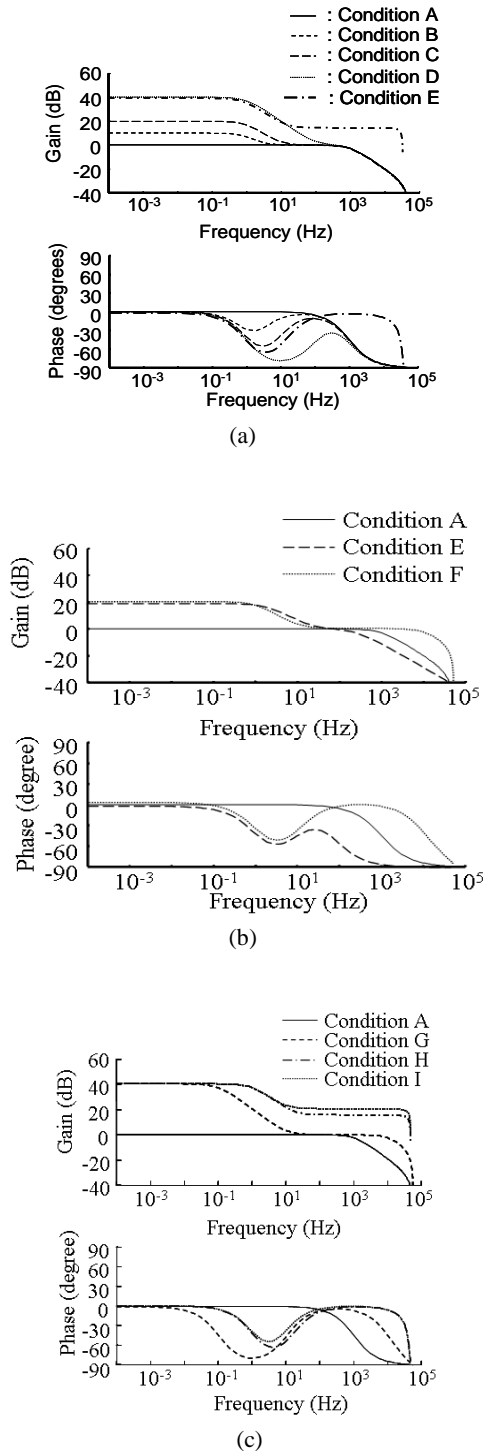
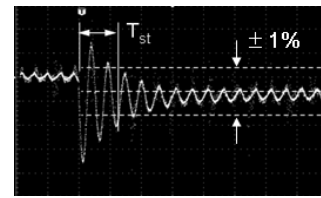


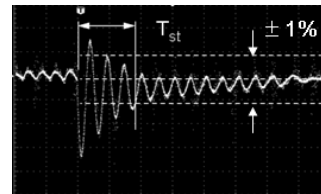
Fig. 7. Frequency characteristics in IIR filter.



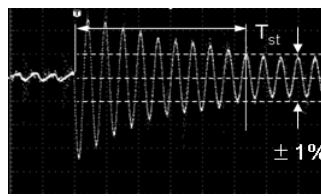
(a) Condition A



(b) Condition B



(c) Condition C



(d) Condition D

Vertical : 100mV/div., Horizontal : 4ms/div.

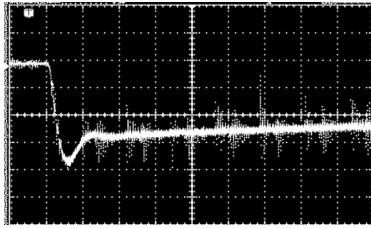
Fig. 8. Indicial response of buck converter with IIR filter.

Figures 9(a) through (i) show the experimental indicial response characteristics of the buck-boost dc-dc converter in Condition A through Condition I in Table 2. The inductance  $L$  is 260  $\mu$  H, the output capacitance  $C$  is 1,880  $\mu$  F, the input voltage is 10V and the others are the same as in Fig. 8.

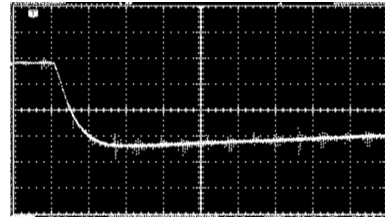
In Figs. 9(a) through (g), the observed undershoot and observed transient time  $T_{st}$  is large as shown in Table 4.

Table 4 Dynamic Characteristics of Buck-Boost Type Converter

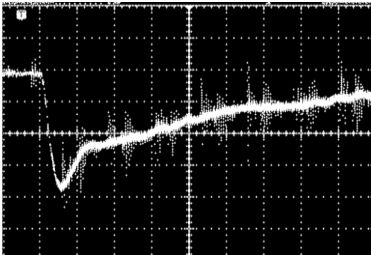
| Condition | Under Shoot(%) | Transient Time(ms) |
|-----------|----------------|--------------------|
| A         | 7.16           | 476.00             |
| B         | 7.20           | 157.00             |
| C         | 6.84           | 40.80              |
| D         | 6.60           | 6.88               |
| E         | 9.68           | 36.60              |
| F         | 6.68           | 36.00              |
| G         | 4.48           | 10.80              |
| H         | 2.66           | 3.92               |
| I         | 2.00           | 2.88               |



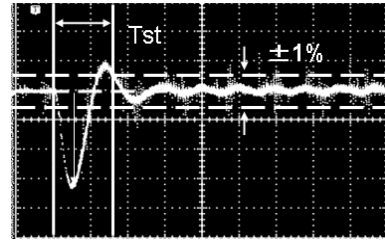
Vertical : 200mV/div, Horizontal : 4ms/div.  
(a) Condition A



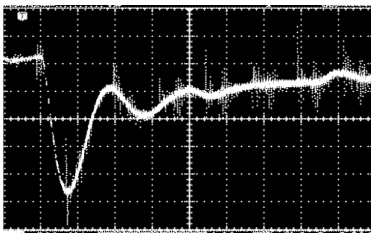
Vertical : 500mV/div, Horizontal : 4ms/div.  
(b) Condition B



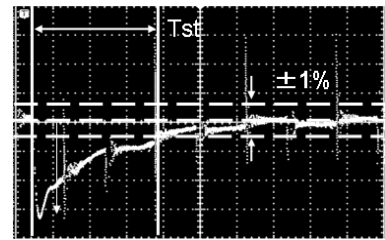
Vertical : 200mV/div, Horizontal : 4ms/div.  
(c) Condition C



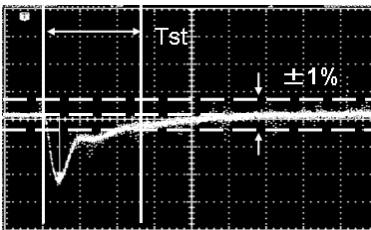
Vertical : 200mV/div, Horizontal : 4ms/div.  
(d) Condition D



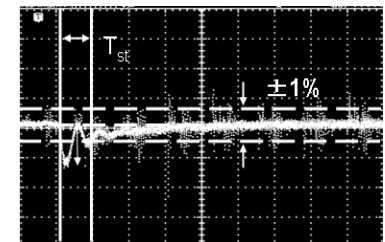
Vertical : 200mV/div, Horizontal : 4ms/div.  
(e) Condition E



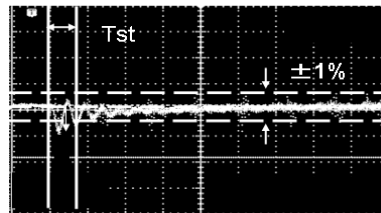
Vertical : 200mV/div, Horizontal : 4ms/div.  
(f) Condition F



Vertical : 200mV/div, Horizontal : 4ms/div.  
(g) Condition G



Vertical : 200mV/div, Horizontal : 4ms/div.  
(h) Condition H



Vertical : 200mV/div, Horizontal : 4ms/div.  
(i) Condition I

Fig. 9. Indicial response of buck-boost converter with IIR filter.

The undershoot is over approximately 5% and the transient time is over approximately 10ms. On the other hand, in Figs. 9(h) and (i), the observed undershoot is less than 3%, the observed transient time  $T_{st}$  is less than 4ms. Under Condition H, the observed waveform has stable transient response characteristics and vibrated phenomena are not observed. The transient time of the buck-boost converter is longer than that of the buck converter because the output capacitance of the buck-boost converter is too large to suppress the output voltage ripple and to maintain the stable state. The oscillation deriving from the limit cycle is also suppressed adequately in Condition H. Therefore, it is revealed that Condition H has also superior characteristics in the digitally buck-boost dc-dc converter with IIR filter.

These results suggest the design criterion of digital control circuit of switching power converters. It is concluded that the first gain  $G_1$ , the second gain  $G_2$  and the second cut-off frequency  $f_c$  are relatively enlarged, and the first cut-off frequency  $f_a$  and the passing frequency  $f_b$  are relatively low in the IIR filter controlled switching dc-dc power converter as shown Condition H in Table 2. Moreover, it is important that the gain decreases at an extremely rapid rate at the second cut-off frequency  $f_c$  as shown in Fig. 7 because  $f_c$  is always less than half of the sampling frequency based on the sampling theory.

#### 4. Conclusions

From the above discussion, it is revealed that the IIR filter control method has good dynamic characteristics. Furthermore, in the IIR filter, it is seen that the oscillation deriving from the limit cycle is suppressed in Condition H. It is concluded that the first gain  $G_1$ , the second gain  $G_2$  and the second cut-off frequency  $f_c$  are relatively enlarged, and the first cut-off frequency  $f_a$  and the passing frequency  $f_b$  are relatively low. Moreover, it is important that the gain decreases at an extremely rapid rate at the second cut-off frequency  $f_c$ .

As a result, in the buck converter, the undershoot is less than 2% and the transient time is less than 0.4ms. On the other hand, in the buck-boost converter, the

undershoot is about 3%. However, the transient time is approximately more than 4ms because the output capacitance is too large to suppress the output voltage ripple in this type of converter.

These results are very useful for realizing a digitally controlled switching power converter using a DSP.

#### Acknowledgment

This work is supported in part by the Grant-in-Aid for Scientific Research (No.18310117) of JSPS (Japan Society for the Promotion of Science) and the Ministry of Education, Science, Sports and Culture.

#### References

- [1] L. Guo, J. Y. Hung and R. M. Nelms, "PID controller modifications to improve steady-state-- performance of digital controllers for buck and boost converters," *Proceedings of Seventeenth Annual IEEE Applied Power Electronics Conference*, No.9.3, Dallas, pp. 381-388, March 2002.
- [2] M. Nashed, "Design of a digital PWM controller for a soft switching SEPIC converter," *Journal of Power Electronics*, Vol. 4, No. 3, pp. 152-160, 2004.
- [3] C. Sudhakarababu and M. Veerachary, "DSP based control of interleaved boost converter," *Journal of Power Electronics*, Vol. 5, No. 3, pp. 180-189, 2005.
- [4] H. Bae, J. Yang, J. Lee and B. Cho, "Digital state feedback current control using the pole placement technique," *Journal of Power Electronics*, Vol. 7, No. 3, pp. 213-221, 2007.
- [5] F. Kurokawa, M. Sasaki, S. Hiura and H. Matsuo, "1MHz high-speed digitally controlled dc-dc converter," *IEICE Trans. on Communications*, Vol. E87-B, No. 12, pp. 3437-3442, Dec. 2004.
- [6] H. Hu, V. Yousefzadeh and D. Maksimovic, "Nonlinear control for improved dynamic response of digitally controlled dc-dc converters," *IEEE PESC'06 Record*, Jeju, pp.2584-2590, June 2006.
- [7] V. Yousefzadeh, A. Babazadeh, B. Ramachandram and E. Alarcon, "Proximate time-optimal digital control for dc-dc converters," *IEEE PESC'07 Record*, Orlando, pp.124-130, June 2007.
- [8] Z. Lukic, C. Blake, S. C. Huerta and A. Prodic, "Universal and fault-tolerant multiphase digital PWM controller IC for high-frequency dc-dc converters," *Proc.*

of *IEEE APEC'07*, Anaheim, pp. 42-47, Feb. 2007.

- [9] F. Kurokawa, T. Sato, H. Matsuo and H. Eto, "Output characteristics of dc-dc converter with DSP control," *Proceeding of IEEE International Telecommunications and energy conference*, Montreal, pp. 421-426, Oct. 2002.
- [10] F. Kurokawa, W. Okamoto and H. Matsuo, "A comparison of steady-state characteristics of buck type dc-dc converter using DSP," *IEICE Trans. on Communications*, Vol. J89-B, No. 5, pp. 673-681, May 2006.
- [11] B. Mulgrew, P. Grant and J. Thompson, "Digital signal processing," Macmillan Press Ltd., London, Chap. 5, 1999.



**Fujio Kurokawa** received his B. S. degree in electronic engineering from the Fukuoka Institute of Technology, Fukuoka, Japan, in 1976, and Dr. Eng. Degree from Osaka Prefecture University, Sakai, Japan, in 1988. Since 1984, he has been with the Faculty of Engineering, Nagasaki University, and is currently an Associate Professor of Electrical and Electronic Engineering. His research and teaching interests are in the area of electronic circuits, power electronics and image processing system. Dr. Kurokawa is a senior member of the Power Electronics Society of IEEE, the Institute of Electrical Engineers of Japan, the Illuminating Engineering Institute of Japan, the Institute of Image Information and Television Engineers of Japan and the Information Processing Society of Japan.



**Masashi Okamatsu** was born in Fukuoka Prefecture, Japan, on February 27, 1985. He received his B.S. degree in electrical and electronic engineering from Nagasaki University, Nagasaki, Japan, in 2007. His research interests are in switching power converters and their digital control.



**Taku Ishibashi** was born in Fukuoka Prefecture, Japan, on July 7, 1986. He is a student in the Department of Electrical and Electronic Engineering, Nagasaki University, Nagasaki, Japan. His research interests are in switching power converters and their digital control.



**Yasuyuki Nishida** was born in Japan on October 19, 1956. He studied Electrical Engineering as an undergraduate at Nihon University, and Power Electronics as a graduate student at Tokyo Denki University. He received his Ph.D. in Electrical Engineering from Yamaguchi University in 1998. From 1998 to 2009, he was with Nihon University in Japan as a lecturer and an associate-professor in the department of Electrical & Electronic Engineering. Since 2009, he has been with the Chiba Institute of Technology in Japan as a full-professor in the department of Electrical, Electronics and Computer Engineering, Faculty of Engineering. He worked for the Swiss Federal Institute of Technology (ETH) Zurich from April to September 2006 as a visiting researcher. The focus of his current research is on single-phase and three-phase PFCs including "Passive and Hybrid PFCs", "Current-Source-Type PWM PFCs." Dr. Nishida's interests also include PE Education tools and systems. He is a senior member and an IAS board officer of the IEEJ and a member of IEEE, EPE and JIPE. He has also served as the vice-chair of Technical Program Committee of PCC-Nagoya-2007, an advisory board member of the international conference on PCIM and a member of other international conferences.