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DSP-Based Digital Controller for Multi-Phase Synchronous Buck Converters

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ABSTRACT

This paper represents a design and implementation of a digital controller for a multi-phase synchronous buck converter (SBC) using a digital signal processor (DSP). The multi-phase SBC has generally been used for a voltage regulation module (VRM) of a microprocessor because of its high current handling capability at a low output voltage. The VRM requires high control performance of tight output regulation, high slew rate, and load sharing capability of multiple converters. In order to achieve these requirements, the design and implementation of a digital control system for a multi-phase SBC are presented in this paper. The digital PWM generation, current sensing, and voltage and current controller using a DSP TMS320F2812 are considered. The experimental results are provided to show the validity of the implemented digital control system.

Keywords: Synchronous buck converter, Voltage regulation module, Digital controller, Parallel operation, Digital signal processor

1. Introduction

In recent years, high performance microprocessors with a high integration density and a fast clock frequency need a high performance DC/DC converter, known as a voltage regulation module (VRM) to deliver a high quality power. Fig. 1 shows a typical desktop computer power supply with a VRM. The requirements for a VRM are the low voltage and high current output, high current slew rate, low output impedance and tight output voltage regulation.

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A multi-phase synchronous buck converter (SBC) is generally used for VRM applications because of its high current handling capability at a low output voltage. In addition, the interleaved operation of the multiple buck converters can provide the advantage of reducing the current and voltage ripples. However, this converter needs more complicated control techniques for the interleaved and synchronous operation of the MOSFET switches and load sharing of parallel converters [1]-[7].

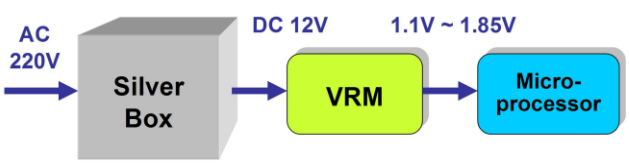

Fig. 1. Typical configuration of desktop computer power supply.

Analog PWM controllers have been generally used for the high frequency DC/DC converters. However, the application of a digital controller to the high frequency DC/DC converters has been recently studied. The digital controller for the VRM with a multi-phase SBC provides advantages such as the possibility of using modern control techniques, precise control of the PWM timing, reliability improvements against aging and noises, and intelligent power management and fault diagnosis.

In this paper, a design and implementation of a digital controller using a digital signal processor (DSP) for a multi-phase SBC is presented. The multi-phase digital PWM and current sensing techniques are first investigated. The design of digital current and voltage controllers based on the averaged small signal model are also presented. The proposed controller is implemented for the four-phase SBC using the TMS320F2812 and the experimental results are provided to show the validity of the controller design.

2. Control System of Multi-Phase SBC

Fig. 2 shows the digital control system of the four-phase SBC for a VRM, which consists of the four parallel SBCs, current sensing circuits and a DSP-based digital controller with a multi-phase digital PWM generator.

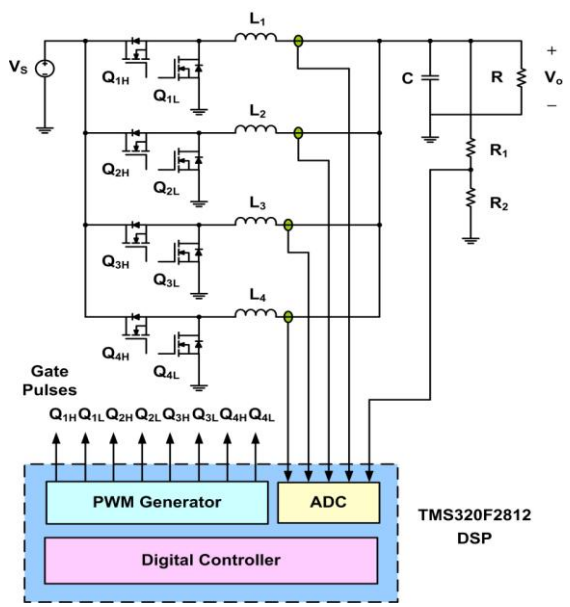

Fig. 2. Configuration of the four-phase SBC control system.

The interleaved PWM control is employed to reduce the current and voltage ripples. The lossless current sensing technique is also considered and the measured current signals are fed to the DSP controller using A/D converters. The control algorithms for the current and voltage regulation are implemented using the software of the DSP.

2.1 Digital PWM Generation

Eight gate signals are needed to control the four-phase SBC and can be described as shown in Fig 3, where the phase shift between two adjacent converters in N-phase converter system is given as

$$\varphi_d = \frac{360^o}{N} \tag{1}$$

The time delay of the gate signal for the *i*-th converter is also derived as

$$\varphi_i = \frac{(i-1)\cdot T}{N} \tag{2}$$

where i = 1, 2, 3, …, N, and T denotes the switching period.

The digital PWM generation method used in the proposed control system is described in Figs. 4 and 5. This method is implemented using the timers in the TMS320F2812 DSP. Fig. 4 shows the timing diagram of the proposed PWM generation method. Two independent general purpose (GP) timers in the DSP are used to generate dual carriers with a phase difference of 90 degrees. The gate pu

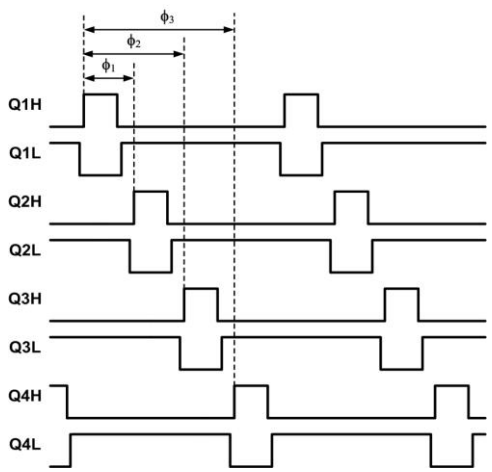

Fig. 3. Gate signals for the four-phase SBC.

lses for Phase 1 and 2 are synchronized with the top points of GP timer 1 and 2, respectively, while Phase 3 and 4 are synchronized with the bottom points of both timers. The inductor currents in each phase converters are sampled at the bottom of GP timer 1 and 2. The PWM references for Phase 1 to 4 converters are calculated after the current sampling and are updated just before the bottom points of the GP timer 1 for Phase 1 and 2, and the top points of GP timer for Phase 3 and 4, respectively. The gate pulse generation methods for Phase 1, 2 and Phase 3, 4 are different as shown in Fig. 5. The gate pulse is high when the carrier (timer) is greater than the PWM reference (d_{ref}) for Phase 1 and 2. Whereas the PWM reference of 2_n-d_{ref} is loaded for Phase 3 and 4, and the gate pulse is active when the PWM reference is greater than the carrier.

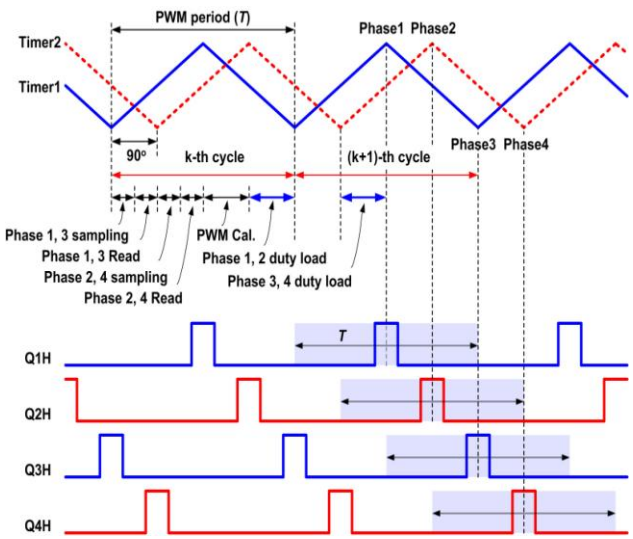

Fig. 4. Digital PWM generation timing diagram for the four-phase SBC.

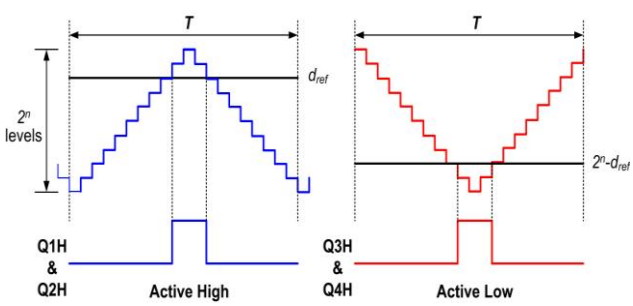

Fig. 5. Gate pulse generation methods for Phase 1, 2 and 3, 4.

2.2 Current Sensing

The inductor current sensing is important for the average current mode control and even current sharing. Since the VRM has the low voltage and high current characteristics, the shunt resistor causes the high voltage drop, which results in high conduction loss. Thus, the lossless current sensing is needed to improve the converter efficiency.

The inductor current sensing method using the circuit shown in Fig. 6 is utilized in this system. The voltage V_L across the inductor can be given as

$$V_L = (R_L + sL)\cdot I_L \tag{3}$$

The voltage across the capacitor C_s can be derived as

$$\begin{aligned} V_C &= \frac{1/sC}{R_s + 1/sC}\cdot V_L = \frac{(R_L + sL)\cdot I_L}{1 + sR_sC_s} \\ &= R_L \cdot \left(\frac{1+s\tau_L}{1+s\tau_s}\right)\cdot I_L \end{aligned} \tag{4}$$

where $\tau_L = L/R_L$, $\tau_s = R_sC_s$. If the time constant of the inductor and RC circuit as $\tau_L = \tau_s$, the capacitor voltage can be represented as

$$V_C = R_L I_L \tag{5}$$

It is known from this relation that the capacitor voltage is proportional to the inductor current under the assumption that R_L is constant. Fig. 6 shows the inductor current and capacitor voltage waveforms.

The simulated waveform is also shown in Fig. 8, where the device parameters are L=4.2uH, R_L=1$m\Omega$, C_s=0.22uF, and R_s= 19$k\Omega$, respectively. In practice, since the capacitor voltage v_{cs} is very small, the method of minimizing the effects of the measurement noise should be considered.

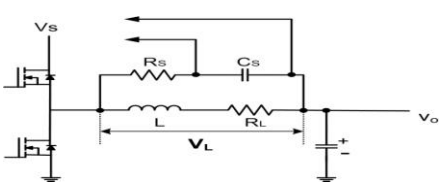

Fig. 6. Inductor current sensing circuit.

2.3 Current Sampling

The inductor current has unavoidable ripple components. Thus, the sampled average current has different values for the different sampling instants. In order to obtain the average current, the inductor currents are sampled at the bottom points of timer 1 and 2. Fig. 9 shows the sampling instants of the inductor currents in the proposed control. The inductor currents for Phase 1 and 3 converters are sampled at the bottom point of timer 1, where the sampled currents are the same with the average inductor currents. The current sampling for Phase 2 and 4 is synchronized with the bottom point of timer 2.

3. Design of Digital Controller

3.1 Small Signal Model

The small signal model of the first converter of the four-phase SBC can be represented as shown in Fig. 10, where the remained three converters are assumed as a current source. The block diagram of this model can also be described as shown in Fig. 11.

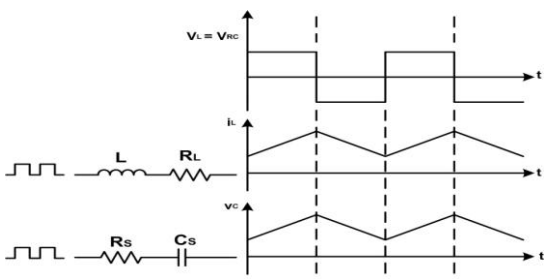

Fig. 7. Inductor current and capacitor voltage waveform.

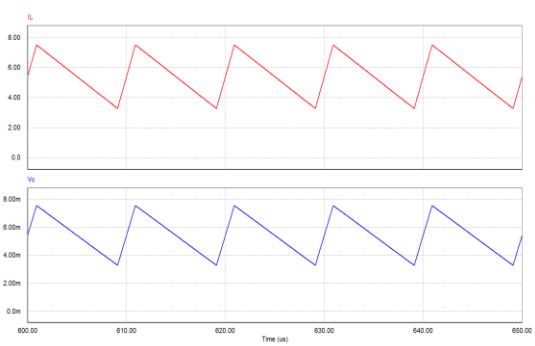

Fig. 8. Simulated results for the inductor current sensing method.(Upper: inductor current, Lower: capacitor (C_s) voltage).

The state equation of the small signal model for the i-th converter can be expressed as

$$\frac{di_{Li}}{dt} = -\frac{1}{L_i}v_o + \frac{V_s}{L_i}\hat{d}_i + \frac{D_i V_s}{L_i} \tag{6}$$

$$\frac{dv_o}{dt} = \frac{i_{Li}}{C} - \frac{1}{RC}v_o + \frac{1}{C}\sum_{j\neq i}^{N} i_{Lj} \tag{7}$$

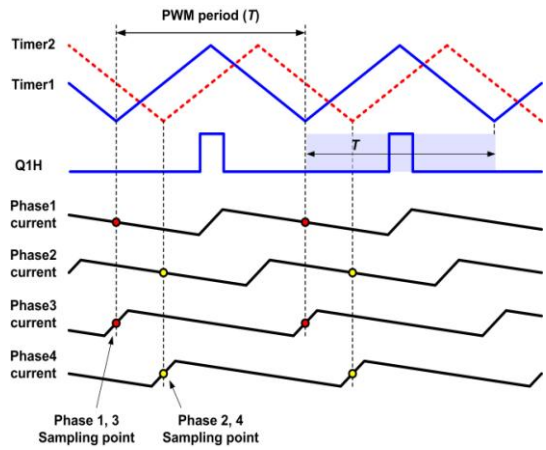

Fig. 9. Sampling points of the inductor currents.

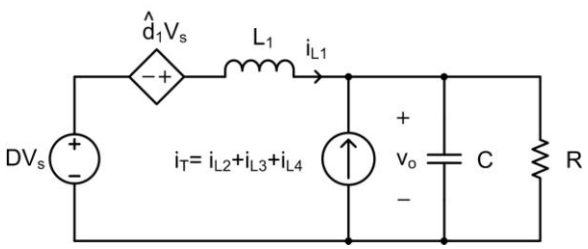

Fig. 10. Signal model for the first converter of the four-phase SBC.

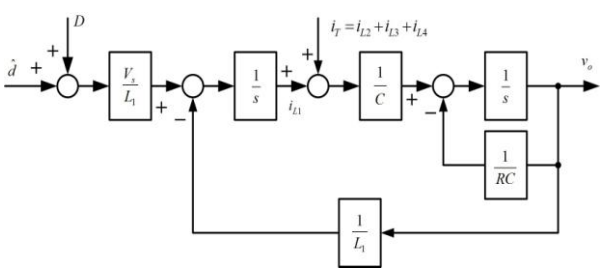

Fig. 11. Block diagram of the small signal model for the first converter of four-phase SBC.

where i = 1, 2, …, N, and N is the number of the parallel SBCs. The symbols L_i, C, i_{Li}, V_s and v_o mean the inductance of the i-th converter, output capacitance, inductor current of the i-th converter, input voltage and output voltage, respectively. The duty cycle of the i-th converter is defined as

$$d_i = D_i + \hat{d}_i \tag{8}$$

where D_i and $\hat{d}_i$ represent the fixed and perturbed terms of the duty, respectively.

3.2 Predictive Current Controller

In order to ensure the fast dynamic response of the inductor current, a predictive current controller is used for the current control loop. The control input for the i-th converter using a simple Euler method can be derived from (6) as

$$\hat{d}_i(k) = \frac{L_i}{V_s}\frac{i_{Li}^*(k+1) - i_{Li}(k)}{T} + \frac{v_o(k)}{V_s} - D_i \tag{9}$$

where $i_{L1}^*(k+1)$ denotes the current reference at the (k+1)-th instant as shown in Fig. 12.

3.3 PI Controller for Output Voltage Regulation

Since the inductor current is controlled by the inner-loop current controller, the current dynamics can be neglected in designing the outer voltage control loop. Thus, the block diagram for the voltage control loop can be simplified as shown in Fig. 13.

The open loop transfer function of the voltage control loop in a discrete-time domain is given as

$$G_d(z) = Z\left[\frac{(1-e^{-sT})}{s} G(s)G_{dealy}(s)\right] \tag{10}$$

Where

$$G(s) = \frac{1}{C}\cdot\frac{1}{s+\frac{1}{RC}} \tag{11}$$

and $Z[\cdot]$ means z-transform of the continuous-time domain function. The transfer function $G_{dealy}(s)$ is the time delay of the control system given as

$$G_{dealy}(s) = e^{-T_d s} \tag{12}$$

where T_d is the delay time. The PI plus decoupling controller is used as a voltage controller. The PI controller can be represented in a discrete-time domain as

$$G_c(z) = K_P + \frac{K_I T}{z-1} \tag{13}$$

where K_P and K_I denote the proportional and integral gains, respectively. The voltage controller including the decoupling term is given as

$$i_{Li}(k) = i_{Pi}(k) + i_{Ii}(k) + i_{Ci}(k) \tag{14}$$

Where

$$i_{Pi}(k) = K_P e(k) \tag{15}$$

$$i_{Ii}(k) = i_{Ii}(k-1) + K_I e(k)T \tag{16}$$

$$i_{Ci}(k) = -\sum_{j=i}^{N} i_{Lj}(k) \tag{17}$$

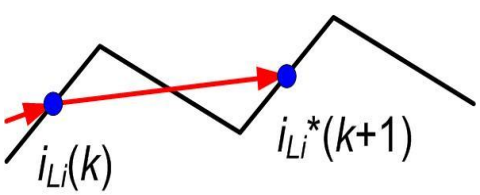

Fig. 12. Current reference at the (k+1)-th instant.

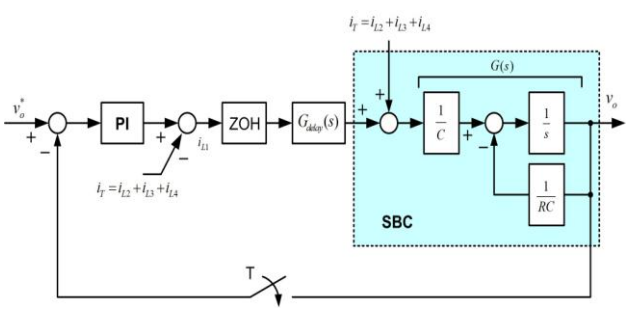

Fig. 13. Block diagram of voltage controller.

4. Experiments

The experimental study is carried out for the four-phase SBC to verify the validity of the proposed control system. The experimental parameters are given in Table 1.

Table 1 Experimental parameters

Item	Value	Item	Value
Input voltage (V_s)	12V	Output voltage (v_o)	1.4V
Filter capacitance (C)	440uF	Filter inductance (L_1=L_2=L_3=L_4)	4.2uH
Switching freq. (f_s)	100kHz	Voltage ripple (v_o)	15mV

The gains of the PI controller are given as K_P = 8.0, K_I = 200, T = 10us, and one step time delay is considered as T_d = 10us. For these parameters, the Bode plot of the closed loop system can be described as shown in Fig. 14, where the gain and phase margins are 18dB and 81.5 degrees, respectively.

Figs. 15 and 16 show the gate pulses for the four-phase SBC, which represents the high and low side gate pulses with a phase delay of 90 degrees. It can be shown from these figures that the gate pulses are successfully generated from the implemented PWM generator.

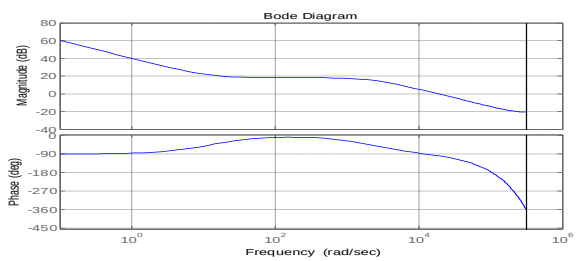

Fig. 14. Frequency response of the closed loop system.

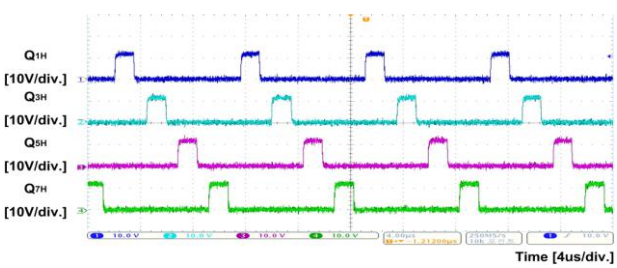

Fig. 15. High side gate pulse waveform.

Fig. 17 shows the inductor current waveforms of the four SBCs and the input current of the output capacitor, i.e., the sum of the four inductor currents. It is noted from this figure that the effective ripple current can be reduced by using the interleaved operation of the four-phase converter.

Fig. 18 shows the output voltage and current waveforms when the load resistance is abruptly changed from R=0.1Ω to R=0.06Ω. The output voltage reference is 1.4V. The results show that the output voltage can be well controlled under the step load changes.

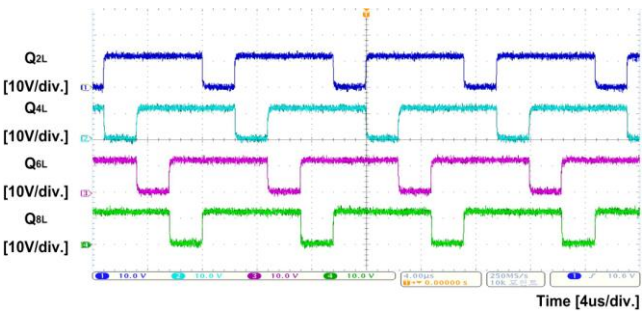

Fig. 16. Low side gate pulse waveform.

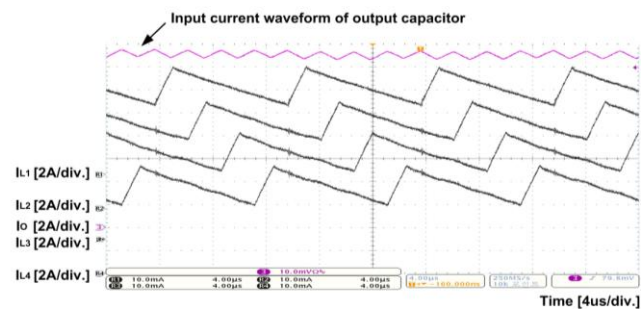

Fig. 17. Inductor current waveforms of the four SBCs and the input current of the output capacitor.

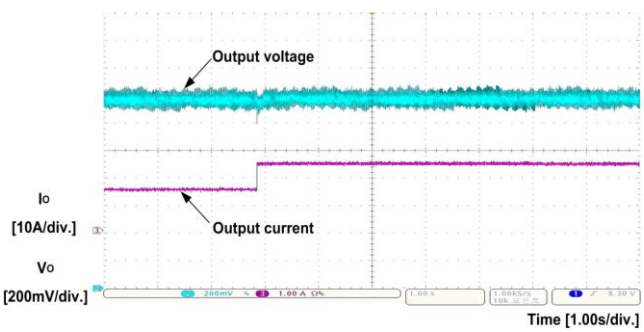

Fig. 18. Output voltage and load current waveforms.

5. Conclusions

The design and implementation of the digital controller for the VRM using the multi-phase SBCs have been described in this paper. The implementation methods of the digital PWM and current sensing were presented. The digital current and voltage controllers were designed using the averaged small signal model of the four-phase SBCs. The experimental studies were finally carried out for the digital control system of the four-phase SBC using the DSP TMS320F2812. The results greatly verify the validity of the proposed digital control system. It is noted from the results of this paper that the digital VRM controllers show a good performance over the conventional analog controllers and will be used for the high performance and reliable controller for the VRM applications. The development of the full custom ASIC controller can be considered as a further work for commercializing the digital VRM controller.

Acknowledgement

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