

A Novel Ripple-Reduced DC-DC Converter

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ABSTRACT

A DC/DC converter generally needs to work under high switching frequency when used as an adjustable power supply to reduce the size of magnetic elements such as inductors, transformers and capacitors, but with the rising of the switch frequency, the switch losses will increase and the efficiency will reduce. Recently, to solve these problems, research is actively being done on a soft switching method that can be applied under high frequency and on a PWM converter that can be applied under low frequency such as a multi-level topology. In this paper a novel DC-DC conversion method for reducing the ripple of output voltage is proposed. In the proposed converter, buck converters are connected in series to generate the output voltage. By using this method, the ripple of output voltage can be reduced compared to a conventional buck converter. Particularly when output voltage is low, the number of acting switching elements is less and the result of ripple reduction is more obvious. It is expected that the converter proposed in this paper could be very useful in the case of wide-range output voltage.

Keywords: DC/DC converter, Multi-level, Ripple reducing, Wide-range output

1. Introduction

With the recent development of industrial technologies and requirements for new energy, current research in this field is mostly about adjustable DC power supplies and DC-DC conversion technology^[1,2]. Generally, the voltage-source PWM DC/DC converter has been widely used in many technical areas. In order to reduce the ripple of output voltage, many circuit typologies have been proposed recently^[3]. Generally speaking, a DC/DC converter usually works under high frequency to reduce the size of inductors, transformers and capacitors, etc.

However, the higher the switching frequency, the more losses suffered, which results in a new problem of efficiency reduction. Recent studies mainly focus on two fields: one is on software switching methods to reduce the losses of switching under high working frequency conditions, and the other is on the structure of multi-level converters under low frequency working conditions^[4,5].

Although software switching methods can reduce switching losses, the peak value of voltage or current will rise at the same time, so that the rated value of switch elements has to be improved. Furthermore, additional protection circuit parts are also needed.

Multi-level conversion technology has the advantage of reducing output voltage ripple even under low switching frequency. Nevertheless, the number of switch elements has to be added according to the increase in levels. The losses of switch elements will increase according to the

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increase of on-switch elements.

Recent studies of multi-level converters are paid more attention for AC inverters while there are not enough studies on DC/DC converters [6]. In this paper, a new multi-level DC/DC conversion method is presented to reduce the output voltage ripple of DC/DC converters. The proposed converter producing multi-voltage is made of buck converters in series, which reduces the ripple of output voltage compared to traditional buck converters. Furthermore, the number of acting switch elements will be reduced when the output voltage is lower, so that the multi-level DC/DC conversion method has a special advantage under lower output voltage. The proposed converter is especially suited for application to wide range output.

2. Multi-level Conversion Method

2.1 Proposed Multi-level Conversion Method

The structure of a conventional non-isolated buck converter is shown as Figure 1. In this type of converter, by adjusting the duty ratio (D) of the switch output voltage, the filter input voltage is

$$V_f = DV_i + \frac{2V_i}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\pi D) e^{j(2\pi n)t} \quad (1)$$

From formula (1) it can be determined that the input voltage of the filter is composed of DC composition and the harmonics which are integral times the fundamental frequency. If the harmonics can be filtrated through the filter, the output voltage will only be related to DC, explained in formula (2)

$$V_o = DV_i \quad (2)$$

The ripple of inductance current in the DC/DC converter shown as Figure 1 is

$$\Delta I_L = \frac{V_i - V_o}{L} DT_s \quad (3)$$

The ripple of the capacitor output voltage can be described as

$$\Delta v_o = \frac{1}{LC} \frac{V_i(1-D)D}{8f_s^2} \quad (4)$$

It is calculated that the voltage ripple is maximum when the duty ratio is set to 0.5 from the differential of formula (4). This maximum ripple of the output voltage is

$$\Delta v_{o\max} = \frac{1}{32} \frac{V_i}{LCf_s^2} \quad (5)$$

From Formula (5) we know that the output voltage ripple of the DC/DC converter is determined by the collective effect of the switching frequency, inductance, capacitor, duty ratio and input voltage, etc. Therefore, the output voltage ripple can be reduced in many ways such as by improving the frequency of switching, increasing filter inductance or capacitance, or reducing the output voltage.

However, increasing the switch frequency will increase the switch loss and reduce the efficiency, and increasing the filter inductance or capacitance will cause an increase of volume and system cost.

In this paper, to reduce the output voltage ripple, a method of reducing the input voltage is proposed. This new multi-level DC/DC converter structure is presented in Figure 2. It consists of traditional DC/DC converters in series. The output parts of Buck converters are connected with diode in series which ensures the output isolation of all converters. In each level the middle diode and switching element are connected to the negative point of the up buck converter.

As to the conventional multi-level inverter, with the increase of levels and the number of switch elements, diodes and capacitors have to be added rapidly. However, the number of switch elements and the number of diodes will be reduced by N separately in the proposed N-level DC/DC converter. The power loss can be reduced by minimizing the acting levels according to the level of generating voltage.

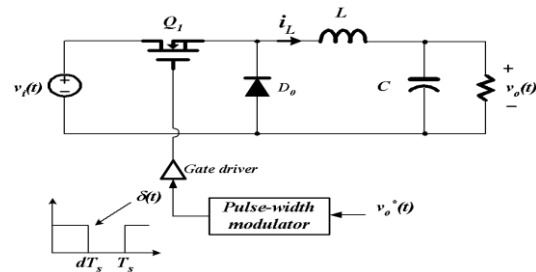


Fig. 1. Conventional non-isolated buck converter.

The output voltage ripple of the N-level converter in Figure 2 is described in formula (6).

$$\Delta v_o = \frac{1}{32N} \frac{V_i}{LCf_s^2} \tag{6}$$

It can be determined that the output voltage ripple is reduced to 1/N.

Figure 5(b) shows the current flowing when the level is 2, while the switch Q1 of the first buck converter is on and the switch Q2 of the second buck converter is activated by the PWM signal.

When Q2 is on, the direction of current is Q1-Q2-D2-L-C. Finally, twice the input voltage will be added to the input port of the filter. When Q2 is off, the direction of current is Q1-D1-L-C. Finally, input voltage will be added to the input port of the filter. Figure 5(c) shows the current flowing when the level is 3, when Q1 and Q2 is on and Q3 is activated by the PWM signal. The voltage on the input port of the filter will be 3 or twice the

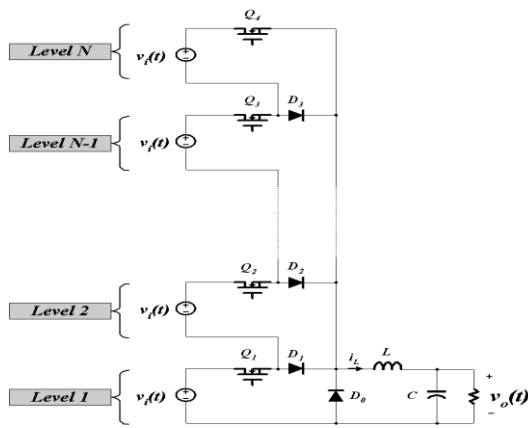


Fig. 2. Proposed multi-level DC/DC converter.

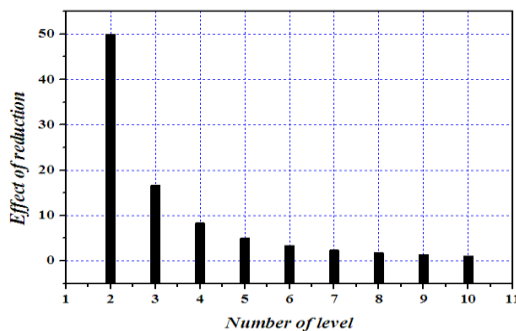


Fig. 3. Reduction effect of ripple according to levels.

input voltage according to the On/Off state of Q3. Figure 5(d) shows the current flowing when the level is 4. Similarly, it can be determined that the voltage on the input port of the filter will be 3 or 4 times the input voltage according to the On/Off state of Q3. Thus, the voltage added to the filter according to the On/Off state of the upper switch can be seen in Formula (7).

$$\begin{aligned} V_{on} &= nV_i \\ V_{off} &= (n-1)V_i \end{aligned} \tag{7}$$

From formula (6) it can be seen that the added voltage to the filter is N or N-1 times the input voltage according to the switch states (On/Off) of different levels.

Figure 6 shows the filter voltage and the switch signals of different levels applied in the proposed multi-level DC/DC converter.

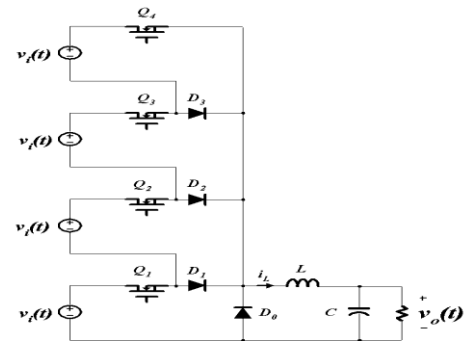


Fig. 4. Proposed 4-level DC/DC converter.

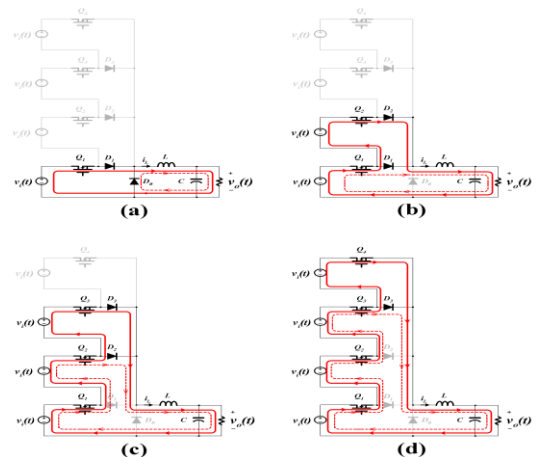


Fig. 5. Operation mode of 4-level DC/DC converter. (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4

In Figure 6 the output voltage of the proposed multilevel DC/DC converter according to the duty ratio of the upper switch is shown as

$$V_o = (n - 1 + D)V_i \tag{8}$$

2.2 Structure of the Controller

The filter of the DC/DC converter is shown in Figure 7. The inductance designed to ensure the current is continuous at least load and the capacitance is decided by the ripple ratio.

Here, the switching frequency is set to 10 [kHz]. On the input side, the 4 levels of 80[V] can generate 320[V] maximum voltage. The lowest load current is set to 1A and the maximum ripple of voltage is set to 0.25[V]. Then the inductance is calculated as 1 [mH] and the capacitor is calculated as 100[uF]. The transform equation of the filter input is shown as formula (9).

$$H(s) = \frac{1/LC}{s^2 + 1/RCs + 1/LC} = \frac{10^7}{s^2 + 333s + 10^7} \tag{9}$$

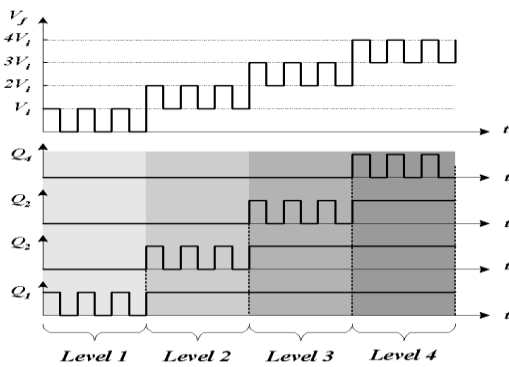


Fig. 6. Switching signal and filter voltage on levels.

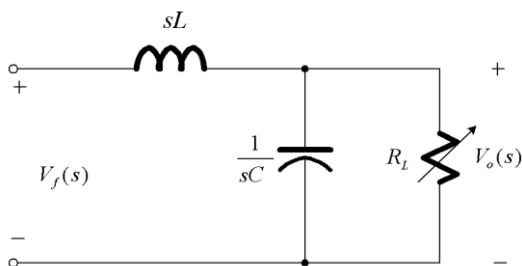


Fig. 7. Filter of DC/DC converter.

On rated voltage, the natural frequency (f_n) is 500[Hz] and the damping ratio (δ) is about 0.33. The controller is necessary because the overshoot is large. The controller consists of a voltage controller including an inner current controller. The controller construction is shown as Figure 8.

In Figure 8, the time constant (τ) is R_2C_1 and the current gain is R_2R_4/R_1R_3 . In the current controller, the time constant is set to 1 [ms] and the gain is set to 0.2. In the voltage controller, the time constant is set to 10 [ms] and the gain is set to 0.2.

The control block of the proposed multilevel DC/DC converter is shown as Figure 9.

As shown in the figure, through the PI controller the reference current is generated by the error between the reference voltage and the output voltage. Then the reference current and the real current are compared in the inner current controller. The result can generate the PWM signals. The carrier wave that is used to generate the PWM signals is set to 10 [kHz].

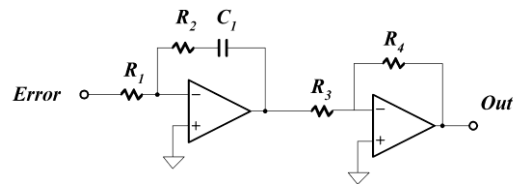


Fig. 8. PI controller circuit.

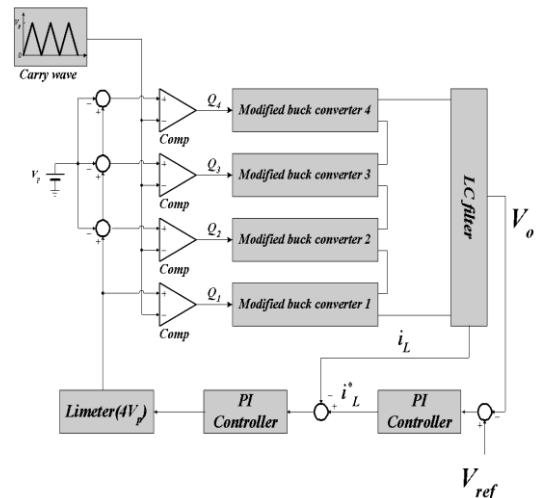


Fig. 9. Control block of multi-level DC/DC converter.

This multilevel DC/DC converter generates the maximum voltage when the PWM reference value is four times the carrier-wave value. The signal on 1 level is made by comparing the PWM reference value and the Carrier-wave. The upper level signal is made by comparing the Carrier-wave and the difference between the PWM reference and the Carrier-wave. By just doing this repeatedly, the right switching signals that can generate the wanted voltage can be determined.

3. Simulation and Results

Figure 10 shows the PSIM-simulation circuit to test the rationality of the proposed 4-level DC/DC converter. In order to compare with the results of the conventional buck converter, both the controller and filter are defined with the same parameters in the simulation.

Figure 11 shows the voltage of the filter, the current of the conductor and the output voltage, respectively, in the proposed converter and the conventional buck converter when the output voltage is set to 200[V]. As shown in the figure, the voltage of the filter is 0 and 320[V] in the conventional buck converter. In the proposed converter, the second level voltage is 160[V] and the third level voltage is 320[V]. Thus, in the conventional buck converter, the current ripple is about 7.4[A] and in the proposed converter, it is about 2[A]. 7.4[A] is about 3.7 times 2[A]. Using the same capacitor, the ripple of the proposed converter is smaller.

The harmonics analysis of the filter input voltage is shown as Figure 12. The harmonics of the switch on/off are smaller in the proposed converter than in the conventional buck converter.

When the output voltage is 160[V] (the maximum ripple in the conventional buck converter), the output of the proposed converter and conventional buck converter are compared in Figure 13. The output voltage ripple is about 1[V] in the conventional buck converter; in the proposed converter the 2 levels are completely in the "On" state, so the ripple is 0.

When the reference voltage is set to 200[V] filter voltage, the inductance voltage and output voltage in the proposed converter and conventional buck converter are compared in Figure 14. Here, the parameter of the current and

voltage controller are the same. It can be determined that the dynamic characteristics are similar between them.

Figure 15 shows a photo of the proposed DC-DC multilevel converter. Figure 16 shows the input voltage, output voltage and current of the filter in the multilevel converter. It is obvious that the input voltage of the filter appeared in level sequence and the current ripple is affected by the switching signals generating each level voltage.

When the reference voltage is 350[V] and load is changed as 0.4-0.8-1.2-0.8[kW] in the sequence, the output voltage, output current and multilevel voltage are shown as Figure 17. Though the load is changed quickly, the output voltage is still stable. When the load is 400[W] and the reference voltage is 350[V], the output voltage, output current and multilevel voltage are shown as Figure 18.

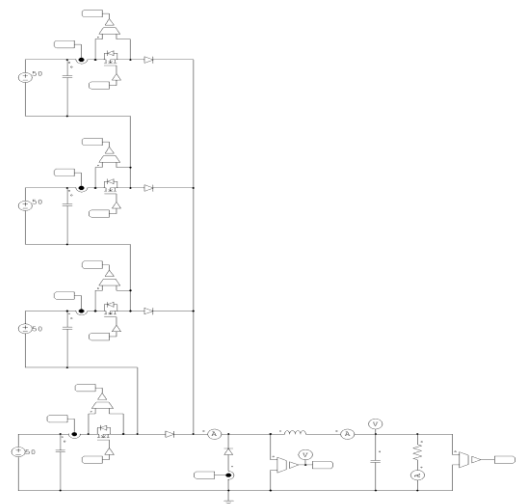


Fig. 10. Simulation circuit.

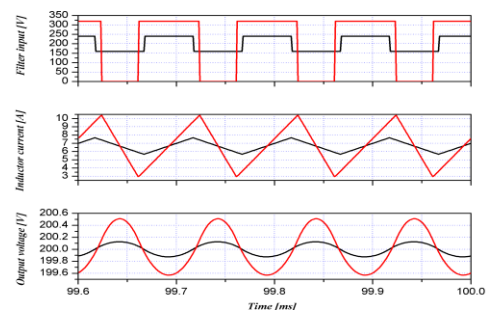


Fig. 11. Waveforms at 200[V] output voltage.

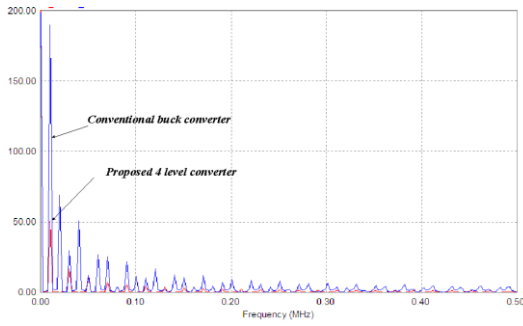


Fig. 12. Harmonics analysis on filter input voltage.

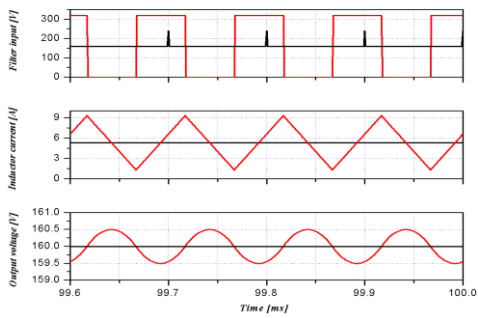


Fig. 13. Ripple at 160[V] output voltage.

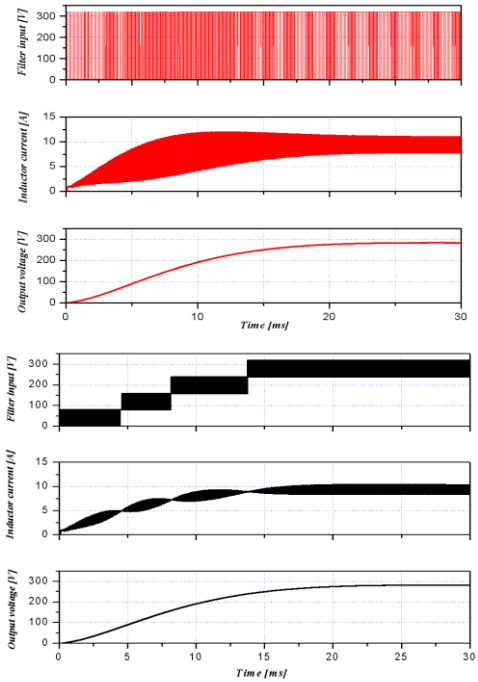


Fig. 14. Dynamic characters compare.

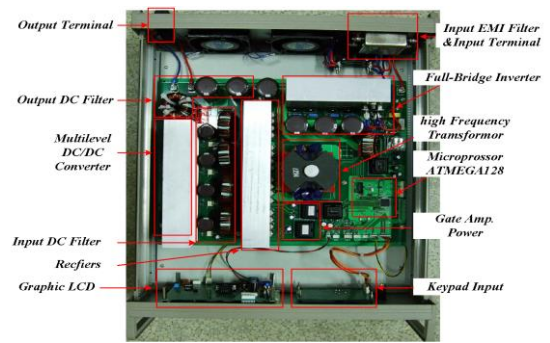


Fig. 15. Photo of the proposed converter.

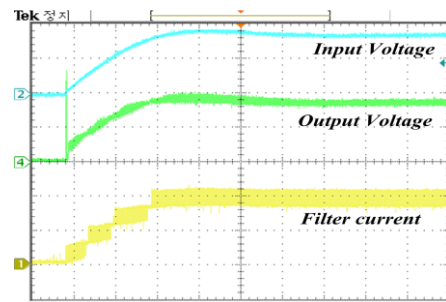


Fig. 16. Input voltages, output voltage and current of the filter in multilevel converter.

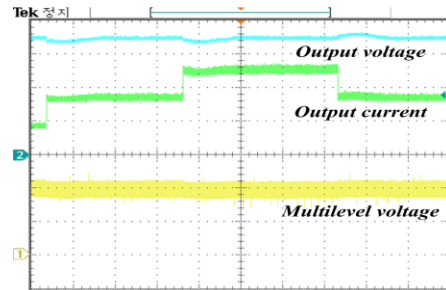


Fig. 17. Output at variational load.

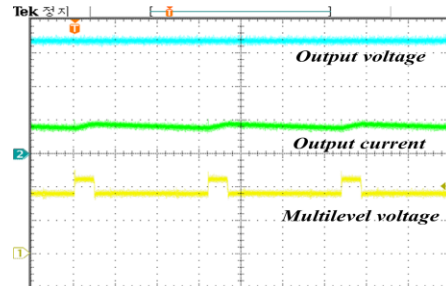


Fig. 18. Outputs at load is 400[w].

4. Conclusions

In this paper, a new structure of a converter producing multi-level output voltage is made from conventional buck converters in series to reduce the output voltage of the DC/DC converter. The proposed multilevel DC/DC converter can reduce the ripple of the current because of the decrease of voltage added to the inductance. Therefore, the output voltage ripple can be reduced at the same time. Furthermore, the size and weight of inductance and capacitance will also be reduced using this new structure. Consequently, this proposed DC/DC converter is more credible. Besides, the proposed converter structure is fit for wide-range output voltage applications.

Current ripple will be reduced accordingly for little voltage change of the output filter, which results in the reduction of the output voltage ripple at the same time. Therefore, when we design power conversion systems, both the size and weight of inductors and capacitors will be reduced if the proposed multilevel DC/DC converter is used. Thus, the reliability of the designed DC/DC converter will be improved.

Element stress will be reduced when high output voltage is shared by each power element. Therefore, it is possible to use lower rated voltage switching elements in the power conversion system.

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