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Minimization of Voltage Stress across Switching Devices in the Z-Source Inverter by Capacitor Voltage Control

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ABSTRACT

The Z-source inverter (ZSI) provides unique features such as the ability to boost dc voltage with a single stage simple structure. Although the dc capacitor voltage can be boosted by a shoot-through state, the voltage stress across the switching devices is rapidly increased, so high switching device power is required at the ZSI. In this paper, algorithms for minimizing the voltage stress are suggested. The possible operating region for obtaining a desired ac output voltage according to both the shoot-through time and active state time is investigated. The reference capacitor voltages are derived for minimizing the voltage stress at any desired ac output voltage by considering the dc input voltage. The proposed methods are carried out through the simulation studies and experiments with 32-bit DSP.

Keywords: DC boost control, Modified SVPWM, Voltage stress, Z-source inverter

1. Introduction

In a traditional PWM inverter, the ac output voltage is limited by the dc input voltage, so an additional dc-dc boost converter is required to obtain the desired ac output voltage. The dead time to block both the upper and lower devices of the same phase leg has to be provided to prevent a short circuit. In order to overcome this limitation of a traditional inverter, a Z-source inverter (ZSI) which uses a Z-network to replace the traditional dc link was introduced [1]. A ZSI has a unique feature that allows it to boost the dc voltage by using the shoot-through operating mode, which is forbidden in a traditional PWM inverter. A ZSI provides a simple single stage approach for applications of any dc sources such as a photovoltaic (PV) array or a fuel cell stack [2]. Also, it improves the reliability of the inverter because a short circuit across any of the phase legs is allowed. The ZSI can be applied to a grid-connected PV system and adjustable speed drive [3],[4].

Three different inverters: a conventional PWM inverter, dc-dc boosted PWM inverter, and ZSI were compared for fuel-cell vehicle applications using total switching device power (SDP), passive components requirement, and efficiency [5],[6]. As the dc capacitor voltage is boosted by

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increasing the shoot-through time at the ZSI system, the voltage stress across the switching device is rapidly increased. The high voltage stress across the devices should be restricted to the obtainable ac output voltage gain because of the limitation of the device voltage rating. Thus, if the same boost ratios are used for three different inverters, the ZSI requires low SDP in the low boost ratio region, and at high boost ratio, the higher SDP is required due to increasing the voltage stress across the switching devices. A third harmonic injection method at the carrier-based PWM is proposed for decreasing the voltage stress of the devices by producing a maximum dc voltage under a given modulation index [7]. The paper [8] presented dc and ac analyses on ZSI control to study its transient behavior, using both small-signal analysis and the signal-flow-graph method.

In this paper, a method is proposed to control a desired ac output voltage while minimizing the voltage stress of the switching devices by adjusting the capacitor voltage in order to reduce the SDP. The operating boundary for ac voltage gains according to the modulation indexes is investigated. The dc capacitor voltage for minimizing the voltage stress at any desired ac voltage gain is derived. A modified space vector PWM (MSVPWM) is suggested to effectively control the shoot- through time. The simulation studies and experimental results with a 32-bit DSP are carried out.

2. Operation of Z-Source Inverter

Fig. 1 shows the general Z-source converter structure, which consists of inductors L_1, L_2 and capacitors C_1, C_2 connected in an X shape coupling the inverter to the dc voltage source.

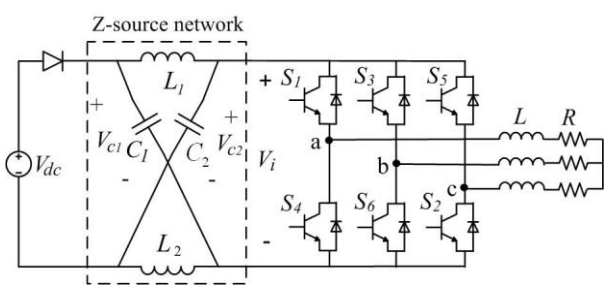

Fig. 1. General configuration of ZSI.

A Z-source converter can produce a desired ac voltage regardless of the dc source voltage. The general inverter has six active voltage vectors and one zero voltage vector. However, the three-phase ZSI has one extra zero voltage vector when the load terminals are shorted through both the upper and lower switching devices of any of the phase legs.

The ZSI has three operation modes: normal mode, zero-state mode, and shoot-through mode. In normal mode and zero-state mode, the ZSI operates under the traditional PWM. In the shoot-through mode, the load terminals are shorted at both the upper and lower switching devices of any of the phase legs. The dc capacitor voltage can be boosted as [1],

$$V_C = \frac{T_s - T_{sh}}{T_s - 2T_{sh}} V_{dc} = \frac{1 - M_{sh}}{1 - 2M_{sh}} V_{dc}. \quad (1)$$

where T_s, T_{sh} are the sampling period and the shoot-through time respectively, and $M_{sh} = T_{sh}/T_s$ is defined as the modulation index for T_{sh}.

The stress voltage of the switching device is expressed in terms of M_{sh}.

$$\hat{V}_i = \frac{1}{T_s - 2T_{sh}} V_{dc} = \frac{1}{1 - 2M_{sh}} V_{dc} \quad (2)$$

The ratios of both the voltage stress to dc input voltage and the capacitor voltage to dc input voltage versus M_{sh} are plotted in Fig. 2.

As M_{sh} increases from 0 to 0.5, the dc capacitor voltage is boosted, and the voltage stress across the switching devices is greater than the capacitor voltage. It can be seen that the capacitor voltage can be boosted more times than

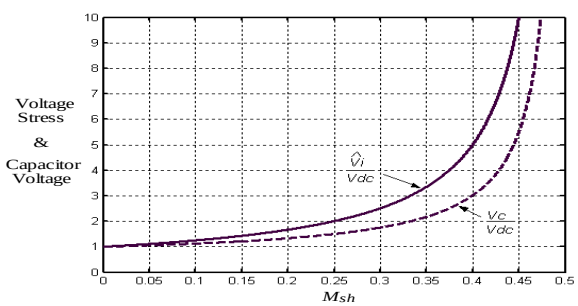

Fig. 2. Capacitor voltage and stress voltage versus M_{sh}.

the dc input voltage by controlling the shoot-through time without an additional dc boost converter. This is a unique feature of the ZSI. However, the voltage stress is quite high, which should restrict the obtained ac voltage gain because of the limitation of the device voltage rating.

3. Modified Space Vector PWM

Space vector PWM techniques have been widely used in current regulated PWM inverters due to lower current harmonics and a higher modulation index [9],[10]. A SVPWM is suitable to control the shoot-through time at the ZSI. The eight space vectors $\overline{V}_0 \sim \overline{V}_7$ are used in the SVPWM, where $\overline{V}_1 \sim \overline{V}_6$ are active vectors, and $\overline{V}_0$, $\overline{V}_7$ are zero vectors. If the reference voltage vector V_{ref} is located at sector I, the reference voltage vector is divided into the two adjacent voltage vectors V_1 and V_2.

In one sampling interval, V_1 and V_2 are applied at the time T_1 and T_2, respectively, and the zero vector is applied at time $T_0 = T_s - (T_1 + T_2)$. The reference voltage vector V_{ref} can be obtained as

$$V_{ref} = V_1 T_1 + V_2 T_2 \tag{3}$$

$$T_1 = \sqrt{3}\frac{V_{ref}}{\hat{V}_i} T_s \sin(\frac{\pi}{3} - \alpha) \ , \ T_2 = \sqrt{3}\frac{V_{ref}}{\hat{V}_i} T_s \sin\alpha \tag{4}$$

, where α is the angle between the reference voltage vector V_{ref} and voltage vector V_1.

The symmetrical pulse pattern of voltage vectors V_1, V_2 and zero vector for one sampling period of a traditional SVPWM is illustrated in Fig. 3(a). Unlike the traditional SVPWM, the MSVPWM has an additional shoot-through time besides time intervals T_1, T_2, T_0. Fig. 3(b) shows the switching pattern for a conventional MVSPWM. The zero voltage period T_0 should be diminished for generating a shoot-through time T_{sh}, while the active state times T_1, T_2 are unchanged. The shoot-through time is evenly assigned to each phase with (T_{sh}/6) which is defined as T. At this switching pattern, the zero state period is reduced from (T_0/4) to (T_0/4 - 2T) and (T_0/4 - T). As both zero state periods should be greater than 0, the shoot-through time is less than (3/4)T_0 at period (T_0/4 - 2T), and less than (4/3)T_0 at period (T_0/4 - T). As the shoot-through time is limited to (3/4)T_0, the dc voltage is not able to be boosted to maximum.

Fig. 4 shows the switching pattern for a traditional SVPWM and a novel MSVPWM at sector I, where the shoot-through time is distributed into (T_{sh}/4), (T_{sh}/6), and (T_{sh}/12) during the half sampling period. As shown in Fig. 4(b), two reduced zero state periods are the same as (T_0/4 – T_{sh}/4). As the shoot-through time can be extended to the zero state time T_0, the maximum dc capacitor voltage can be obtained. During the shoot-through period, both switches of the phase leg are conducted simultaneously for boosting the dc capacitor voltage. The six PWM pulses in the MSVPWM should be controlled independently.

4. Algorithms for Minimizing Voltage Stress

From Fig. 4(b), one sampling period consists of the active state time T_a and shoot-through time T_{sh}, and reduced zero state time T_0' at MSVPWM for ZSI as $T_s = (T_1+T_2)+T_0'+T_{sh} = T_a+T_0'+T_{sh}$, where $T_0' = T_0 - T_{sh}$.

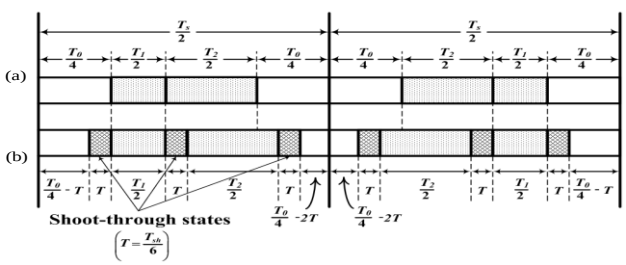

Fig. 3. Switching pattern for both traditional SVPWM and MSVPWM at sector I: (a) Traditional SVPWM, (b) Modified SVPWM.

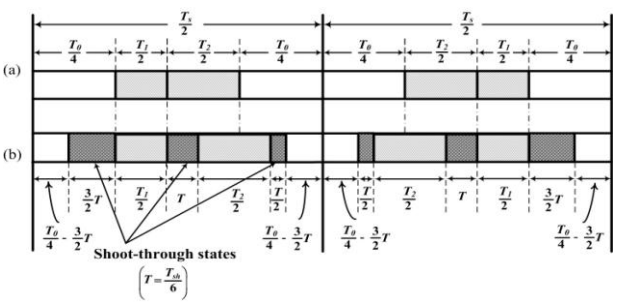

Fig. 4. Switching pattern for both traditional SVPWM and a novel MSVPWM at sector I: (a) Traditional SVPWM, (b) Novel MSVPWM.

From (4), the active state time T_a can be derived as follows.

$$T_a = T_1 + T_2 = \sqrt{3}\frac{V_{ref}}{\hat{V}_i} T_s \sin(\alpha + \frac{\pi}{3}) \tag{5}$$

The time T_a varies with each cycle and repeats periodically every π/3.

In order to derive an ac voltage gain which is the ratio of the output voltage versus the dc input voltage, the average active state time is derived as

$$\begin{aligned}(T_a)_{avg} &= \frac{1}{(\frac{\pi}{3})}\int_0^{\frac{\pi}{3}} \sqrt{3}\frac{V_{ref}}{\hat{V}_i} T_s \sin(\alpha + \frac{\pi}{3}) d\alpha \\ &= \frac{3\sqrt{3}}{\pi} T_s \frac{V_{ref}}{\hat{V}_i}\end{aligned} \tag{6}$$

Substituting (2) into (6), the average T_a can be expressed as M_{sh}.

$$(T_a)_{avg} = \frac{3\sqrt{3}}{\pi} T_s (1 - 2M_{sh}) \frac{V_{ref}}{V_{dc}} \tag{7}$$

As the magnitude of the reference voltage V_{ref} is equal to the peak of the output phase voltage, the ac voltage gain G_{ac} can be calculated from both the modulation index M_a and M_{sh}.

$$G_{ac} = \frac{V_{ac}}{V_{dc}} = \frac{\pi}{3\sqrt{2}} \frac{M_a}{1 - 2M_{sh}} \tag{8}$$

, where $M_a = \frac{(T_a)_{avg}}{T_s}$ is the modulation index of active state time and V_{ac} is the rms output line voltage.

The boundary of two modulation indexes M_a, M_{sh} for any ac voltage gain is plotted. When the zero state time T_0 is adjusted to 0, the active state time T_a has a maximum value, and so M_{sh} becomes the minimum value as

$$M_{a(\max)} = 1 - M_{sh(\min)}. \tag{9}$$

Substituting M_a in (9) into (8), the minimum M_{sh} can be expressed as the ac voltage gain.

$$M_{sh(\min)} = \frac{\frac{3\sqrt{2}}{\pi} \times G_{ac} - 1}{\frac{6\sqrt{2}}{\pi} \times G_{ac} - 1} \tag{10}$$

As M_{sh} is increased, the voltage stress across the device rapidly increases. The maximum M_{sh} is determined on the allowable voltage stress across the switching devices. If the voltage stress is limited to five times the dc input voltage, the maximum M_{sh} becomes 0.4 as shown in Fig. 2.

Fig. 5 shows the boundary of two modulation indexes for a given ac voltage gain, when the maximum M_{sh} is 0.4. The shadow area is the possible operation region under the dc boost and ac voltage control, and the operation region can be enlarged by increasing the maximum M_{sh}. However, the voltage stress restricts the obtainable ac voltage gain because of the limitation of the device voltage rating. In order to minimize the voltage stress of the device for a given ac voltage gain, the capacitor voltage is adjusted near the minimum boundary line of M_{sh} within the operation region because the capacitor voltage as well as the voltage stress are a function of M_{sh}.

The reference capacitor voltage versus the desired ac output voltage is plotted in Fig. 6, where the reference capacitor voltage is calculated by adding 10% margin to the capacitor voltage at the minimum boundary line of M_{sh} at Fig. 5.

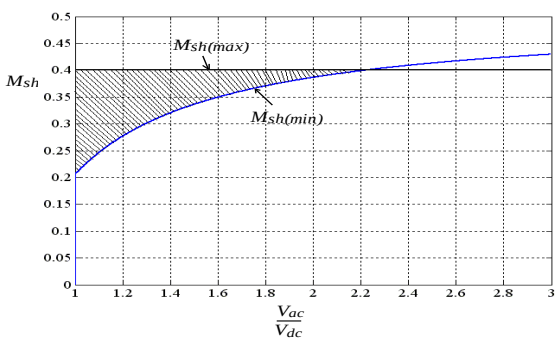

Fig. 5. Operation region for M_{sh}.

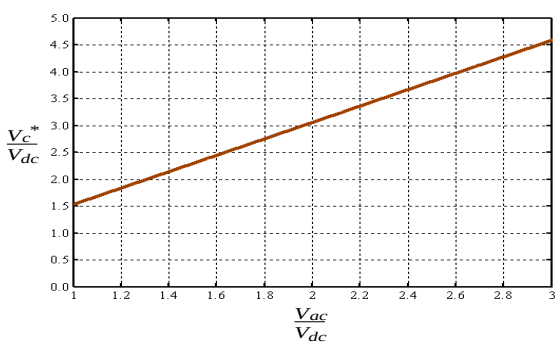

Fig. 6. Reference capacitor voltage versus ac voltage gain.

The ac voltage gain with variations of both the M_a and M_{sh} is plotted in Fig. 7. Many combinations of two modulation indexes are available for obtaining a desired ac voltage. If the M_a is decreased while ac voltage gain is kept constant, M_{sh} should be increased to boost the dc capacitor voltage. Also, the voltage stress is increased as shown in Fig. 2.

Fig. 8 shows the block diagram for controlling the ZSI. If the ac output voltage is assigned as a feedback signal at the output voltage PI controller, the phase delay between the reference ac output voltage and actual ac output voltage is generated due to the integral component in the PI controller. Therefore, the peak ac output voltage which is a dc value is used to control the ac output voltage. After detecting the 3-phase line voltages, the 3-phase voltages are transformed into 2-axis voltages in the stationary reference frame, and then the peak output voltage V_{sp} can be calculated from the 2-axis voltages. The output of the ac output voltage PI controller becomes the reference voltage for the MSVPWM. The reference capacitor voltage for minimizing the voltage stress at both the desired ac output voltage and input dc voltage is obtained from Fig. 6. The output of the capacitor voltage PI controller becomes the shoot-through time.

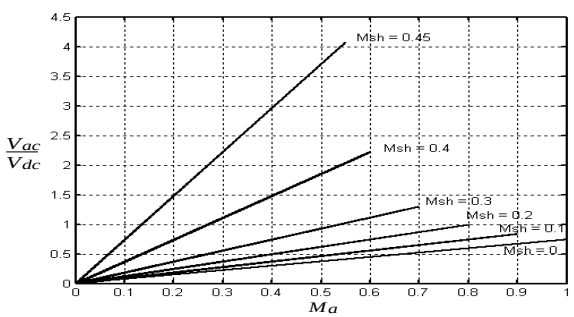

Fig. 7. Voltage gain according to both M_a and M_{sh}.

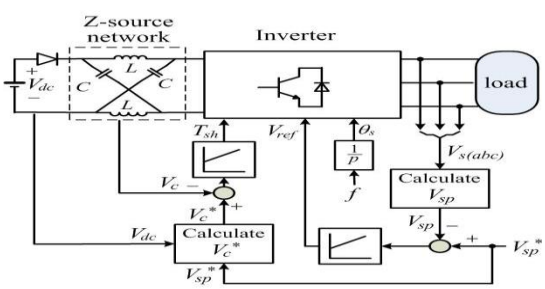

Fig. 8. Block diagram for ZSI control.

5. Simulation and Experimental Results

5.1 Simulation studies

Some simulation studies are carried out in order to verify the algorithms for ac output voltage control while minimizing the voltage stress across devices. The circuit parameters of ZSI are $L_1 = L_2 = 3$mH, $C_1 = C_2 = 1$mF, and the 3-phase RL circuit is used as the load of the ZSI. The sampling period of MSVPWM is 200μsec, and so the switching frequency of the PWM becomes 5Khz.

Fig. 9 shows the simulation results at $V_{DC} = 60$V, $V_{sp}^* = 85$V, where the ac voltage gain G_{ac} is 1. When the capacitor voltage is set to 180V, the voltage stress becomes 300V which is five times the dc input voltage. From Fig. 6, the ratio of the reference capacitor voltage to the dc input voltage at $G_{ac} = 1$ is about 1.5. Thus, the reference capacitor voltage for minimizing the voltage stress is determined to be 90V. As the capacitor voltage is decreased to 90V by adjusting the T_{sh} from 80μsec to 50μsec, the voltage stress can be suppressed to about 120V. The active state time is increased from 53μsec to 135μsec in order to keep the ac output voltage to its desired voltage while reducing the dc capacitor voltage.

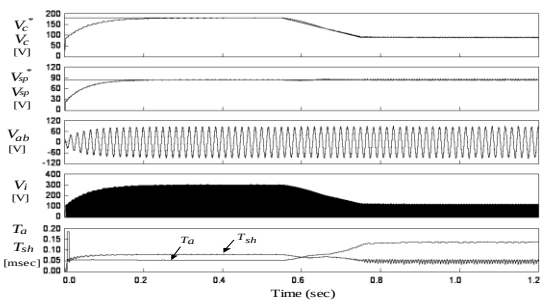

Fig. 9. Simulation result at $V_{sp}^* = 85$V.

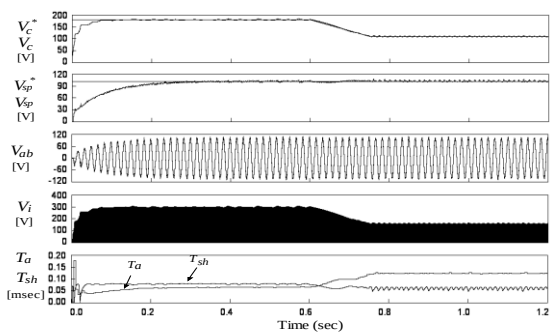

Fig. 10. Simulation result at $V_{sp}^* = 102$V.

Fig. 10 shows the simulation results at V_{DC} = 60V, V_{sp}^{*} = 102V, where the G_{ac} is 1.2. The reference capacitor voltage at G_{ac} = 1.2 becomes 110V, which is about 1.8 times the input dc voltage. When the capacitor voltage is adjusted from 180V to 110V, the voltage stress can be decreased by around 40%. As the capacitor voltage is reduced, both the active state time and shoot through time are changed to 62μsec and 120μsec, respectively.

5.2 Experiment results

The control system is implemented by a 32-bit DSP type TMS320F2812 operating with a clock frequency of 150Mhz and sampling interval of 200μs for the controlling ZSI system. Fig. 11 shows a photograph of the experiment equipment of the ZSI system, the power capacity of which is 3KVA.

Fig. 12 shows the PWM signals of the switching devices S1, S4, S3, S6 at T_a = 85μsec, T_{sh}=60usec. As shown in Fig. 4(b), the shoot-through periods at a-phase and b-phase legs are different: 15μsec and 10μsec, respectively.

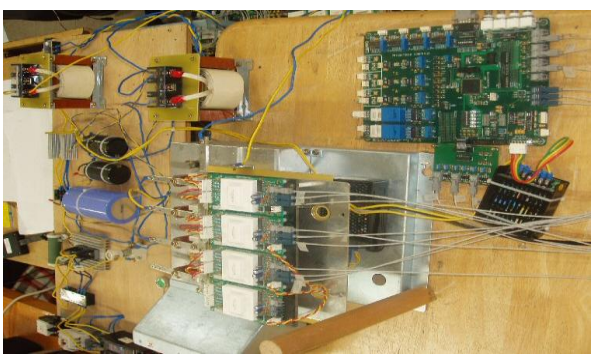

Fig. 11. Photograph of experiment equipment.

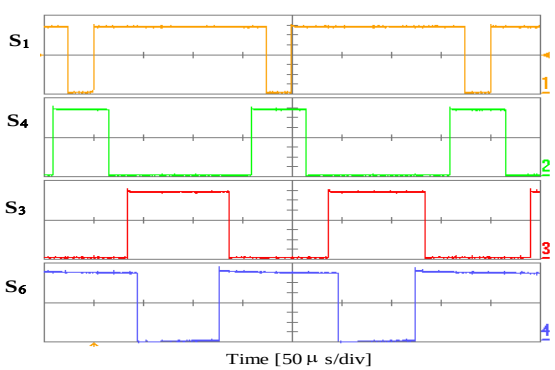

Fig. 12. Switching pulses of MSVPWM.

Figs. 13 and 14 show the experimental waveform of ac output voltage, dc capacitor voltage, voltage stress, and shoot-through time under the same operation conditions as in the simulations shown in Figs. 9 and 10, respectively. The experimental results are nearly identical with the simulation results, although the waveform of the voltage stress contains some noise.

6. Conclusion

Algorithms for minimizing the voltage stress by adjusting the dc capacitor voltage across the switching devices at the ZSI were proposed. As the shoot- through state time is extended to the zero state time by a modified SVPWM, the maximum dc voltage boost can be achieved. The possible operating region for an ac output voltage to dc input voltage is very dependent on the allowable voltage stress. The reference capacitor voltage for the minimization of the voltage stress at the ratio of the ac output voltage to dc input voltage was derived. The voltage stress across the switching device can be greatly reduced at any desired ac output voltage, and the reduction of voltage stress varies with the ac voltage gain. The total device power required at the ZSI can be decreased by the proposed algorithms.

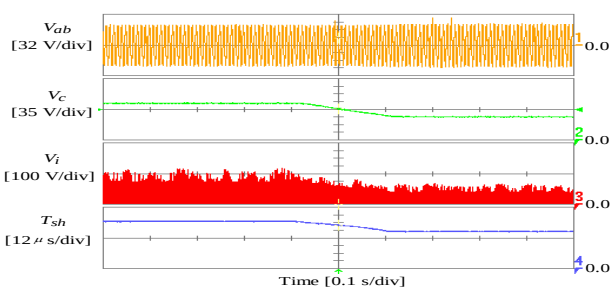

Fig. 13. Experimental result at V_{sp}^{*} = 85V.

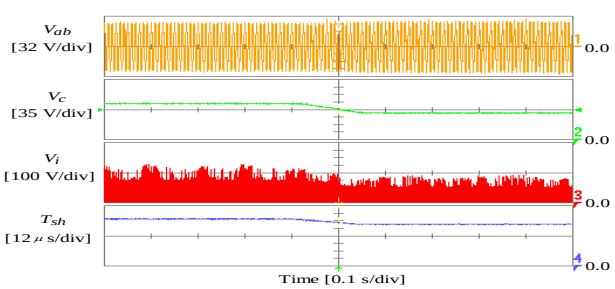

Fig. 14. Experimental result at V_{sp}^{*} = 102V.

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References

[1] F.Z.Peng, "Z-Source Inverter", *IEEE Trans. on Industry Applications*, Vol. 39, No.2, pp.504-510, March/April, 2003.

[2] J.S.Lim and S.K.Chung, "Implementation of a Fuel Cell Dynamic Simulator," *Journal of Power Electronics*, Vol.7, No.4, pp. 336-342, Oct., 2007.

[3] Y.Huang, M.Shen, F.Z.Peng, and J.Wang, "Z-Source Inverter for Residential Photovoltaic Systems," *IEEE Trans. Power Electronics*, Vol.21, No.6, pp.1776-1782, Nov., 2006.

[4] F.Z.Peng, X.Yuan, and Z.Qian, "Z-Source Inverter for Adjustable Speed Drives," *IEEE Power Electronics Letters*, Vol.1, No.2, pp.33-35, June, 2003.

[5] M.Shen, A.Joseph, J.Wang, F.Z.Peng, and D.J.Adams, "Comparison of Traditional Inverters and Z-Source Inverter for Fuel Cell Vehicles," *IEEE Trans. Power Electronics*, Vol.22, No.4, pp.1453-1463, July, 2007.

[6] T.Ahmed, S.Nagal, M.Nakaoka, and T.Tanaka, "Utility-Interactive Four-Switch Three-Phase Soft-Switching Inverters with Single Resonant DC-Link Snubber and Boost Chopper," *Journal of Power Electronics*, Vol.7, No.2, pp. 109-117, April, 2007.

[7] M.Shen, J.Wang, F.Z.Peng, L.M.Tolbert, and D.J.Adams, "Constant Boost Control of the Z-Source Inverter to Minimize Current Ripple and Voltage Stress," *IEEE Trans. on Industry Applications*, Vol. 42, No.3, pp.504-510, May/June, 2006.

[8] P.C.Loh, D.M.Vilathgamuwa, C.J.Gajanayake, Y.R.Lim, and C.W.Teo, "Transient Modeling and Analysis of Pulse-Width Modulated Z-Source Inverter," *in Conf. Rec. of IEEE- IAS Annual Meeting*, pp.2782-2789, 2005.

[9] Y.H.Liu, C.L. Chen, and R.J.Tu, "A Novel Space-Vector Current Regulation Scheme for a Field-Oriented- Controlled Induction Motor Drive," *IEEE Trans. Industrial Electronics*, Vol.45, No.5, pp. 730-737, Oct., 1998.

[10] K.Zhou and D.Wang, "Relationship Between Space-Vector Modulation and Three-Phase Carrier- Based PWM: A Comprehensive Analysis," *IEEE Trans. Industrial Electronics*, Vol.49, No.1, pp. 186-196, Feb., 2002.

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