A 0.18-μm CMOS UWB LNA Combined with High-Pass-Filter

Jeong-Yeon Kim · Chang-Wan Kim

Abstract

An Ultra-WideBand(UWB) Low-Noise Amplifier(LNA) is proposed and is implemented in a 0.18-μm CMOS technology. The proposed UWB LNA provides excellent wideband characteristics by combining a High-Pass Filter (HPF) with a conventional resistive-loaded LNA topology. In the proposed UWB LNA, the bell-shaped gain curve of the overall amplifier is much less dependent on the frequency response of the HPF embedded in the input stage. In addition, the adoption of fewer on-chip inductors in the input matching network permits a lower noise figure and a smaller chip area. Measurement results show a power gain of +10 dB and an input return loss of more than −9 dB over 2.7 to 6.2 GHz, a noise figure of 3.1 dB at 3.6 GHz and 7.8 dB at 6.2 GHz, an input P1dB of −12 dBm, and an IIP3 of −0.2 dBm, while dissipating only 4.6 mA from a 1.8-V supply.

Key words : CMOS, Low Noise Amplifier, RFIC, Ultra-Wideband, Wideband Amplifier.

Ⅰ. Introduction

In recent years, the Ultra-Wideband(UWB) communi-cations system has emerged as a leading technology due to its high data-rate. The UWB system can provide up to 2 Gbps by using a bandwidth from 3.1 to 10.6 GHz with a limited transmitted power level of −41.3 dBm/MHz[1]. However, the implementation of all of the hard-ware blocks in a UWB system is challenging because all of the circuit blocks require very wide band characte-ristics compared with those of previous narrow-band sys-tems. The Low-Noise Amplifier(LNA), the first gain block in the UWB receiver, is required to have wide-band input matching, a wide bandwidth, and a low noise figure from 3.1 to 10.6 GHz, while demonstrating low dc power consumption. A CMOS UWB LNA has recen-tly been reported that adopts a three-section passive Ba-nd-Pass Filter(BPF) in combination with the input stage of a narrow-band amplifier[2]. This topology shows ex-cellent wideband characteristics compared with other wideband topologies[3],[4]. However, the major drawback of this UWB LNA is the adoption of many on-chip inductors at the input stage, which tends to increase ch-p-area and degrade the Noise Figure(NF) due to parasitic resistances in the inductors. The bell-shaped gain curve of the LNA strongly depends on the frequency charac-teristics of the BPF in the input matching stage. The-refore, if the quality factor(Q) and the inductance value of each on-chip spiral inductor in the BPF unexpectedly change or deviate due to process variations, both the wideband input matching and the bandwidth of the LNA can be considerably degraded.

This paper proposes a wideband CMOS low-noise amplifier for UWB applications that combines a high-pass filter(HPF) with a conventional resistive-loaded LNA topology to achieve superior wideband input matching, a lower noise figure, and a wide bandwidth with lower dc power consumption.

Ⅱ. Proposed Receiver Architecture

Fig. 1 shows the proposed direct-conversion receiver architecture for the UWB systems, which supports the full UWB band from 3.1 to 10.6 GHz. In Fig. 1, in-coming UWB signals are amplified by the LNA and then down-converted to baseband signals by using a quadrature mixing process. Baseband signals are conti-nuously filtered and amplified through the following ba-seband circuitry(LPF and VGA).

To satisfy the NF of 6.6 dB in the UWB receiver[1], the NF of the UWB receiver from the LNA to the

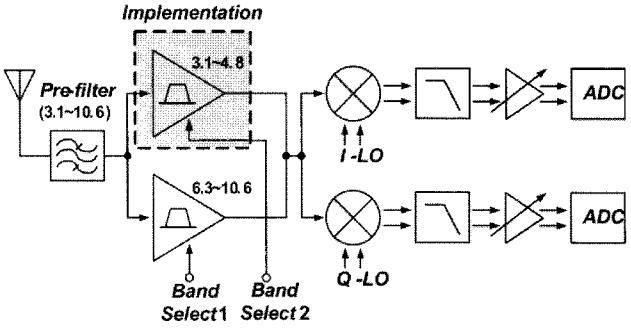

Fig. 1. Proposed RF front-end receiver.

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baseband circuits should be less than 4.6 dB because the overall loss from the external passive components(the BPF and the RF switch) is about 2 dB[5]. Previously reported full-band UWB LNAs inevitably consume more dc current for high transconductance(G_m) to achieve a sufficiently low NF from 3.1 to 10.6 GHz[6],[7]. In Fig. 1, the proposed architecture uses a parallel-connected LNA configuration instead of a full-band UWB LNA topology to cover the full-band UWB signals; one LNA processes UWB signals in the lower band(3.1 to 4.8 GHz) and the other processes UWB signals in the upper band(6.3 to 10.6 GHz).

Accordingly, each LNA in Fig. 1 can be more easily implemented for the lower and the upper UWB bands and the requirements of each LNA can be also considerably alleviated. In Fig. 1, each LNA is selectively enabled by using two-bit control signals. In Fig. 1, to cope with strong out-of-band interferers, especially in the 5-GHz WLAN frequency band, notch filters are embedded in the *I/Q* down-conversion mixer following the UWB LNA. In this paper, a CMOS UWB LNA for the lower band from 3.1 to 4.8 GHz is implemented and its design methodology is also discussed.

Ⅲ. Design of Wideband LNA

Fig. 2 shows the synthesis process of the frequency response(S_{11} and S_{21}) of a High-Pass Filter(HPF) and a Low-Pass Filer(LPF) in order to achieve the frequency response of a Band-Pass Filter(BPF) in the linear system. As can be seen in Fig. 2, the lower and upper −3 dB cut-off frequency ω_L and ω_H of the BPF can be independently decided or adjusted by the HPF and the LPF, respectively. In Fig. 2, the LPF can be replaced with a conventional resistively loaded amplifier, which inherently shows a low-pass frequency response due to parasitic capacitances at the output node. Accordingly, we can implement a wideband amplifier with band-pass frequency characteristics by combining a HPF and a resistively loaded amplifier. Fig. 3 shows the schematic of the proposed UWB CMOS LNA, which is composed of two different functional blocks; a passive HPF and a narrow-band amplifier with a resistive load. For the design of the wideband amplifier, first, the HPF in Fig. 2 is designed as a three-section Chebyshev filter with high attenuation, as shown in Fig. 3, but a T-type topology is adopted in this work to reduce the number of on-chip inductors[8]. The HPF in Fig. 3 is designed for a pass-band ripple of 0.1 dB, a −3 dB cutoff frequency of 2.5 GHz, and an attenuation of 10 dB at 1.6 GHz. In Fig. 3, component values in the HPF are given as C_1=C_2=1.2 pF and L_1=1.9 nH. Second, the LPF in Fig. 2 is designed as a resistively loaded amplifier in Fig. 3. The resistively loaded amplifier inherently provides low-pass filter characteristics due to parasitic capacitance at the output node. As shown in Fig. 3, the −3 dB bandwidth of the amplifier is enhanced by adopting the shunt-peaking inductor L_L[9]. Finally, the −3 dB upper cutoff frequency of the resistive-loaded amplifier is set at 10 GHz. Since the HPF described above is designed in a 50-ohm environment, the input impedance of the following amplifier also has to be 50 ohm. By using the proper combination of M_1, L_s, and L_g, the input impedance of the amplifier becomes 50 ohm near 6 GHz. An additional capacitor C_p in Fig. 3 helps to reduce the size of L_s and dc power dissipation[10]. The size of the components in the narrow-band amplifier are M_1=160 μm/0.18 μm, M_2=80 μm/0.18 μm, R_L=70 ohm, C_p=280 fF, L_L=1.6 nH, and L_g=2.3 nH. The L_S(about 0.6 nH) is implemented as a bonding-wire inductance in this work.

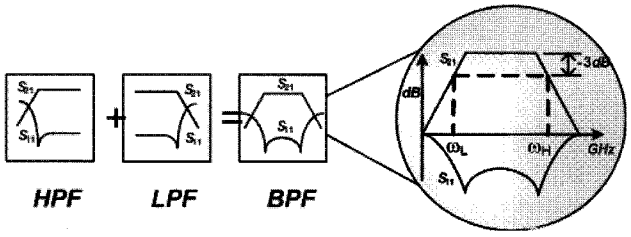


Fig. 2. Frequency response of BPF(=HPF+LPF).

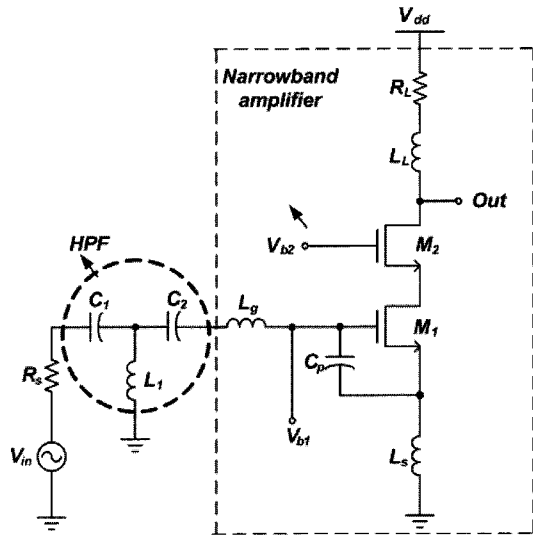
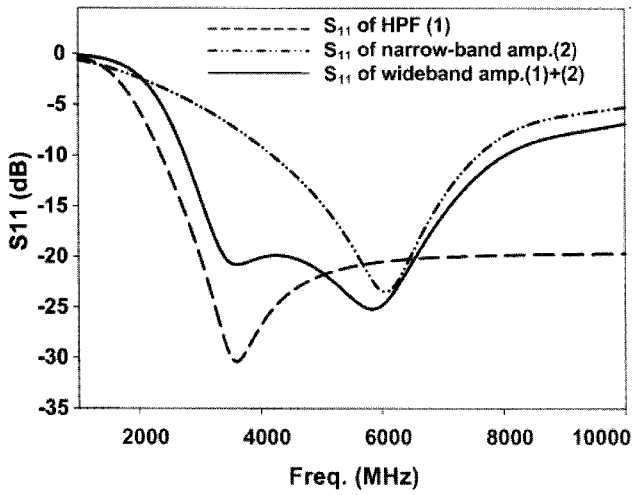
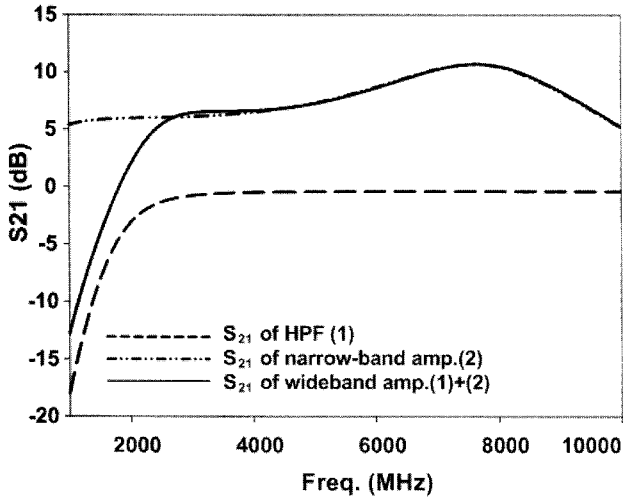


Fig. 3. Proposed wideband LNA which consists of a HPF and a narrow-band amplifier.

Fig. 4 shows the simulated S_{11} and S_{21} for the HPF, the resistive-loaded amplifier, and the overall wideband amplifier. As can be seen in Fig. 4, the frequency response(S_{11} and S_{21}) of the overall wideband amplifier is well synthesized with those of the HPF and the resistive-loaded amplifier. The simulated −3 dB bandwidth



(a) S_{11}



(b) S_{21}

Fig. 4. Simulated S-parameter results.

is about 2.5 to 8 GHz, and provides a sufficient margin for the lower UWB band.

Ⅳ. Measurement Results

The proposed UWB LNA is implemented in a 0.18-μm CMOS technology. Fig. 5 shows a microphotograph of the chip of the fabricated LNA, which has a die area of 1,000×800 μm, including the pads. The fabricated chip is mounted on a FR4 PCB and is tested by Chip-On-Board(COB). Fig. 6 shows the measured S_{11}, S_{21}, and NF of the proposed wideband LNA. In Fig. 6, all loss from the RF cable and the PCB are compensated and some fluctuations in s-parameter curves are expected due to some contact problems in the measuring procedure. The measured −3 dB bandwidth is about 2.7 to 6.2 GHz, which is reduced by 1.8 GHz compared with the simulation results. This is due to an unexpected parasitic capacitance at the output node of the LNA. As

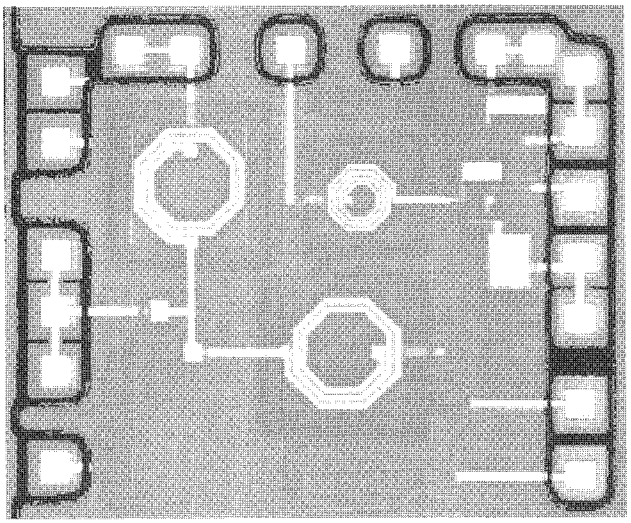


Fig. 5. Chip photograph.

shown in Fig. 6, from 2.7 to 6.2 GHz, S_{21} shows a clear bell-shaped curve and its average power gain is +10 dB. This bell-shaped gain curve can suppress unwanted out-of-band interferers(in 1,800/1,900 GSM, 2.4 ISM, and 5 GHz WLAN frequency bands) and improve receiver linearity. In Fig. 6, S_{11} also shows good wideband input matching, where two valleys at 3.8 and 5.4 GHz are caused by the HPF and the resistive-loaded amplifier, respectively. This measured S_{11} curve is well matched to the simulated results in Fig. 4, though it is slightly shifted to the lower frequency range. In Fig. 6, the minimum value of the NF of the fabricated CMOS LNA is 3.1 dB at 3.6 GHz, and rises to 7.8 dB at 6.2 GHz. However, for the operating frequency band(3.1 to 4.8 GHz) the measured NF is in the range of 3.1 to 4 dB. Fig. 7 shows the input 1-dB compression point of −12 dBm and an IIP3 of −0.2 dBm for two tones of 4.5 GHz and 4.55 GHz, respectively. In Table 1, the measured results are compared with previously reported

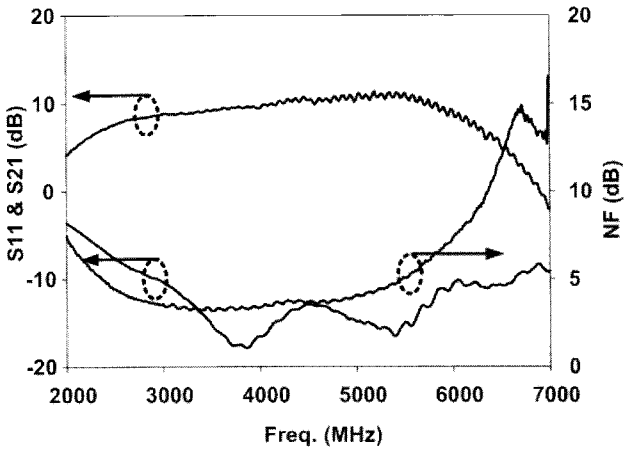


Fig. 6. Measured S_{11}, S_{21}, and NF.

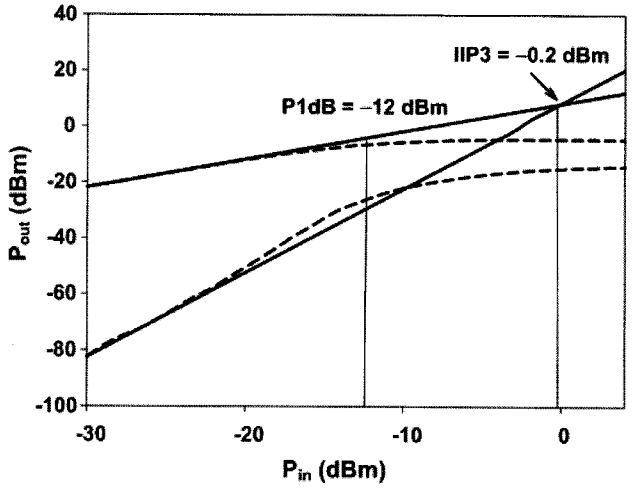


Fig. 7. Measured input-referred P1 dB and IIP3.

Table 1. Performance comparison.

	This work	[2]	[6]	[7]	[11]
CMOS(μm)	0.18	0.18	0.13	0.18	0.18
Gain(dB)	10	9.3	11	9.7	9.8
BW(GHz)	2.7~6.2	2.3~9.2	2~9.6	1.2~11.9	2~4.6
NF(dB)	3.1~7.8	4.2~8	3.6~4.8	4.5~5.1	2.3~5.2
S_{11}(dB)	<-9	<-9.4	<-8.3	<-11	<-10
IIP3(dBm)	-0.2	-6.7	-7.2	-6.2	-7
# of Inductor	4	5	0	5	3
Chip area	0.8	1.1	0.05	0.59	0.9
Power(mW)	8.3	9	19	20	9

CMOS UWB LNAs.

V. Conclusion

A wideband CMOS low-noise amplifier that combines a passive HPF with a conventional resistively loaded amplifier has been proposed. Fewer passive elements in the T-type HPF leads to a lower NF of the overall LNA and a smaller chip size. The proposed wideband LNA is implemented in a 0.18-μm CMOS technology and consumes 4.6 mA from a 1.8-V supply voltage. From the measurement results, the proposed wideband CMOS LNA can be employed in UWB applications.

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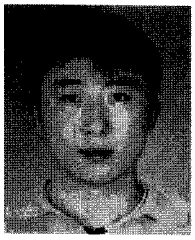

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