Temperature Dependent Characteristics Analysis of FLL Circuit

Jin-Ho Choi, *Member, KIMICS*

Abstract— In this paper, the temperature characteristics of full CMOS FLL(frequency locked loop) are analyzed. The FLL circuit is used to generate an output signal that tracks an input reference signal. The locking time of FLL is short compared to PLL(phase locked loop) circuit because the output signal of FLL is synchronized only in frequency. Also the FLL is designed to allow the circuit to be fully integrated. The FLL circuit is composed two FVCs, two buffers, a VCO and two frequency dividers. The temperature variation of frequency divider, FVC and buffer cancelled because the circuit structure is the same and the temperature effect is cancelled by the comparator. Simulation results are shown to illustrate the performance of the designed FLL circuit with temperature.

Index Terms— frequency locked loop, frequency-to-voltage converter, temperature stable characteristics, voltage controlled oscillator,.

I. INTRODUCTION

A PLL circuit is an important electronic block widely used in many integrated circuits. It is used in systems involving automatic control of frequency or phase, such as communication systems, frequency synthesis circuit and telemetry systems[1]. A PLL is a feedback loop comprised of a phase detector, low pass filter and VCO(voltage controlled oscillator)[2]. The output voltage of the phase detector is the phase difference between the input signal and the VCO output signal. The high frequency components are removed by the low pass filter. And then the output of the low pass filter is amplified and applied as the control voltage of the VCO. However the PLL can't be fully integrated because the low pass filter has to be implemented externally with discrete components.

A FLL is similar to a PLL in the way that it generates an output signal which tracks an input reference signal. But the FLL circuit has a simple structure compared to PLL which contains a FVC(frequency-to-voltage converter), VCO and an opamp(operational amplifier). The operation of FLL circuit is based on frequency comparison by the two FVC circuit blocks. It generates an output signal which tracks an input reference frequency. The designed FLL circuit is based on frequency comparison by the FVC which does not required the charge pump and the low pass filter[3,4]. Therefore the designed FLL can be integrated on the one chip. The architecture of FVC circuit is built on the charge redistribution principle based on switching capacitor[5].

This work describes temperature characteristics of the proposed FLL circuit. In Section II the output characteristics of FLL circuit are described. In Section III the simulation results of FVC, buffer and comparator will be shown with temperature. Finally, the conclusions show in Section IV.

II. FLL CIRCUIT IMPLEMENTETION

Fig. 1 shows the block diagram of the FLL circuit. The FLL circuit is composed of two FVCs, two buffers, a VCO, and two frequency dividers. First, the frequency of the input signal is divided by 2^{n1} and converted to a voltage by the FVC1[3]. The converted voltage, V_{O_FVC1}, is linearly dependent on the frequency of the input signal. The output of the VCO is divided by 2^{n2} in the same way. And the frequency information is converted to the voltage signal, V_{O_FVC2}, by the FVC2. The buffer is used for driving which is implemented an opamp. The voltage difference between V_{M1} and V_{M2} is then amplified by the opamp and the output voltage of the opamp, V_{IN_VCO}, is employed to control the output frequency of the VCO. The voltage V_{M2} will increase or decrease until the frequency of V_{O_FVC2} becomes equal to the frequency V_{REF}.

Manuscript received November 30, 2008; revised February 8, 2009.

Jin-Ho Choi is with the Department of Embedded IT, Pusan University of Foreign Studies, Busan, 608-738, Korea (Tel: +82-51-640-3194, Fax: +82-51-640-3038, Email: jhchoi@pufs.ac.kr)

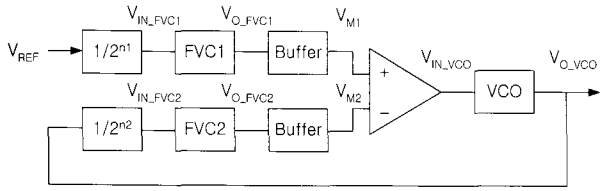

Fig. 1 Block diagram of the FLL circuit

The performance of the designed FLL circuit is shown in Fig. 2 at the room temperature[3]. From simulation results, the time required for the FLL to adjust the output frequency to a change in the input frequency from about 40MHz to 60MHz is about 10 input pulses. Fig. 2 shows the ratio output frequency and input frequency when the input frequency is varied from 40MHz to 60MHz. From the simulation results when the input frequency is varied in range from 41.7MHz to 58MHz the error can be neglected.

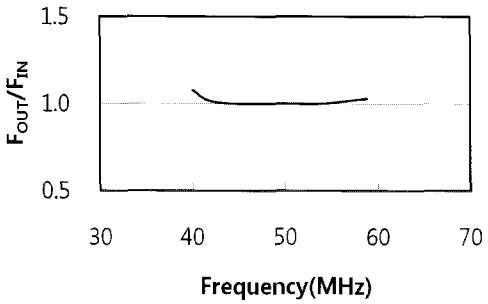

Fig. 2 F_{OUT}/F_{IN} with input frequency

III. TEMPERATURE CHARACTERISTICS OF FLL CIRCUIT

Fig. 3 shows the output frequency of the designed FLL circuit with temperature. The output frequency decreases with increase of temperature. Because the electrical characteristics of CMOS are degrade with increase of temperature such as threshold voltage and saturation drain current. Fig. 4 shows the error of the output frequency with temperature and the error is calculated as follows:

$$Error = \frac{Freq.(temp.) - Freq.(25^{\circ}C)}{Freq.(25^{\circ}C)} \times 100(\%) \quad (1)$$

When the temperature is varied from 5°C to 65°C, the variation of output frequency is about from 5.7% to -7.7%. Fig. 5(a) shows V_{O_FVC1} and V_{O_FVC2}, the output voltages of FVC, with temperature and Fig. 5(b) shows the variation rate of V_{O_FVC1} and V_{O_FVC2} with temperature. The variation rate is calculated as follows:

$$V_{O\_FVC} = \frac{V_{O\_FVC}(temp.) - V_{O\_FVC}(25^{\circ}C)}{V_{O\_FVC}(25^{\circ}C)} \times 100(\%) \quad (2)$$

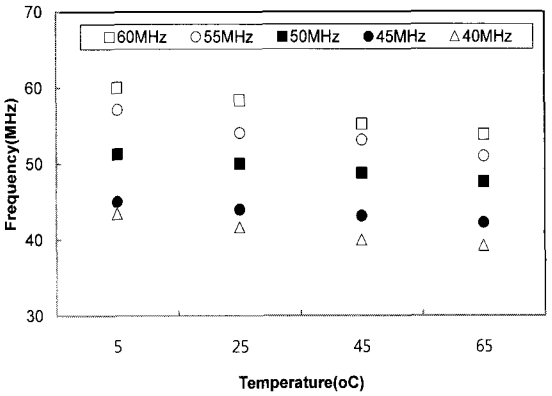

Fig. 3 Output frequency with temperature

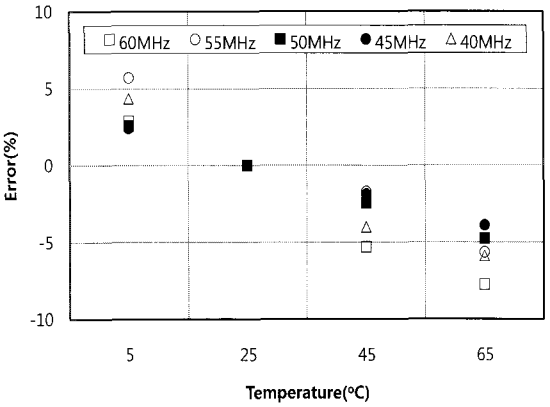

Fig. 4 Error of output frequency with temperature

When the temperature is varied from 5°C to 65°C, the variation rate of V_{O_FVC1} is about from 1.86% to -2.26%. And the variation rate of V_{O_FVC2} is about from 1.36% to -2.78%.

Fig. 6(a) shows the variations of V_{M1} and V_{M2}, the output voltages of buffer, with the temperature and Fig. 6(b) shows the variation rate range from 5°C to 65°C.

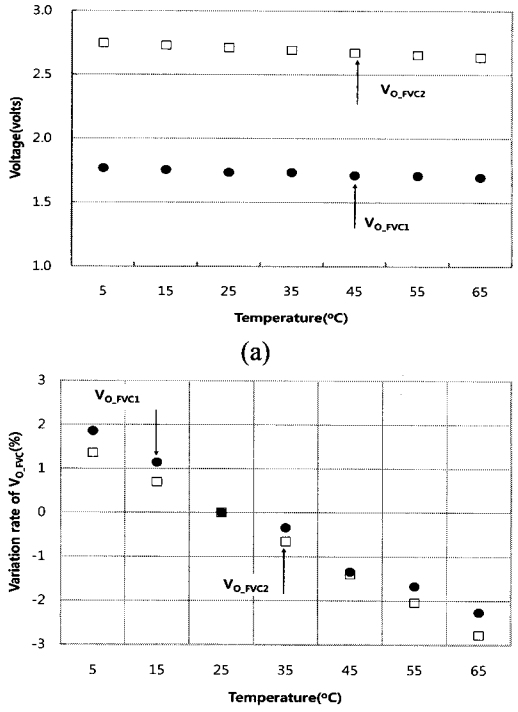

Fig. 5 Output voltages of FVC1 and FVC2 with temperature (a) output voltage (b) variation rate of output voltage

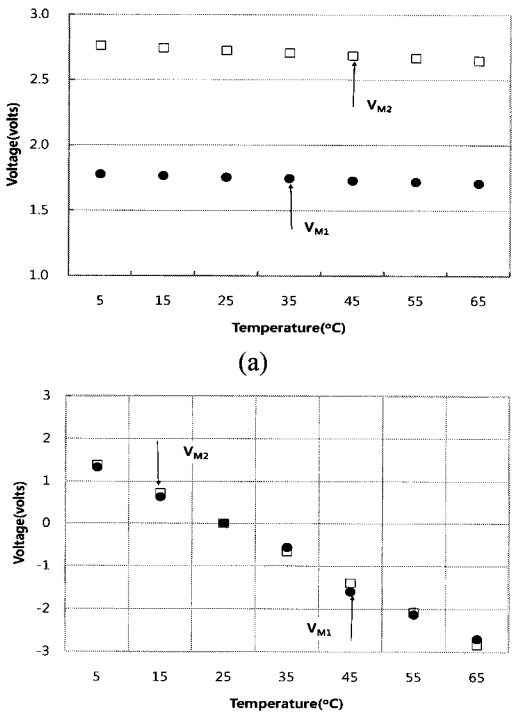

Fig. 6 Output voltages of buffer1 and buffer2 with temperature (a) output voltage (b) variation rate of output voltage

The variation rate is calculated as follows:

$$V_M = \frac{V_M(temp.) - V_M(25^\circ C)}{V_M(25^\circ C)} \times 100(\%) \quad (3)$$

When the temperature is from 5°C to 65°C, the variation rate of V_{M1} is about from 1.38% to -2.83%. And the variation rate of V_{M2} is about from 1.32% to -2.69%.

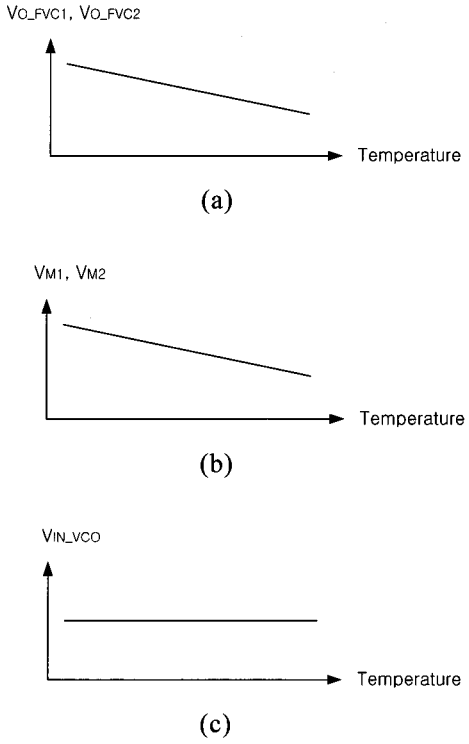

Fig.7 Output characteristics of FVC, buffer and comparator with temperature (a)FVC (b) buffer (c) comparator

Fig. 8 shows the calculation results from eq. (4), eq. (5) and eq. (6). The variation rate of comparator, F2-F1, is nearly zero with temperature.

$$F1 = \frac{V_{M1}(temp.) - V_{M1}(25^\circ C)}{V_{M1}(25^\circ C)} \times 100(\%) \quad (4)$$

$$F2 = \frac{V_{M2}(temp.) - V_{M2}(25^\circ C)}{V_{M2}(25^\circ C)} \times 100(\%) \quad (5)$$

$$F = F2 - F1 \quad (6)$$

From Fig. 8, V_{IN_VCO} is almost constant over the temperature range from 5°C to 65°C. Because the VCO circuit input voltage, V_{IN_VCO}, is obtained by subtracting V_{M1} from V_{M2}. From these results, to

obtain temperature stable characteristics of FLL circuit the VCO has the temperature stable characteristics. Because the output voltage change of FVC and buffer can be cancelled with temperature.

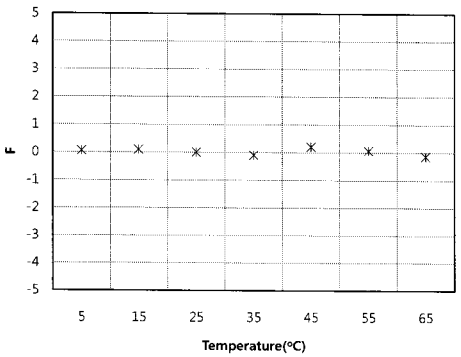

Fig.8 Variation rate of buffer output voltage difference with temperature

Fig. 9 shows the proposed VCO circuit[3]. The output frequency of the VCO is calculated as follows:

$$f_O = \frac{V_{IN\_VCO} / R5}{C1 \times (V_{REF1} - V_{REF2})} \propto \frac{1}{R5C1 \times \Delta V} \qquad (7)$$

V_{REF1} and V_{REF2} are the oscillation peak voltage of the VCO. If the multiplication of 1/R5, C1, the difference of V_{REF1} and V_{REF2} is constant in eq. (7) with temperature the temperature stable characteristic can be obtained.

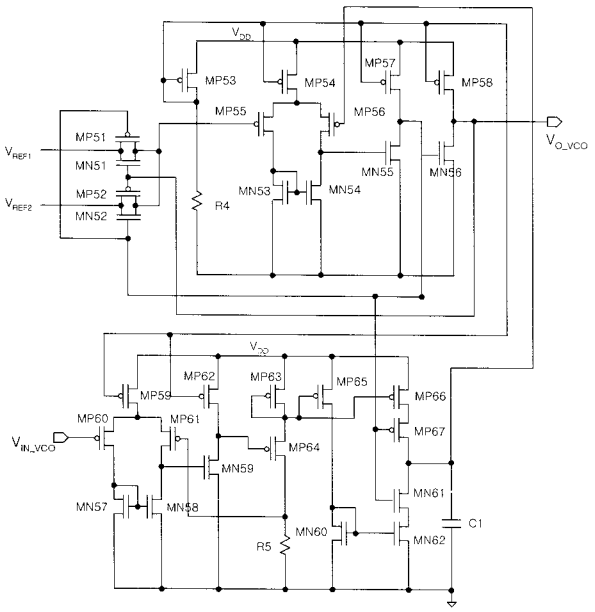

Fig. 9 VCO circuit

For obtaining constant $RC\Delta V$ with temperature the reference voltage difference, ΔV, have to be controlled[5].

IV. CONCLUSIONS

The temperature characteristics of the proposed FLL circuit are analyzed. The circuit was designed by 0.35μm CMOS process and simulation carried out with HSPICE. The temperature variation of FVC and buffer was cancelled because the circuit structure is the same. Also the temperature effect is cancelled by the comparator. Therefore the temperature stable FLL can be obtained if the VCO will be designed the temperature independent characteristics.

REFERENCES

[1] R. E. Best, *Phase-Locked Loops: Theory, Design and Applications,* New York:McGraw-Hill, 1984.

[2] Sidney Soclof, *Applications of analog integrated circuits*, Prentice-hall, 1985.

[3] Jin Ho Choi, "Design of Frequency Locked Loop Circuit," The Korea Institute of Maritime Information & Communication Sciences, pp.275-278, 2008.

[4] A. Djemouai, M. Sawan and M. Slamani, "New Circuit Techniques Based on a High Performance Frequency-to-Voltage Conversion," *Proceedings of IEEE Int. Conf. Electronics Circuits and Systems*, pp. 13-16, 1999.

[5] Jin-Ho Choi and Young-Jung Yu, "Temperature Stable Frequency-to-Voltage," *The Journals of The Korea Institute of Maritime Information & Communication*, vol. 11, no. 5, pp. 949-954, May 2007.

Jin-Ho Choi
(M'85–SM'87–F'92) received the B.S. degree in electronics from Busan University in 1985, and the M.S. degree in electronics from KAIST in 1987. He received the Ph. D. degree in electronics from KAIST in 1992. From 1992 to 1996, he was a researcher at Hynix Semiconductor Inc.. Since 1996, he has been a professor in Dept. of Computer Engineering, Pusan University of Foreign Studies. His research interest includes VLSI design.