

# Subthreshold Current Model of FinFET Using Three Dimensional Poisson's Equation

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**Abstract**— This paper has presented the subthreshold current model of FinFET using the potential variation in the doped channel based on the analytical solution of three dimensional Poisson's equation. The model has been verified by the comparison with the data from 3D numerical device simulator. The variation of subthreshold current with front and back gate bias has been studied. The variation of subthreshold swing and threshold voltage with front and back gate bias has been investigated.

**Index Terms**— FinFET(fin field effect transistor), subthreshold current, 3D Poisson's equation, subthreshold swing, threshold voltage

## I. INTRODUCTION

THE fin field effect transistor(FinFET) having three gates not only offers higher current drive per unit silicon area and better short channel immunity, but also it presents a method to scale down the transistor to 20nm gate length. Since the FinFET is formed by narrow silicon ridge that rises up from the wafer surface and rests on the insulating layer like silicon dioxide, the leakage is reduced. The control by gates in FinFETs is stronger than that in the conventional FETs since the gates of FinFET drapes across the fin, giving the FinFET multiple gates. The FinFET has three gates having the same workfunction. The three dimensional structure such as the FinFETs requires three dimensional analysis.

The threshold voltage of a transistor is one of the key parameters in design of devices, and Lim *et al.*[1] have modeled the threshold voltage  $V_T$  for long channel SOI MOSFETs using the solution of one dimensional Poisson's equation. As the device

dimensions are scaled down to nano regime to get better output characteristics, the one dimensional model becomes even more challenging. The rigorous solution of the two dimensional Poisson's equation has been used to model the short channel effects for SOI MOSFET and double gate MOSFET[2]. The solution of two dimensional Poisson's equation has been obtained from many methods. Pseudo two dimensional solution and a quasi two dimensional method have been presented in other papers[3,4]. The analytical solutions by means of power series[5] and Green's function technique[6] are another method to solve two dimensional Poisson's equation. Another famous approach to solve two dimensional Poisson's equation is to separate the two dimensional Poisson's equation into a one dimensional Poisson's equation and a two dimensional Laplace equation[7].

The device geometry of MOSFET has been developed to nano structure regime of short channel and narrow width. The short channel influences on higher speed and lower supply voltage, and narrow width on higher density and lower power consumption. The two dimensional solutions discussed above take into account the scaling of the channel length, but donot take into account narrow width effects. The three dimensional solution of Poisson's equation need including narrow width effects. Recently Havaladar *et al.*[8] have reported a model for  $V_T$  of mesa-isolated small geometry for fully depleted silicon-on-insulator(FD SOI) MOSFETs based on the solution of three dimensional Poisson's equation and it is extended to model the subthreshold current and  $V_T$  in FinFETs with doped and undoped channels. They also studied the dependences of  $V_T$  and subthreshold swing on channel doping concentration.

In this paper current model has been presented using analytical solution of the three dimensional Poisson's equation, and dependences of front and back gate bias on drain current are also studied.

The analytical potential model and current model based on solution of the three dimensional Poisson's equation are derived in Section II. The results from this model are compared with the solutions of numerical simulation and discussed in Section III. The conclusions are explained in Section IV.

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## II. THE ANALYTICAL MODEL OF POTENTIAL AND CURRENT FOR FINFET

Fig. 1 shows the cross-sectional view of a FinFET along the channel and width. Note that the FinFET is same as the mesa-isolated SOI MOSFETs in layout, and the gates drapes channel on the three sides in both cases. Therefore the same boundary conditions can be used to solve the Poisson's equation. Thus, the solution of the three dimensional Poisson's equation for SOI MOSFET[9] can be extended to FinFETs. Since the FinFET, however, has channel of fin shape, height and width of channel region have to choose appropriately. Using the same procedure as reference paper[9], the potential in channel of FinFET is the following ;

$$\begin{aligned} \psi(x, y, z) = & \psi_{sb} + E_{sb}(H_{fin} - x) + \frac{q}{2\epsilon_{Si}} N_A (H_{fin} - x)^2 \\ & + \sum_{r=1}^{\infty} \frac{1}{\sinh(\gamma_r L_{eff})} [V_r \sinh(\gamma_r y) + V_r \sinh(\gamma_r (L_{eff} - y))] \\ & \times [\sin(\gamma_r x) + \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{oxf} \gamma_r \cos(\gamma_r x)] \\ & + \sum_{s=1}^{\infty} \sum_{r=1}^{\infty} P_{sr} [\sinh\{\chi_{sr} (T_{fin} - z)\} + \sinh(\chi_{sr} z)] \\ & \times \frac{\sin(\alpha_s (y - L_{eff}))}{\cos(\alpha_s L_{eff})} [\sin(\beta_r x) + \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{oxf} \beta_r \cos(\beta_r x)] \end{aligned} \quad (1)$$

where  $N_A$  is the channel doping concentration,  $t_{oxf}$  is the oxide thickness of the top gate,  $L_{eff}$  is the effective channel length,  $T_{fin}$  and  $H_{fin}$  are thickness and height of the fin. The  $\epsilon_{Si}$  and  $\epsilon_{ox}$  are the dielectric constants of silicon and  $SiO_2$ . The definitions for the other parameters refer to the paper[9]. In this paper the first ten terms ( $1 \leq r \leq 10$ ) of the first series and the first term ( $s=1$ ) of second series is used to calculate the potential because it has been observed that other terms donot affect the results.

To calculate the subthreshold current  $I_{ds}$ , the channel is now divided into two parts as following ;

- 1)  $0 \leq x \leq x_{min}$
- 2)  $x_{min} \leq x \leq H_{fin}$

where the potential is the minimum at  $x_{min}$ . Thus, the subthreshold current is consisted of front current  $I_{ds}^f$  and back current  $I_{ds}^b$  as following;

$$I_{ds} = I_{ds}^f (0 \leq x \leq x_{min}) + I_{ds}^b (x_{min} \leq x \leq H_{fin}) \quad (2)$$

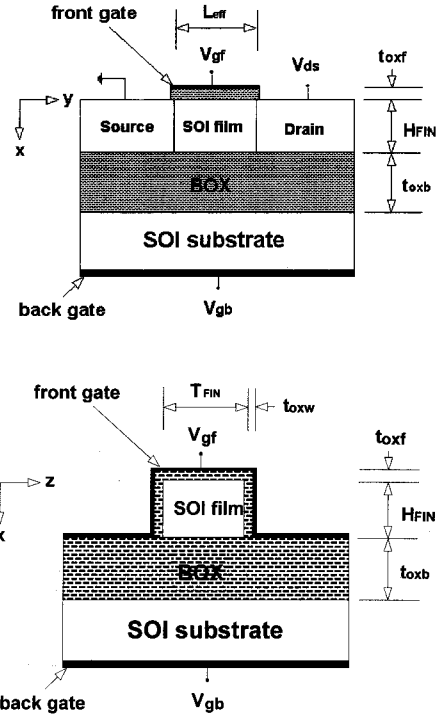


Fig. 1 Cross-sectional view of FinFET along the channel length(above) and along the channel width(bottom).

The potential variation is small along the height because of lesser control of the front gate and in the width direction because of the proximity of the two side gates that are at the same potential. Hence the error due to the variation of potential in the both directions is negligible. This leads to

$$I_{ds}^f = \frac{T_{fin} V_t^3 \mu_n n_i^2 x_{min}}{L_e N_A (\psi_s^f - \psi_{min}) (\psi_s^s - \psi_{min})} (e^{\frac{\psi_s^f}{V_t}} - e^{\frac{\psi_{min}}{V_t}}) \times (e^{\frac{\psi_s^s - \psi_{min}}{V_t}} - 1) (1 - e^{\frac{V_{ds}}{V_t}}) \quad (3)$$

$$I_{ds}^b = \frac{T_{fin} V_t^3 \mu_n n_i^2 (H_{fin} - x_{min})}{L_e N_A (\psi_s^b - \psi_{min}) (\psi_s^s - \psi_{min})} (e^{\frac{\psi_s^b}{V_t}} - e^{\frac{\psi_{min}}{V_t}}) \times (e^{\frac{\psi_s^s - \psi_{min}}{V_t}} - 1) (1 - e^{\frac{V_{ds}}{V_t}}) \quad (4)$$

where  $L_e$  takes into account lateral penetration of the depletion regions associated with the source and drain[5]. The notation for potentials is  $\psi_s^f = \psi(0, y_{min}^f, T_{fin}/2)$ ,  $\psi_s^b = \psi(H_{fin}, y_{min}^b, T_{fin}/2)$  and  $\psi_s^s = \psi(x_{min}, y_{min}^f, 0)$  where  $y_{min}^f$  is the lateral position of the minimum front surface potential and  $y_{min}^b$  is the lateral position of the minimum back

surface potential.

### III. RESULTS OF POTENTIAL AND CURRENT

Fig 2 shows the potentials obtained from Eq.(1) for the channel doped with  $N_A = 1.5 \times 10^{16} / \text{cm}^3$ . The results from this model are compared with those of the simulations using the three dimensional device simulator DAVINCI[10]. Note that results of this paper agree well with three dimensional results. The potential variation along the channel width is symmetrical at  $z = T_{fin} / 2$ .

To calculate subthreshold current, the diffusion current is only considered because the carrier concentration is low and the drift current is negligible in the subthreshold region. The relationship of subthreshold current versus front gate bias ( $V_{gf}$ ) is derived of this model as shown in Fig. 3. As shown in Fig. 3, the subthreshold current is consisted with mostly front current under condition of back gate bias  $V_{gb} = 0$ . As described above, front current is component in the region of  $0 \leq x \leq x_{min}$ , and back current is in  $x_{min} \leq x \leq H_{fin}$ .

When the back gate bias is zero,  $x_{min}$  is nearly  $H_{fin}$ . Thus, most current is front current. Note that a current increases with an increase in front gate voltage due to p-type channel.

We can know current level can be changed when the back gate is biased. Fig. 4 shows the variation of drain current according to back gate bias  $V_{gb}$ . As expected, the current is increasing when back gate bias

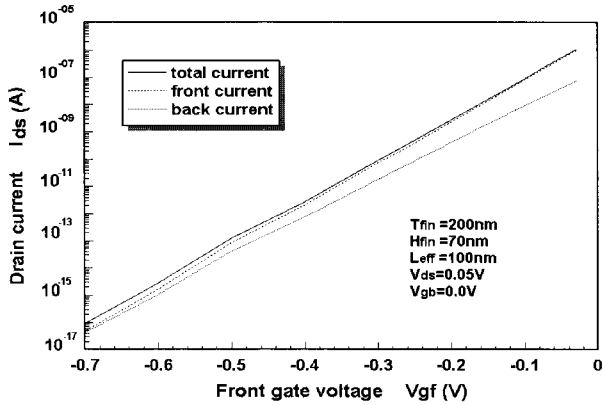


Fig. 3 The drain current according to front gate voltage. Note that most current is front current because of back gate bias  $V_{gb} = 0$ .

bias increases. Note increasing rate is constant.

The constant increasing rate means uniformity of subthreshold swing. Thus, subthreshold swing is not changed with back gate bias. The threshold voltage ( $V_{th}$ ) of FinFET can also be obtained from the subthreshold characteristics. Based on the definition of the threshold voltage of the FinFET as the value of  $V_{gf}$  for which the drain current is given by  $I_{ds} = 300nA \times W / L_{eff}$ , where  $w$  is the effective width of the FinFET given by  $W = 2H_{fin} + T_{fin}$  [8], the threshold voltage is decreasing but nearly constant when back gate bias increases as shown in Fig. 4. Fig. 5 shows current occupation ratio of front current and back current according to front gate bias under the same geometry as shown in Fig. 3. The results show an increase in the front current and an decrease in the back current with an increase in front gate bias.

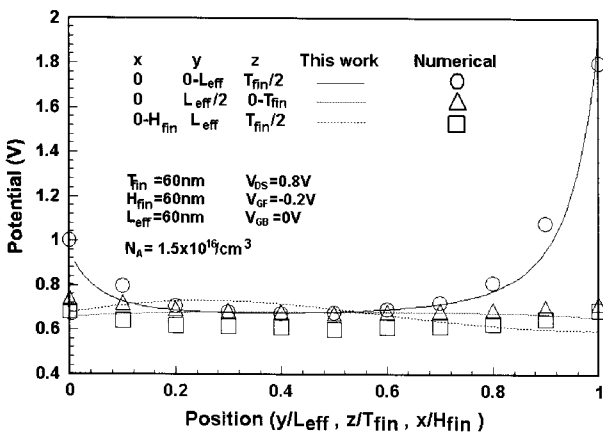


Fig. 2 The three dimensional potential variation in the channel of FinFET with doped fin.

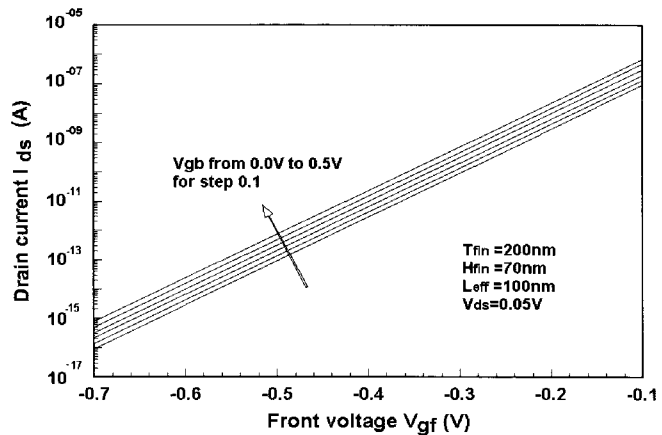


Fig. 4 The drain current according to variation of back gate bias. Note that increasing rate is constant.

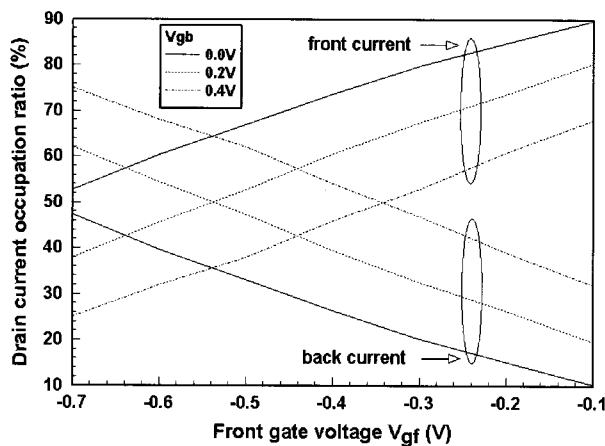


Fig. 5 The current occupation ratio of front current and back current according to front gate bias.

As expected in Fig. 3 and Fig. 5, the percentage of the front current is increasing with an increase in front gate bias since  $x_{\min}$  is going to  $H_{fin}$  with an increase in front gate bias. Alternatively the percentage of back current is increasing with an increase in back gate bias since  $x_{\min}$  is going to 0 with an increase in back gate bias  $V_{gb}$ . Note the portion of back current pass the one of front current in the lower front gate bias. The portion of back current is increasing with constant rate according to increasing of back gate bias. Note the increasing rate in front current with an increase in front gate bias is similar to the increasing rate in back current with an increase in back gate bias.

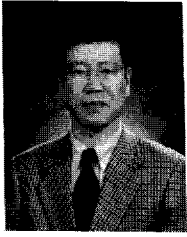
#### IV. CONCLUSIONS

Based on the analytical solution of three dimensional Poisson's equation with doped channel, the subthreshold current model of FinFET using the potential variation in the channel has been presented in this paper. The potential values of this model have been compared with the data from 3D numerical device simulator. This paper shows this model is valid since those agreed well with 3D data. The variation of subthreshold current, consisted of front current and back current, with a change in front gate and back gate bias has been studied. The portion of front and back current is changed with variation in front and back gate bias, and the variation rate is nearly constant. The subthreshold swing is not changed with back gate bias, and the threshold voltage is decreasing but nearly

constant when back gate bias increases. Henceforth, the variation of subthreshold characteristics will be studied with the geometry of device. This model will therefore be useful for the design of FinFETs and for circuit simulation purposes.

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