

Timing Analysis of Discontinuous RC Interconnect Lines

Taeheon Kim, Youngdoo Song, and Yungseon Eo

Abstract—In this paper, discontinuous interconnect lines are modeled as a cascaded line composed of many uniform interconnect lines. The system functions of respective uniform interconnect lines are determined, followed by its time domain response. Since the time domain response expression is a transcendental form, the waveform expression is reconfigured as an approximated linear expression. The proposed model has less than 2% error in the delay estimation.

Index Terms—Interconnect modeling, RC interconnects, transmission lines

I. INTRODUCTION

As the clock frequency of VLSI circuits dramatically increases over several GHz, interconnect lines play a pivotal role in the determination of circuit performance [1-4]. Thus, signal integrity of the interconnect lines has to be verified in the early stage of circuit design.

In practical integrated circuits, most of interconnect lines is neither simple uniform nor isolated straight lines but discontinuous lines. That is, the characteristic impedance of the line of the interest may be changed during the signal propagation from a source to a destination because of neighbor lines. Physically, while signal paths near circuit blocks may have narrow routing spaces, the other area may be more enough routing space. Consequently, a signal path may have different line width for suitable layouts. Alternatively, many of the signal lines may be complicatedly coupled with neighbor lines in parts. As an example, an

interconnect line from a circuit block to another circuit block may be coupled in a part as shown in Fig. 1. In such case, the signal transient of the line may be significantly affected by neighbor line switching. That means a part of the line may have different characteristics with the remaining part of the line. Thus, existing simple timing models that assume a uniform straight line may not be accurate enough as shown in Fig. 2. In reality, although such complicated line can be accurately evaluated with

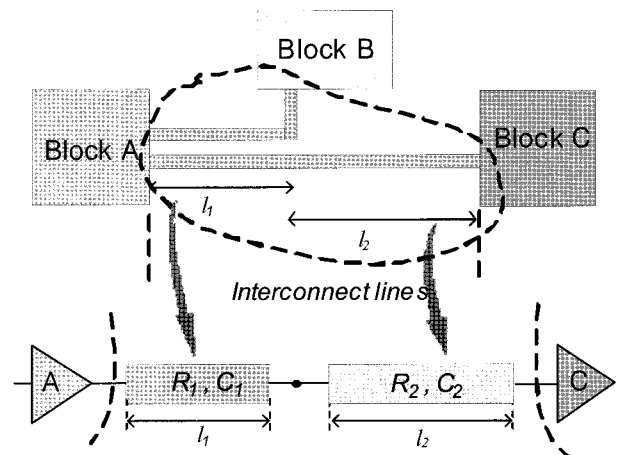


Fig. 1. Coupled interconnect lines in a part.

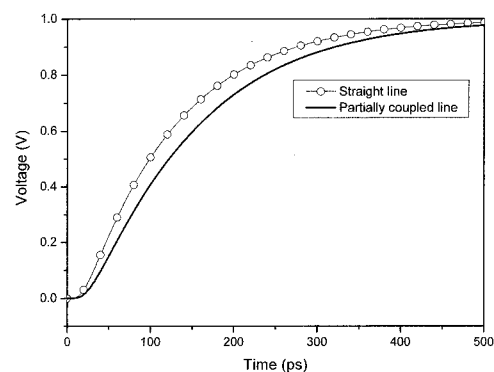


Fig. 2. Signal transient for the interconnect line between block A and block C of Fig. 1.

SPICE simulation, it may not be suitable for the timing verification of practical circuits which has myriad interconnect nets. Thus, a much simpler timing model for such lines is highly required to be incorporated into various circuit design CAD tools.

In order to readily determine the delay time of discontinuous lines, previously moment-matching technique [6-10] have been employed. Although they reduce computation time and guarantee accuracy, recursive moment calculations may significantly increase computation time since the number of RC segments is increased with technology scaling.

Bhavnagarwala *et al.* [11] derived a simple timing model for tree-structure-like discontinuous lines. However, the model is not accurate enough since they aggressively approximate the expression during the model derivation. Thus, it needs to be improved for more accurate timing verification of today's high-performance integrated circuits. Zhou *et al.* [12] proposed a two-pole transfer function for RLC networks using ABCD matrix of transmission line. Since the approximated transfer function may not be stable, a modified model [16] is used to ensure the stability. However, it results in inaccuracy problem.

In this paper, discontinuous interconnect lines are modeled as a cascaded line composed of many uniform interconnect lines. Then, exploiting the signal transient waveform expression of an intermediate node, a more general waveform expression for the discontinuous interconnect line is derived. It is shown that the model has excellent agreement with SPICE simulation in less than 2% error in the delay estimation.

II. TIME DOMAIN RESPONSE OF DISCONTINUOUS INTERCONNECT LINE

1. System Function of RC Interconnect Line

In [13], assuming an one dominant pole, a step input response for an RC interconnect line of Fig. 3 can be represented as

$$v_o(t) = 1 + K \exp(-t/\tau) \quad (1)$$

where

$$\begin{aligned} K &= -1.01(R_T + C_T + 1)/(R_T + C_T + \pi/4) \\ \tau &= RC(R_T C_T + R_T + C_T + (2/\pi)^2)/1.04 \\ R_T &= R_S/R, \quad C_T = C_L/C \end{aligned} \quad (2)$$

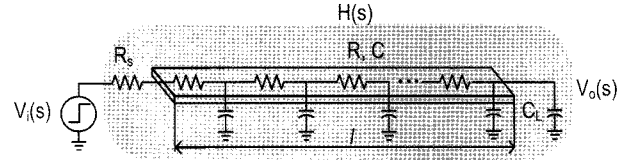


Fig. 3. An RC Interconnect Line.

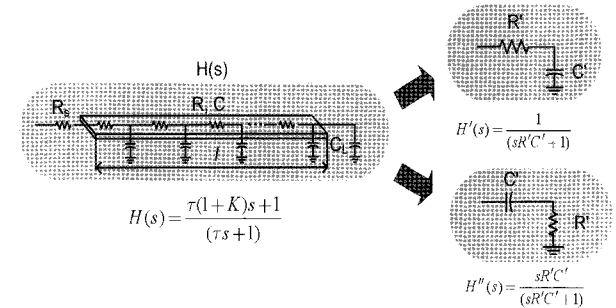


Fig. 4. Decomposition of the system function for an interconnect line.

$R(C)$ is the total resistance (capacitance) of the line. It can be represented with $R = R_u \cdot l(C = C_u \cdot l)$, where R_u and C_u are per-unit length (PUL)-resistance and PUL-capacitance, respectively and l is the length of the line. Since the frequency domain response of (1) becomes

$$V_o(s) = \frac{\tau(1+K)s+1}{s(\tau s+1)} = \frac{1}{s} \cdot \frac{\tau(1+K)+1}{\tau s+1} \quad (3)$$

the system function of the line can be regarded as

$$H(s) = \frac{\tau(1+K)s+1}{(\tau s+1)} = H'(s) + (1+K)H''(s) \quad (4)$$

where

$$\begin{aligned} H'(s) &\equiv \frac{1}{(\tau s+1)} \\ H''(s) &\equiv \frac{\tau s}{(\tau s+1)} \end{aligned} \quad (5)$$

In distributed RC line, the effective time constant is much smaller than that of the lumped model. Thus, defining R' as the total resistance of the system, C' can be determined as

$$\begin{aligned} R' &\equiv R_S + R = R(R_T + 1) \\ C' &\equiv \tau / R' \end{aligned} \quad (6)$$

Thus, since the time constant becomes

$$\tau = R'C' \quad (7)$$

$H'(s)$ and $H''(s)$ can be rewritten as

$$\begin{aligned} H'(s) &= \frac{1}{sR'C' + 1} \\ H''(s) &= \frac{sR'C'}{sR'C' + 1} \end{aligned} \quad (8)$$

Therefore, (4) can be represented with the combination of two equivalent circuits as shown in Fig. 4.

2. Time Domain Response at Intermediate Node

A discontinuous line can be represented with distributed circuit model as shown in Fig. 5 (a). Since the line is discontinuous, a system function needs to be determined in the discontinuous node (e.g., node-1). Note, unlike the circuit of Fig. 3 that has the lumped capacitance load, the intermediate node (i.e., the node-1) of the circuit of Fig. 5 (a) has the interconnect line as a load. Thus, (4) has to be modified a bit.

In order to determine the system function of the node-1,

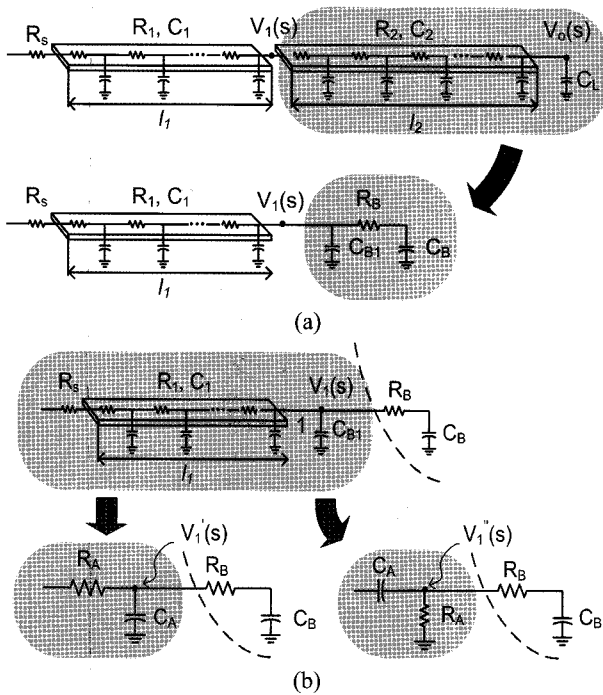


Fig. 5. The model simplification of an interconnect chain. (a) Circuit model of cascaded interconnects and driving point admittance approximation for the second line. (b) Decomposition of the first line.

the driving point impedance of the right hand side of the node is represented with an approximated lumped circuit as shown in Fig. 5 (a) [14]. Defining the input admittance at the node-1 as $Y_1(s)$, $Y_1(s)$ can be represented by its Taylor series expansion around $s=0$:

$$Y_1(s) = \sum_{n=1}^{\infty} y_n s^n = y_1 s + y_2 s^2 + y_3 s^3 + \dots \quad (9)$$

where y_n is the moment of the admittance for node-1. Then, the lumped circuit model parameters can be determined as

$$R_B = -y_3^2 / y_2^3 \quad C_B = y_2^2 / y_3 \quad C_{B1} = y_1 - y_2^2 / y_3 \quad (10)$$

Note that as shown in Fig. 6, the time domain response for such an approximation circuit has excellent agreement with that of the original circuit model.

Regarding C_{B1} as the load of the left-hand side line of the node-1, the discontinuous line can be represented as in Fig. 5 (b). Note that R_A and C_A can be determined by using the similar technique as in determining R' and C' ,

$$R_A \equiv R_s + R_1 = R_1(R_{T1} + 1), \quad C_A \equiv \tau_1 / R_A \quad (11)$$

Since the circuit of Fig. 5 (b) is similar to that of Fig. 4, combining (4) with (8), the transfer function of the left-hand-side line can be represented as

$$H_1(s) \approx H'_1(s) + (1 + K_1)H''_1(s) \quad (12)$$

where

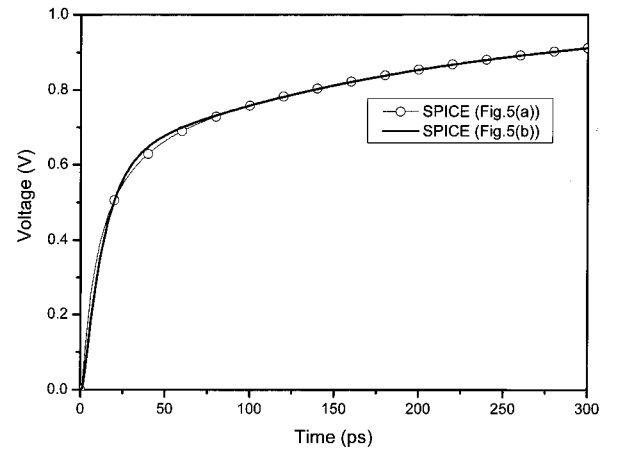


Fig. 6. Waveforms of node 1 for Fig. 5 (a) and Fig. 5 (b).

$$H_1'(s) = \frac{1 + sR_B C_B}{1 + s[R_A(C_A + C_B) + R_B C_B] + s^2 R_A R_B C_A C_B}$$

$$H_1''(s) = \frac{sR_A C_A (1 + sR_B C_B)}{1 + s[R_A(C_A + C_B) + R_B C_B] + s^2 R_A R_B C_A C_B}$$

Thus, $V_1(s)$ becomes

$$V_1(s) = \frac{1}{s} \cdot H_1(s) = \frac{1}{R_A R_B C_A C_B} \cdot \frac{(1 + sR_B C_B)[1 + sR_A C_A (1 + K_1)]}{s(s - p_1)(s - p_2)} \quad (13)$$

where

$$p_{1,2} = \frac{-b \pm \sqrt{b^2 - 4a}}{2a}$$

$$a = R_A R_B C_A C_B, \quad b = R_A(C_A + C_B) + R_B C_B$$

Thus, the time domain counter part is

$$v_1(t) = 1 + A_1 e^{p_1 t} + A_2 e^{p_2 t} \quad (14)$$

where

$$A_1 = \frac{1}{a} \cdot \left[\frac{1 + p_1 R_B C_B}{p_1(p_1 - p_2)} + \frac{R_A C_A (1 + p_1 R_B C_B)(1 + K_1)}{p_1 - p_2} \right]$$

$$A_2 = \frac{1}{a} \cdot \left[\frac{1 + p_2 R_B C_B}{p_2(p_2 - p_1)} + \frac{R_A C_A (1 + p_2 R_B C_B)(1 + K_1)}{p_2 - p_1} \right]$$

3. Time Domain Response at Output Node

Since $H_1(s)$ was determined, only if $H_2(s)$ is known, the response of the discontinuous line ($V_o(s)$) can be readily determined from the circuit of Fig. 5 (a),

$$V_o(s) = \frac{1}{s} \cdot [H_1'(s) + (1 + K_1)H_1''(s)]H_2(s) \quad (15)$$

Since the circuit of Fig. 5 (b) is similar to that of Fig. 4, from (1) and (4), $H_2(s)$ can be determined follows:

$$H_2(s) = \frac{\tau_2(1 + K_2)s + 1}{(\tau_2 s + 1)} \quad (16)$$

Thus, from (12), (15), and (16), $V_o(s)$ becomes

$$V_o(s) = \frac{1}{a} \cdot \frac{(1 + sR_B C_B)[1 + sR_A C_A (1 + K_1)] \tau_2(1 + K_2)s + 1}{s(s - p_1)(s - p_2)(\tau_2 s + 1)} \quad (17)$$

The time domain response becomes

$$v_o(t) = 1 + B_1 e^{p_1 t} + B_2 e^{p_2 t} + B_3 e^{p_3 t} \quad (18)$$

where

$$p_3 = -1/\tau_2$$

$$B_1 = A_1 \cdot \frac{p_1(1 + K_2) - p_3}{p_1 - p_3}$$

$$B_2 = A_2 \cdot \frac{p_2(1 + K_2) - p_3}{p_2 - p_3}$$

$$B_3 = \frac{K_2}{a} \cdot \frac{(1 + p_3 R_B C_B)[1 + p_3 R_A C_A (1 + K_1)]}{(p_3 - p_1)(p_3 - p_2)}$$

III. MODEL VERIFICATION

In order to verify the proposed technique, the various interconnect line parameters are defined as summarized in Table 1. Then, signal transients using (18) are compared with both [12] and SPICE simulation. As shown in Fig. 7, the signal transient wave shapes using the proposed model

Table 1. Tested Transmission Line Parameters.

	R_1 (Ω)	C_1 (pF)	R_2 (Ω)	C_2 (pF)
Case1	30	1	100	0.2
Case2	100	0.2	200	0.3
Case3	50	0.1	300	0.6
Case4	200	0.1	50	1

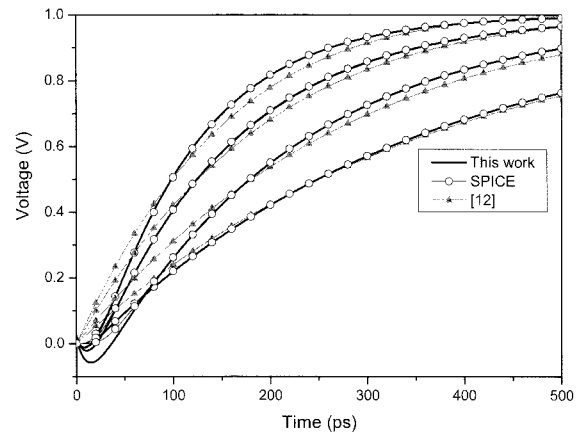
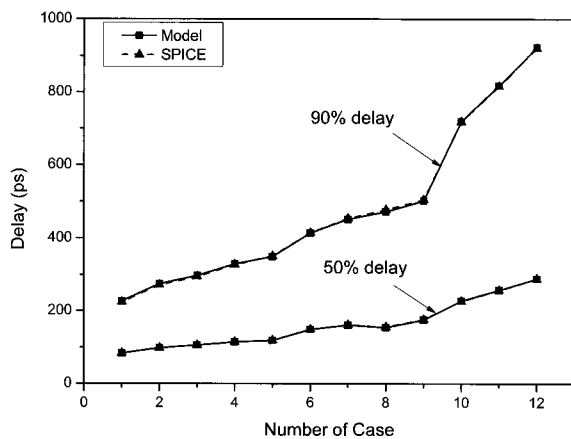


Fig. 7. Comparison of voltage waveforms at the output node. $R_s = 50 \Omega$, $C_L = 0.2$ pF.

Table 2. Tested parameters for model verification.

Case	R_S (Ω)	C_L (pF)	R_1 (Ω)	C_1 (pF)	R_2 (Ω)	C_2 (pF)
1	50	0.1	30	1	100	0.2
2	50	0.1	100	0.2	200	0.3
3	100	0.05	100	0.2	200	0.3
4	150	0.02	100	0.2	200	0.3
5	100	0.05	30	1	100	0.2
6	50	0.1	50	0.1	300	0.6
7	100	0.05	50	0.1	300	0.6
8	150	0.02	30	1	100	0.2
9	150	0.02	50	0.1	300	0.6
10	50	0.1	200	0.1	50	1
11	100	0.05	200	0.1	50	1
12	150	0.02	200	0.1	50	1

**Fig. 8.** Comparison of the proposed model with SPICE simulation for 50% and 90% time delay.

have excellent agreement with SPICE simulation. Therefore, the proposed model is more accurate than [12].

The 50% time delay and 90% time delay for various line parameters are determined as shown in Table 2 and Fig. 8. Note that the error between the model and SPICE simulation is less than 2%. Since the wave shapes are in agreement with the analytical model, interconnect line timing data may be readily determined by using the same algorithm [15].

IV. CONCLUSIONS

In this paper, since the generic circuit model of a discontinuous line is too much complicated to be analyzed, it was modeled as a cascaded interconnects line chain. Then an analytical expression for the signal transient wave shapes was derived by using the new simple equivalent

circuit. It was shown that the model expression has excellent agreement with SPICE simulation in less than 2% error in the delay estimation.

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Taehoon Kim received his B.S. in electrical and computer engineering from Hanyang University, Korea in 2007. He is currently working toward his M.S in Electrical and Computer Engineering at Hanyang University, Ansan, Korea.

His research interests are high-frequency characterization, modeling, and simulation concerned with the signal integrity verification of high-speed integrated circuits, IC interconnect, and IC packaging.



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Yungseon Eo received his B.S. and M.S. in electronic engineering from Hanyang University, Seoul, Korea, in 1983 and 1985, respectively, and his Ph.D. in Electrical Engineering from the University of Florida, Gainesville, FL, in 1993.

From 1986 to 1988, he was with the Korea Telecommunication Authority Research Center, Seoul, where he performed telecommunication network planning and software design. From 1993 to 1994, he was with Applied Micro Circuits Corporation, San Diego, CA., where he performed s-parameter-based device characterization and modeling for high-speed circuit design. From 1994 to 1995, he was with the Research and Development Center of LSI Logic Corporation, Santa Clara, CA, where he worked in the signal integrity characterization and modeling of high-speed CMOS circuits and interconnects. From 2004 to 2005, he was with High-Speed Microelectronics Group as a guest researcher at the National Institute of Standards and Technology (NIST), Boulder, CO. He is now a Professor of Electrical and Computer Engineering at Hanyang University, Ansan, Korea. His research interests are high-frequency characterization, modeling, and simulation methodology concerned with integrated circuits interconnects, integrated circuit packaging, and system level integration technology.