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Analysis and Control of a Modular MV-to-LV Rectifier based on a Cascaded Multilevel Converter

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ABSTRACT

In this paper a modular high performance MV-to-LV rectifier based on a cascaded H-bridge rectifier is presented. The proposed rectifier can directly connect to the medium voltage levels and provide a low-voltage and highly-stable DC interface with the consumer applications. The input stage eliminates the necessity for heavy and bulky step-down transformers. It corrects the input power factor and maintains the voltage balance among the individual DC buses. The second stage includes the high frequency parallel-output DC/DC converters which prepares the galvanic isolation, regulates the output voltage, and attenuates the low frequency voltage ripple ($2f_{line}$) generated by the first stage. The parallel-output converters can work in interleaving mode and the active load-current sharing technique is utilized to balance the load power among them. The detailed analysis for modeling and control of the proposed structure is presented. The validity and performance of the proposed topology is verified by simulation and experimental results.

Key words: Cascaded H-bridge rectifier, Voltage balancing, Parallel-output converters, Active load-current sharing

1. Introduction

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices[1]. Among the multilevel converters, the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels. Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters.

Different applications for the CHB converter have been

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proposed in the literature [2-6]. In [2], a cascaded H-bridge multilevel inverter has been investigated as a static VAR compensator. In the proposed method, the reactive power supplied by the STATCOM to the grid is regulated and the voltage unbalancing problems among the series H-bridges due to different power losses are avoided. Reference[3] has proposed a new configuration of a Unified Power Quality Conditioner (UPQC) which can be connected to the distribution system without a series injection transformer. The CHB converter has also been utilized as an active front-end rectifier in electric trains [4, 5]. This method allows the elimination of the heavy and bulky line transformer, thus reducing encumbrance and cost. In [6], a three-phase five-level cascaded inverter has been presented as a medium-voltage shunt active power filter, where a cycle-by-cycle PWM signal interchange technique is utilized for capacitor voltage balancing.

In this paper, a modular step-down AC/DC converter based on the CHB converter is presented. The converter structure is shown in Fig.1. This scheme can directly connect to the medium voltage levels and does not need the conventional step-down transformers which are bulky and heavy. The proposed rectifier can be utilized as an active rectifier in Uninterruptible Power Supplies (UPS) or in high-power Adjustable Speed Drives (ASDs). Another application is in the Power Electronic-based Transformers with DC links (PETs) [7].

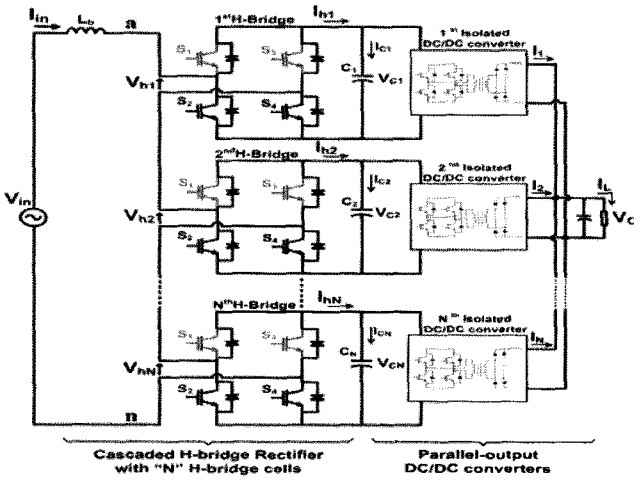


Fig. 1 Modular AC/DC converter based on CHB converter (upper switches in the CHB converter can be replaced by the fast diodes, in unidirectional applications)

The main control issues about the modular AC/DC converter are the voltage and power balancing among the series-input and parallel-output converters, respectively. Several references have studied the DC-bus voltage balance problem in the CHB converters, and proposed different control strategies using low-frequency modulation techniques, as exemplified in [8, 9]. Other references have proposed control methods to achieve active load current sharing among the parallel-output converters[10, 11]. The application of these methods, however, is not straightforward for the AC/DC converters.

In this paper, a new control strategy is presented to ensure that the capacitor voltages converge to the reference value, even if the series H-bridges do not match perfectly or have different power losses. The input current is programmed to be sinusoidal and in phase with the input voltage. However, it is possible to adjust the input power factor to control both the active and reactive powers. An active load-current sharing method is also presented to balance the load power among the parallel cells. Analytical formulas are derived to calculate the effects of mismatches on the equal load current sharing. The performance of the converter and validity of the new approach are verified by simulation and experimental results on a laboratory scale prototype.

2. System Configuration

The power structure shown in Fig. 1 includes two parts: the front-end CHB converter and the parallel-output DC/DC converters which are explained in the following paragraphs.

2.1 Cascaded H-bridge converter

The CHB converter is the best choice for working in high-voltage and high-power applications due to the extreme modularity, simple physical layout, and low losses. As it can be seen from Fig. 1, the CHB converter has N H-bridge cells connected in series. Each H-bridge consists of four power switches (with anti-parallel diodes) and a DC bus capacitor. Each capacitor feeds a high-frequency DC/DC converter.

It is worth noting that the unidirectional rectifier can be realized from the bidirectional rectifier by turning off the

upper switches of the H-bridge cells (or by replacing the upper switches with relatively fast diodes). In this work, the bidirectional CHB converter is analyzed, and the results are used for the unidirectional converter as well.

In Fig. 1, the AC terminal voltage of the rectifier, V_{an}, can be written as follows:

$$V_{an} = V_{h1} + V_{h2} + \cdots + V_{hN} \quad (1)$$

$$V_{hi} = h_i \cdot V_{Ci} \quad ,i = 1,2,\ldots,N \quad (2)$$

where V_{hi}, V_{Ci}, and h_i are the AC terminal voltage, the capacitor voltage, and the switching function of the i^{th} H-bridge (or cell), respectively. Assuming $V_{C1} = V_{C2} = \cdots = V_{CN} = V_C$, where V_C is the reference voltage of DC buses, each cell can generate three voltage levels: $+V_C$, $-V_C$, and zero on the AC side. Therefore, using N H-bridge cells, a maximum of 2N+1 different voltage levels are obtained to synthesize V_{an}. Applying the Kirchhoff Voltage Law (KVL) at the input voltage loop yields:

$$V_{in} = V_{an} + L_b \frac{dI_{in}}{dt} \quad (3)$$

where V_{in} is the input voltage, I_{in} the input current, and L_b the input inductance which is used to shape the input current. Applying Kirchhoff Current Law (KCL) for each cell leads to:

$$I_{hi} = h_i \cdot I_{in} \quad ,i = 1,\ldots,N \quad (4)$$

where I_{hi} is the current of i^{th} H-bridge and is a function of the input current. The equations (1)-(4) describe a Linear Time Varying system with one input (V_{in}) and N+1 states (V_{C1} to V_{CN} and I_{in}). The CHB controller should determine the switching functions, h_1 to h_N, to maintain voltage balancing.

2.2 Parallel-Output DC/DC converters

The second part of the proposed rectifier (Fig.1) contains the parallel-output DC/DC converters. These converters are connected to the distinct DC buses of the CHB rectifier, and are joined to each other at the output side. This extremely modular structure prepares a low-voltage and highly-stable DC output. Additionally, it provides the galvanic isolation between the input and output, regulates the output voltage, and reduces the low frequency voltage ripple generated by the first part, which is inherent to the power factor correction.

In the second stage, different type of DC/DC converters can be utilized. Among the high efficiency isolated converters, the semi-soft switched full-bridge converter presented by [12] has an efficiency equal to that of the zero voltage switched full-bridge converter, but it is much easier to control and does not need an additional series inductor. This converter takes advantage of low leakage inductance and has low turn off losses. Also, the DC bus is maximally used and the converter can utilize the secondary side clamp circuits, resulting in lower reverse recovery related losses.

Due to the interesting features, simplicity, and good performance of the semi-soft switched converter, we can utilize it as the core cell of the isolation stage. It is possible to apply the interleaving technique among the parallel cells to achieve advantages such as a lower current ripple in the output capacitor, faster transient response to load changes[13], and improved power handling capabilities. The filter requirement is also reduced, leading to a higher power density, and possibly higher efficiency of the overall system [11].

Several attempts have been made to combine the functions of the PFC stage (first part) and the isolation stage (second part) to reduce the number of solid-state switches and overall cost. However, the advantage of the two-stage approach is that the CHB converter provides regulated intermediate bus voltages (V_{Ci} = 600V in this case), which facilitates the design optimization of both converters with respect to efficiency. Since in a two-stage front-end converter the design of both stages can be more easily optimized, the overall performance is improved as compared to a single-stage topology. Thus, we use a two-stage design and by proper design, the flexibility, reliability and performance of the whole converter are improved.

3. Modeling and Control of the Modular AC/DC Converter

The modular AC/DC converter consists of two parts and each part can be controlled independently from the other one because the intermediate bus capacitors (C_1 to C_N) are large enough to decouple the operation and the control of both stages, as illustrated in Fig.1.

3.1 Control of the cascaded H-bridge converter

The main challenges associated with the cascaded rectifier control are shaping the input current, controlling the input power factor, and holding the DC bus voltages at the desired reference value. The CHB converter, in the rectification mode, aims to achieve N equal DC voltages across the capacitors (C_1 to C_N). However, this can become difficult if the series H-bridges have slightly different characteristics or have different power losses. When implementing very high voltage converters, even the parasitic stray capacitances to earth can lead to unwanted scaling effects and leads to unequal voltage distribution among the series connected converters.

Fig. 2 shows the basic block diagram of the proposed controller. It consists of the analog and digital parts. The analog controller generates the PWM signal, Q. This controller consists of two control loops: the inner current loop and the outer voltage loop. The voltage loop contains a PI controller to regulate the total voltage of DC buses to the reference value, i.e. $\sum V_{Ci} = N \cdot V_C$. The digital controller generates a square-wave synchronized signal, V'_{in}, from the input voltage.

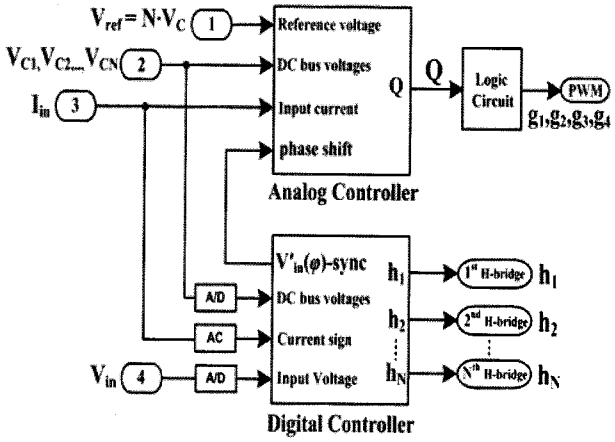


Fig. 2 Block diagram of the proposed controller for the CHB converter

In Fig. 2, the sync signal V'_{in} has the same frequency as the input voltage and its phase is adjusted by the digital controller. The square-wave signal is filtered by a forth-order Butterworth filter and its output is multiplied by the output of the PI controller. Using this method, a pure sinusoidal reference is generated and the input power factor (or the reactive power) is also controlled. After generating the reference current, the inner current loop programs the input current to follow the reference current I_{in}^*.

The task of digital controller is to keep voltage balancing across the DC link capacitors. This controller determines the appropriate switching functions, h_1 to h_N, for N H-bridge cells. Each switching function h_i (i=1,..., N) corresponds to four operating modes: "0", "+1", "-1", and PWM. The operating mode "0" corresponds to the conduction of bottom switches (S_2, S_4), in a cell. In modes "+1" and "-1" the diagonal switches (S_1, S_4) and (S_2, S_3) are turned on, respectively. In PWM mode, the gate signals, g_1 to g_4, drive the corresponding cell. These signals are obtained from Q, the output of the analog controller, as follows:

$$g_1 = V\overline{Q}, \quad g_2 = \overline{V\overline{Q}} \tag{5}$$

$$g_3 = \overline{V}Q, \quad g_4 = \overline{\overline{V}Q} \tag{6}$$

where V is the sign of input voltage and it is one if the input voltage is positive; otherwise it is zero.

To take advantage of both low frequency (stepped modulation) and high frequency (PWM) modulation techniques, the hybrid modulation method is employed which is shown in Fig. 3.

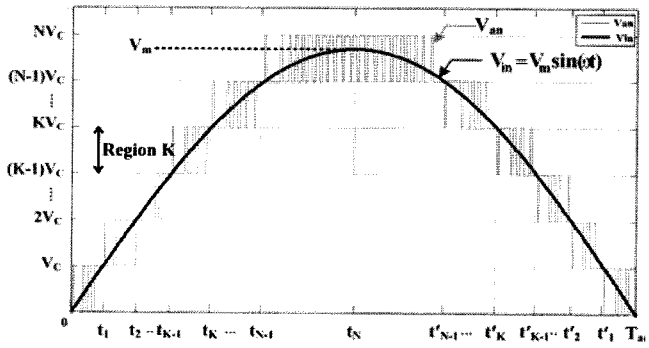


Fig. 3 Definition of voltage regions for K=1,..., N

According to Fig. 3, the input voltage V_{in} is divided into equal sections with the scale of V_C (V_C is the reference of the primary DC links). The voltage region K is then defined as follows:

$$(K-1)\cdot V_C < |V_{in}| < K\cdot V_C \quad ,K = 1,\ldots,N \tag{7}$$

Region K is where the magnitude of input voltage, $|V_{in}|$, lies between (K-1)V_C and KV_C. The minimum number of cells to synthesize the multilevel waveform, V_{an}, is equal to the closest integer greater than (V_m/V_C), where V_m is the peak input voltage. The following benefits can be achieved by utilizing the hybrid modulation technique:

- Considerable reduction in size and volume of the input inductance L_b; because the input inductance will not tolerate a voltage of more than V_C.
- Reduction in THD and EMI at the input side.
- Low switching loss; because at each time only one cell works in high frequency mode.

The digital controller performs the control algorithm to maintain the voltage balancing across the DC link capacitors, while the analog controller regulates the sum of the DC bus voltages to N·V_C. The proposed control rules, defined hereafter, aims to synthesize the waveform shown in Fig. 3 and to maintain the voltage balancing at the primary DC sides.

1. If $V_{in} > 0$, $I_{in} > 0$, and the voltage region is K, then (K-1) cells with the lowest DC bus voltage are chosen to be charged in mode "+1", the K^{th} cell in PWM mode, and the rest in mode "0".
2. If $V_{in} > 0$, $I_{in} < 0$, and the voltage region is K, then (K-1) cells with the highest DC bus voltage are chosen to be discharged in mode "+1", the K^{th} cell in PWM mode, and the rest in mode "0".
3. If $V_{in} < 0$, $I_{in} > 0$, and the voltage region is K, then (K-1) cells with the highest DC bus voltage are chosen to be discharged in mode "-1", the K^{th} cell in PWM mode, and the rest in mode "0".
4. If $V_{in} < 0$, $I_{in} < 0$, and the voltage region is K, then (K-1) cells with the lowest DC bus voltage are chosen to be charged in mode "-1", the K^{th} cell in PWM mode, and the rest in mode "0".

To perform the above rules, the digital controller takes the voltage and current samples with the sampling frequency f_o ($f_o < f_{PWM}$). Then, the region of input voltage, K, is updated according to (7), the control algorithm is performed, and the appropriate switching functions, h_1 to h_N, are determined. The switching functions are applied to the H-bridge cells and the operating modes are performed. This procedure is repeated in the next sampling periods. As a result, the voltage of DC buses is controlled by adjusting the average current fed to the H-bridge cells, over the mains half-cycle (see Fig. 7(b)).

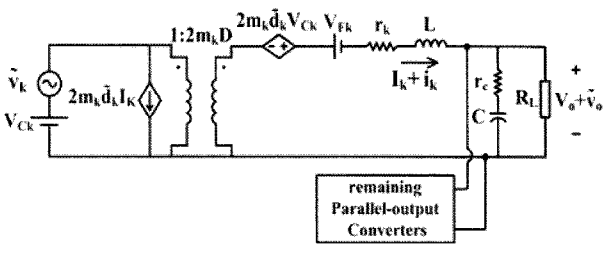
3.2 Modeling of the parallel-output full-bridge converters

The DC/DC converter utilized in the isolation stage is modeled under the following assumptions:

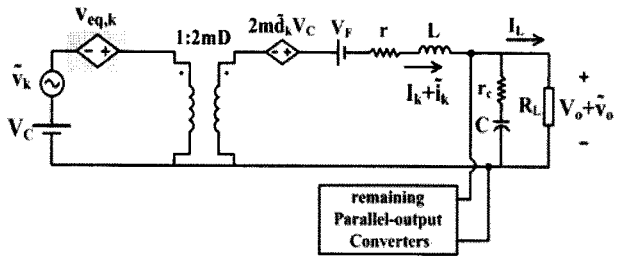
1) Each power switch in the on-state is modeled by a constant voltage source $V_{on,s}$ and a series resistance r_{ds} and in the off state by an infinite resistance.
2) Each diode in the on-state is modeled by a constant voltage source $V_{on,d}$ and a series resistance r_d, and in the off state by an infinite resistance.
3) The parasitic capacitances are neglected.
4) The isolation transformer is assumed to be ideal.
5) The DC/DC converter works in the Continues Conduction Mode (CCM).

To simplify the representation of equations, in the remainder of this manuscript we use the small letter 'x' as a large signal parameter, the capital letter 'X' as a DC value, and the '$\tilde{x}$' symbol as a small signal variable, i.e. $x = X + \tilde{x}$.

According to the above assumptions and the modeling method discussed in [14, 15], the large signal averaged model of the PWM full bridge converter is realized and shown in Fig.4(a).



(a)



(b)

Fig. 4 Modeling of the parallel-output cells: (a) Large signal averaged model of the k^{th} cell, where $n_k=n+n_{pk}$, $r_k=r+r_{pk}$, and $V_{Ck}=V_C+V_{pk}$ (b) Simplified model when the parasitic terms and input DC offset of the k^{th} cell are modeled with $V_{eq,k}$

The illustrated transformer in Fig. 4 is an analytical model that is valid for the entire frequency domain. In Fig.4, V_{CK}, V_O, and I_K are the DC values of the input voltage, output voltage and the load current, respectively. Also $\tilde{v}_k$, $\tilde{v}_o$ and $\tilde{i}_k$ are the corresponding small signal values. The variable D represents the duty cycle of the full-bridge converter and is defined as: $D = t_{on}/T_s \leq 0.5$, where t_{on} is the time duration in which the diagonal switches are on, and T_s is the switching period. Also $\tilde{d}$ represents the corresponding small signal value of the duty cycle. The parameters m, r_c, V_F and r are the transformer ratio, equivalent series resistance of the capacitor, the equivalent averaged voltage drop and the equivalent averaged resistance, respectively. For V_F and r, it is derived:

$$V_F = 2(V_{on,d} + V_{on,s} \cdot 2mD) \tag{8}$$

$$r = r_L + (0.5+D)(2r_d + r_{t2}) + 2Dm^2(2r_{ce} + r_{t1}) \tag{9}$$

where r_L is the equivalent series resistance of the inductor, r_{t1} the resistance of the primary winding and r_{t2} the resistance of the secondary winding. Equations (8) and (9) have been derived using the principle of energy conservation [15].

In practice, when N ideal DC/DC converters are paralleled at the output side, the load current is divided equally among them. However, a very small mismatch among the parallel converters can lead to unequal load current sharing. The main source of mismatches are from the transformers voltage ratio (due to the, e.g., leakage flux), the primary voltage offsets, and the equivalent series resistances. Although this issue will not lead to instability and runaway condition in the modular structure because of the CHB rectifier control, it will cause unequal thermal stress on the components of the parallel converters and a low performance of the converter.

We assume that the transformer ratio (m_k), the cell input voltage (V_{Ck}), and the equivalent averaged resistance (r_K) of the k^{th} cell can be written as:

$$m_k = m + m_{pk}, \quad m_{pk} << m \quad , k=1,\ldots, N \tag{10}$$

$$V_{Ck} = V_C + V_{pk}, \quad V_{pk} << V_C \quad , \quad k=1,\ldots, N \tag{11}$$

$$r_k = r + r_{pk} \quad , \quad r_{pk} << r \quad , \quad k=1,\ldots, N \tag{12}$$

where m, V_C and r are the desired values of each H-bridge and m_{pk}, V_{pk} and r_{pk} are the parasitic terms or deviations from the nominal values. Considering m_k, V_{Ck} and r_k in the large-signal model shown in Fig. 4(a) and analyzing the circuit, a simplified model is achieved, where the effect of parasitic terms is modeled with a controlled DC voltage source, $V_{eq,k}$, as

$$\begin{aligned} V_{eq,k} &= \frac{\left(2m_{pk}(D+\tilde{d}_k)V_{Ck} + r_{pk}I_k\right)}{2mD} + V_{pk} \\ &\approx \frac{m_{pk}}{m}V_C + \frac{r_{pk}I_k}{2mD} + V_{pk} \quad , k = 1,\ldots, N \end{aligned} \tag{13}$$

where $V_{eq,k}$ is a controlled DC voltage source that represents the effects of mismatches and the input DC offset of the k^{th} converter cell. Fig. 4(b) shows the simplified model of the k^{th} cell according to (13). In the simplified scheme, the controlled current source has been deleted; because, it is parallel with the input voltage and does not affect the output voltage v_o and the cell current i_k.

The DC voltage, $V_{eq,k}$, acts such as a DC offset and causes the current offset among the parallel cells. The amount of current offset, $I_{off,k}$ $(k=1,\ldots, N)$, is obtained as follows:

$$\begin{bmatrix} I_{off\,1} \\ I_{off\,2} \\ \vdots \\ I_{offN} \end{bmatrix} = \frac{2mD}{Nr} \begin{bmatrix} (N-1) & -1 & -1 & -1 \\ -1 & (N-1) & -1 & -1 \\ & & \vdots & \\ -1 & -1 & -1 & (N-1) \end{bmatrix} \cdot \begin{bmatrix} V_{eq\,1} \\ V_{eq\,2} \\ \vdots \\ V_{eqN} \end{bmatrix} \quad (14)$$

From (14), it is concluded that a little voltage offset in an H-bridge cell will cause large current offsets among the parallel cells. For example, if the number of parallel cells is N = 5, r = 0.6 Ω, and 2mD ≈ 1, then an offset of 3 V (0.5 %) in the first cell will cause the following offsets: I_{off1} = +4 A and I_{off2} to I_{off5} = -1 A.

3.3 Control of the parallel-output converters

The controller of the parallel-output converters has two main functions: regulation of the output voltage and the load current sharing among the parallel converters. The proposed controller is shown in Fig. 5. This controller uses a voltage control loop and N similar current control loops.

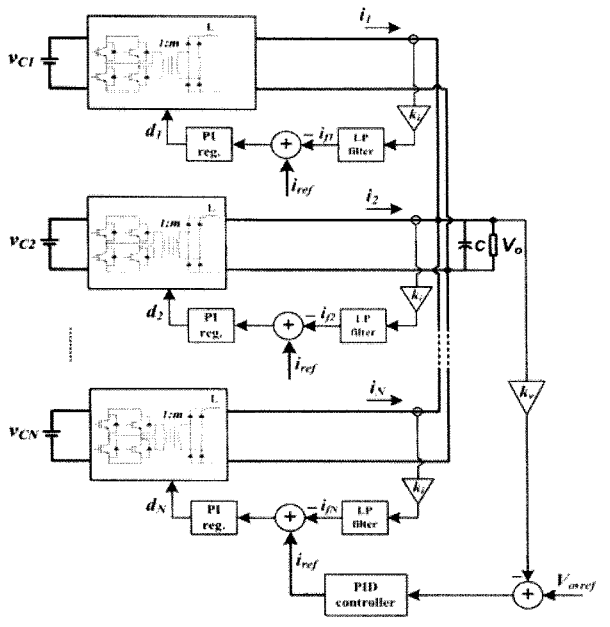


Fig. 5 Proposed scheme for control of parallel-output cells

In Fig.5, the current controllers are designed to provide equal load current sharing among the parallel cells. As it can be seen, the inductor current of the k^{th} cell is sensed and scaled to the proper magnitude. Then, it passes through a low pass filter. This filter is utilized to limit the loop bandwidth and to decrease the noise power. The filter output is compared with the reference current i_{ref} generated by the voltage controller. The error signal is entered to the PI regulator and its output determines the switching duty cycle d_k. The duty cycle expression can be written as follows:

$$d_k = D + D_{off,k} + \tilde{d} \quad , \mathrm{k} = 1,\ldots, \mathrm{N} \quad (15)$$

where d_k is the duty cycle of the k^{th} cell, D is the DC term, and $D_{off,k}$ is a small DC term which is generated by the k^{th} current controller to cancel the offset term defined in (14). According to Fig.4(b), $D_{off,k}$ is derived as follows:

$$\begin{aligned} &2m(D+D_{off,k})\cdot(V_C+V_{eq,k}) \\ &=2m(DV_C+D_{off,k}V_C+DV_{eq,k}+D_{off,k}V_{eq,k}) \end{aligned} \quad (16)$$

In (16), the last term is negligible in comparison with the other terms. As the desired voltage is $2mDV_C$, the remaining terms are set to zero. So, it is obtained:

$$2m(D_{off,k}V_C + DV_{eq,k}) = 0 \rightarrow D_{off,k} = -\frac{DV_{eq,k}}{V_C} \quad (17)$$

As a result, the effects of mismatches and the input voltage offsets (modeled as a part of $V_{eq,k}$) are canceled by the inner current loops and equal DC operating points are achieved for all cells, as follows

$$I_k = I_L/N \ , \ V_{Ck} = V_C \ , \ D \approx \frac{V_O}{V_C}\cdot\frac{1}{2m}\cdot\frac{R_L + r/N}{R_L} \quad (18)$$

It is worth noting that the variable $\tilde{d}$ in (15) is a small signal duty cycle which corresponds to the input voltage and load current variations. This term controls the dynamical behavior of the parallel cells. Furthermore, the external voltage loop, shown in Fig. 5, is used to regulate the output voltage of parallel converters to the reference value $V_{o,ref}$. The output of the PID controller is used as a reference current for all parallel cells. This controller compensates the load side variations.

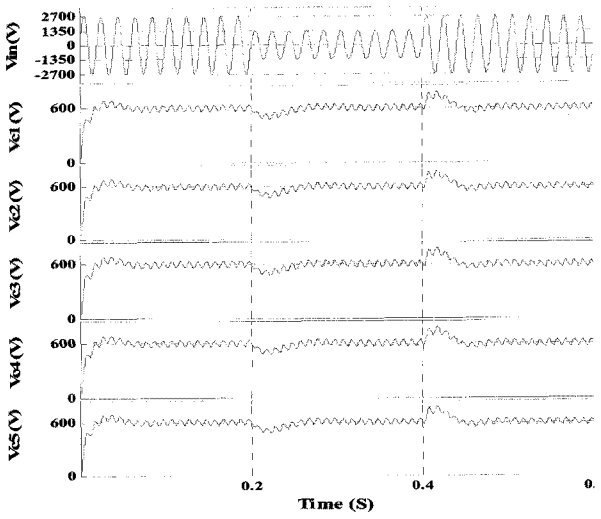
4. Simulation Results

The configuration which has been chosen to verify the controllers behaviors is a 30 kW, 11-level, medium voltage converter with 5 series-connected H-bridges at the MV side (3.3 kV) and 5 parallel-output cells at the LV side (600 V). The reference of primary DC buses, V_{C1} to V_{C5}, is V_C = 600 V, the line side inductance L_b= 5 mH, DC bus capacitors C_i = 470 μf, sampling frequency f_o = 3 kHz, switching frequency f_s= 10 kHz, and transformer ratio m=1:1.2. Computer simulations are carried out using the MATLAB-SIMULINK program.

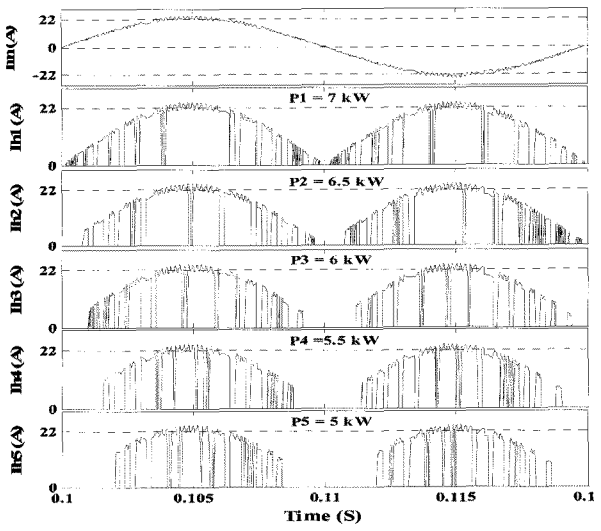
The first simulation investigates the behavior of the CHB rectifier control, where the isolated converters are modeled with the resistive loads. This simulation verifies the controller performance when the series converters extract different amounts of electric power. It is assumed that the supplied power to the H-bridge cells are P_1 = 7 kW, P_2 = 6.5 kW, P_3 = 6 kW, P_4 = 5.5 kW, and P_5= 5 kW. Additionally, to investigate the dynamical behavior of the controller, a 50% voltage sag appears in the primary voltage at t = 0.2 s and lasts 200 ms. The simulation results are shown in Fig. 7(a) and 7(b).

Fig. 7(a) shows the waveforms of the input voltage V_{in} and the primary capacitor voltages, V_{C1} to V_{C5}. It is observed that all DC buses follow the reference voltage V_C = 600 V in both transient and steady state conditions, although the H-bridge cells extract different amounts of power. At transient times, t = 0.2 s and t = 0.4 s, the capacitor voltages return to the initial values in less than 60 ms. The low frequency ripple, which is observed at the DC buses, is inherent to the power factor correction and will be eliminated by the isolation stage.

Fig. 7(b) shows the waveforms of the input current I_{in} and the cells currents, I_{h1} to I_{h5}, over a main period. The input current is a sinusoidal waveform with a high frequency ripple generated by the PWM method. The plurality of series-connected cells leads to achieve an effective switching frequency that is many times the switching frequency of individual cells. The input current is also in phase with the input voltage. Additionally, each cell current I_{hi} contains a DC term, a low frequency harmonic ($2f_{line}$) and a high frequency switching ripple. At steady-state, the low and high frequency components flow into the i^{th} capacitor and the DC term (the cell average current over a half-cycle) is equal to the i^{th} load current. The obtained result in Fig. 7(b) confirms the validity of this discussion.



(a)



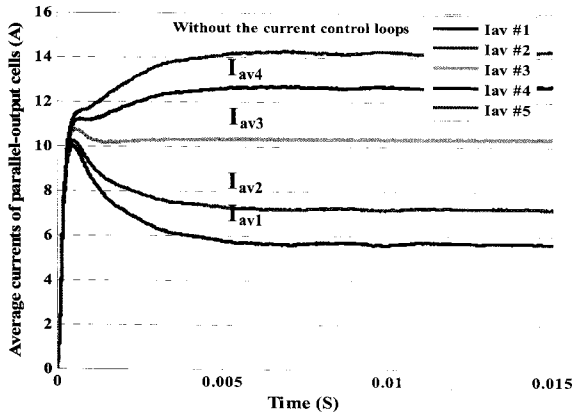
(b)

Fig. 7 Verifying the CHB converter control:
(a) Input voltage (top) and primary DC bus voltage waveforms, V_{C1} to V_{C5}, in sag period
(b) input current top) and cell currents, I_{h1} to I_{h5}, for a mains half cycle efore sag event

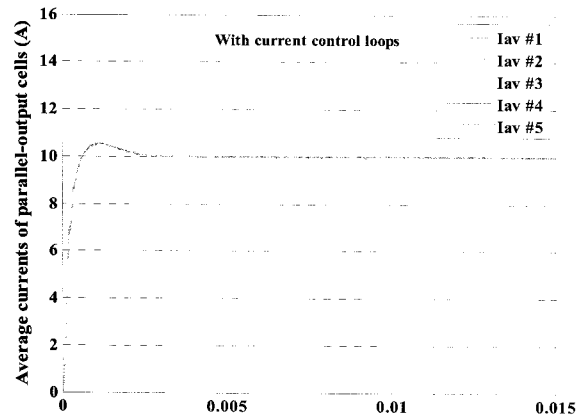
In the second simulation, the performance of the current controllers in the isolation stage is verified. Moreover, the validity of Eq. (14) is verified by the simulation. It is assumed that the total load power is 30

kW and the primary DC buses have very small offsets, e.g., V_{off1} = -3 V, V_{off2} = -2 V, V_{off3} = 0 V, V_{off4} = 1.5 V, and V_{off5} = 2.5 V (compared to the DC bus voltages V_{Ci} = 600 V). Slight mismatches in the feedback passes of the CHB converter may cause voltage offsets. If the current controllers are not used in the control circuit, the voltage offsets will cause a large current deviation among the parallel cells. This situation is shown in Fig.8(a). Further, the offset currents are determined from (14), as follows:

$$\begin{bmatrix} I_{off\,1} \\ I_{off\,2} \\ I_{off\,3} \\ I_{off\,4} \\ I_{off\,5} \end{bmatrix} = \frac{1}{5\times 0.6} \begin{bmatrix} +4 & -1 & -1 & -1 & -1 \\ -1 & +4 & -1 & -1 & -1 \\ -1 & -1 & +4 & -1 & -1 \\ -1 & -1 & -1 & +4 & -1 \\ -1 & -1 & -1 & -1 & +4 \end{bmatrix} \begin{bmatrix} -3 \\ -2 \\ 0 \\ 1.5 \\ 2.5 \end{bmatrix} = \begin{bmatrix} -4.67 \\ -3 \\ +0.33 \\ +2.83 \\ +4.5 \end{bmatrix}$$



(a)



(b)

Fig. 8 Verifying the isolation stage converter control (a) average current of parallel cells without the current controllers (b) average currents in presence of current controllers

Comparing the analytical result with the simulation result in Fig. 8(a) confirms a good agreement between two results. Without the current controllers, the cells currents are divided unequally among the parallel cells. This can bring unequal use of the power switches and increases the complexity of the cooling system and the design.

Fig. 8(b) shows the cells average currents (I_{av1} to I_{av5}) when the current controllers are used. It is observed that the current controllers provide equal load current sharing among the parallel cells, even in the start up period. Each controller generates a compensating duty cycle, according to (17), to cancel the primary voltage offset. The obtained result in Fig. 8(b) confirms the usefulness of the proposed approach.

5. Experimental Results

In this section, the validity of the proposed approach and the designed controllers are verified by experimental results on a laboratory scale prototype. The hardware prototype is an 1800 W single-phase AC/DC converter based on a 7-level CHB converter which is illustrated in Fig. 9. The prototype consists of three series converters at the input side and three parallel cells at the load side. The input AC voltage is 230 Vrms and can vary between 70 and 260 Vrms. The reference voltage for intermediate DC buses is V_C = 125 V and the output voltage V_o = 100 V. The digital control unit is implemented based on a TMS 320F2812 DSP controller. Other principal parameters of the prototype are given in Table 1.

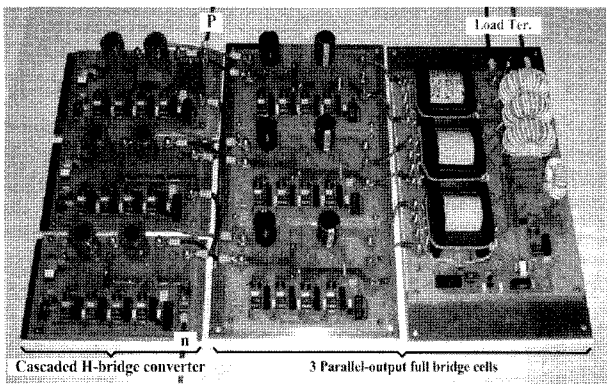


Fig. 9 Modular step-down AC/DC rectifier based on the cascaded H-bridge converter

Table 1 Principal parameters of the experimental prototype

Parameter or Component	Symbol	Value
Number of series H-bridges (cells)	N	3
Nominal power	P	1800 W
Input AC voltage	V_{in}	70-260 V rms
Intermediate DC Bus voltage	V_C	125 V
Output DC voltage	V_o	100 V
Input line inductance	L_b	2 mH
Switching frequency of parallel cells	f_s	15 kHz
Intermediate DC bus capacitor	C_i	1 mF, 250V
Output capacitor	C_o	470 uF, 160V
Output inductor	L_o	220 uH
Steady state Duty cycle	D	0.4
Isolation transformer turn ratio	M	1:1
Solid-state power switches	S_i	IRFP250, 200V
Secondary diodes	D_i	BYW81, 200V
Equivalent average resistance	r	0.26 Ω

It is worth noting that the low voltage power MOSFETs (MOSFET+Internal Body Diode with the break down voltage of 200 V) have been intentionally used in the prototype to demonstrate a scaled-down version of the real situation. However, in medium voltage levels, the IGBTs would be the best choice owing to better voltage and current ratings.

The first experiment investigates the voltage balancing and the current control mechanisms in two cases: with and without the CHB controller. In this experiment, the CHB converter is connected to the resistive loads and the loads are selected as P_1 = 625 W, P_2 = 488 W and P_3= 312 W. The voltage of the DC buses and waveform of the input current are shown in Fig.10.

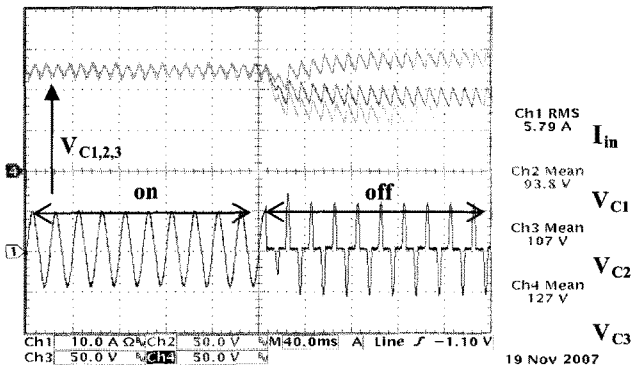


Fig. 10 DC bus voltages and the input current waveforms when the CHB controller is on and off

According to Fig. 10, when the CHB converter control is turned off, the voltage of DC buses diverge from the reference value V_C = 125 V. Without the controller, the current waveform is distorted, low order harmonics appear, and the power loss increases significantly. In addition, the power factor reduces considerably, leading to more generation of reactive power and reduction of real power capacity.

Fig.11 shows the operation principle of the CHB converter. Using 3 series connected H-bridges, a 7-level voltage waveform is obtained to synthesize the AC terminal voltage V_{an}. It is observed that the power switches, located in the H-bridge cells, will not tolerate voltage of more than V_C ($V_C < V_m$). This result confirms the feasibility of working at voltage levels beyond the classic semiconductor limits.

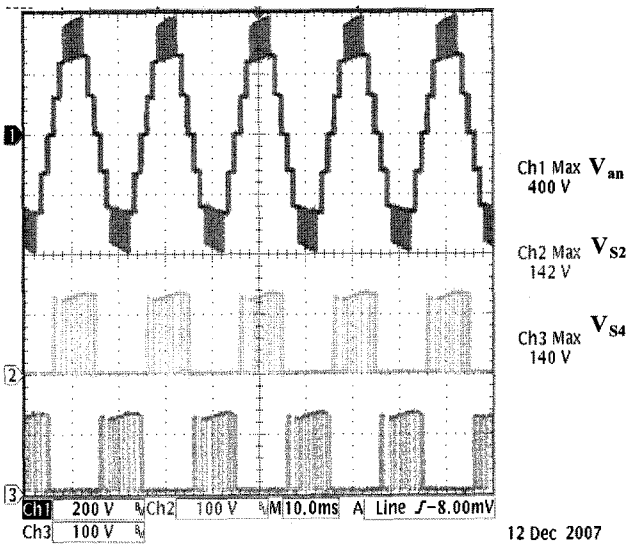


Fig. 11 Operation principle of CHB converter: AC terminal voltage V_{an}, and voltage of power switches

The second experiment investigates the power balancing mechanism among the parallel-output cells. Here, the parallel-output cells are connected to the CHB converter and fed by the primary DC buses. In Fig.12, the average input power transferred to the parallel cells is demonstrated as a function of the source voltage. To investigate the controller behavior, the power and voltage points are measured using the power analyzer and are

shown for two cases: with the current control loops in Fig. 12(a) and without the current control loops in Fig. 12(b).

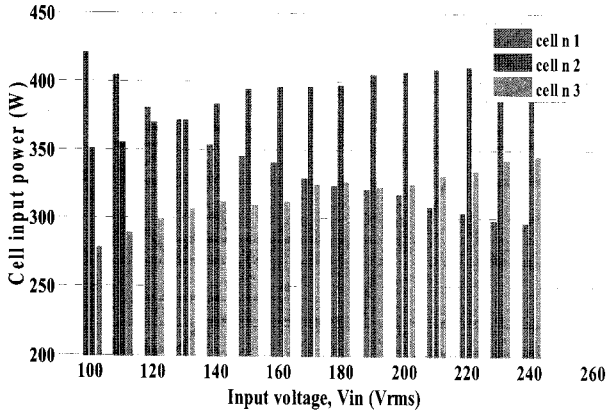


Fig. 12(a) Parallel cells input power versus the AC input voltage, without the current controllers

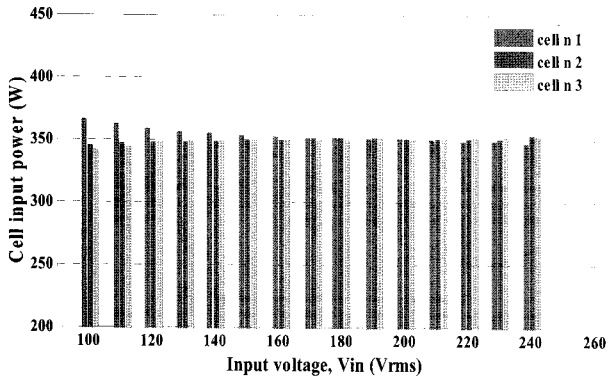


Fig. 12(b) Parallel cells input power versus the AC input voltage, in presence of current controllers

As it can be seen from Fig. 12(a), when the current control loops are not utilized, the load power is divided unequally among the parallel cells and is dependent on the converter operating point. On the other hand, without the current controllers, the load sharing among the parallel cells is different and even the cells have been made in the same manner. This is due to the slight mismatches of the converters and the DC offsets at the primary DC buses.

Fig. 12(b) shows the cells powers when the current loops are utilized. It is observed that the load power is divided equally and symmetrically among the parallel cells. In this test, each current loop corrects the cell duty cycle according to (17) and the current sharing is well done.

The next experiment verifies the dynamic behavior of the CHB converter control and the current controllers under load steps. In this experiment, the input voltage is 230 V and the load power changes between 900 W and 1800 W, in a step-wise manner. The power and voltage points are measured with the power analyzer, NORMA 5000. The total load power, average DC bus voltages (V_{C1} to V_{C3}), and the average input power delivered to the isolated cells are shown in Fig.13. Since the cell voltages are equal, the average input power to each cell would be proportional to the cell average current.

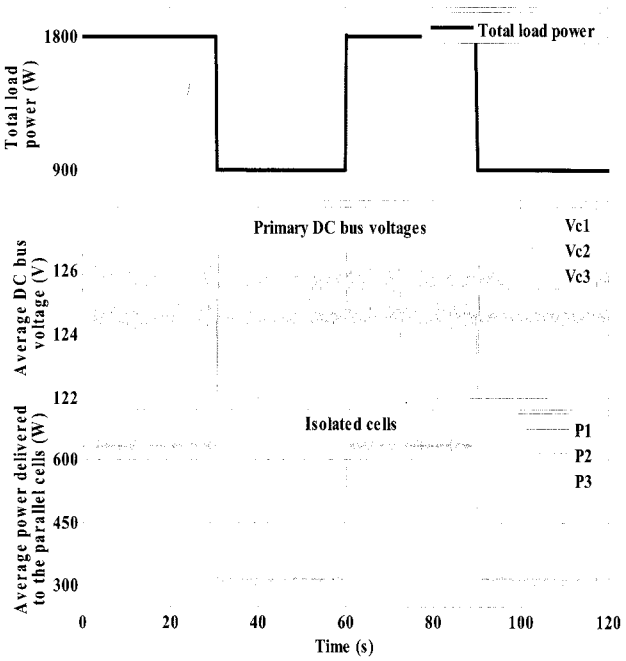


Fig. 13 Dynamical behavior of the CHB converter control and the current controllers under load steps: Total load power (top), average DC bus voltage waveforms (middle), and average input power delivered to the parallel cells (bottom)

As it can be seen from Fig.13, in spite of quick load variations, the CHB converter controls the voltage of primary DC buses and they follow the reference voltage (V_C =125 V) by a DC offset of less than 1%. In the isolation stage, the current controllers compensate the DC offsets seen at the primary DC buses and provide equal load current sharing among parallel cells, in both transient and steady state conditions.

6. Conclusions

In this paper, a modular step-down AC/DC rectifier was presented. The modular structure offers important advantages during design, testing, manufacturing and service stages. The same modules can be used for different voltages (or currents) by stacking (or paralleling) the appropriate number of modules depending on the working voltage (or power). The utilized rectifier contains two parts. At the input side, there is a cascaded H-bridge rectifier which connects directly to the medium voltage levels and corrects the input power factor. The second stage is a modular parallel-output converter which provides a low-voltage and highly-stable DC interface with the consumer applications.

In this paper, a new control strategy was presented to ensure that the primary capacitor voltages converge to the reference value, even if the series H-bridges do not match perfectly or have different power losses. The proposed controller programs the input current to be sinusoidal and in phase with the input voltage. An active load-current sharing method was also presented to balance the load power among the parallel cells. Analytical formulas were derived to calculate the effects of mismatches on the equal load current sharing. The validity of the design and the rectifier performance were verified by simulation and experimental results.

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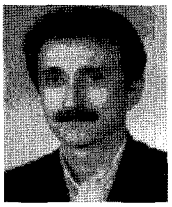

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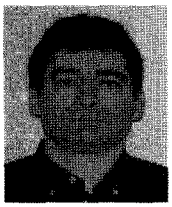

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