JPE 9-6-4

Super-Lift DC-DC Converters: Graphical Analysis and Modelling

Miao Zhu† and Fang Lin Luo*

†Meiden Power Solutions Ltd., Singapore
*Nanyang Technological University, Singapore

ABSTRACT

Super-lift dc-dc converters are a series of advanced step-up dc-dc topologies that provide high voltage transfer gains by super-lift techniques. This paper presents a developed graphical modelling method for super-lift converters and gives a thorough analysis with a consideration of the effects caused by parasitic parameters and diodes' forward voltage drop. The general guidelines for constructing and deriving graphical models are provided for system analysis. By applying it to examples, the proposed method shows the advantages of high convenience and feasibility. Both the circuit simulation and experimental results are given to support the theoretical analysis.

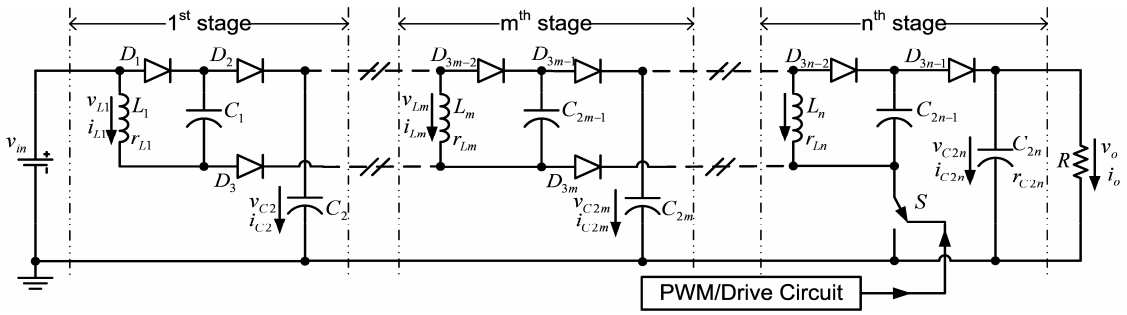
Keywords: DC-DC converter, Modelling, Super-lift, Flow graph

1. Introduction

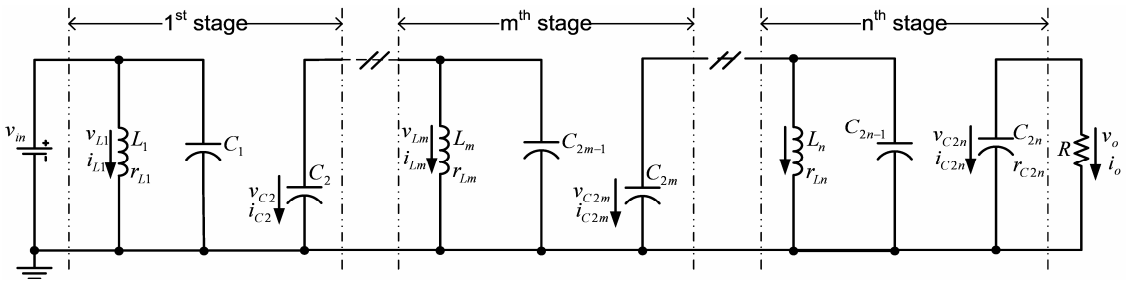
Advanced dc-dc converters with high voltage transfer gains are widely used in various industrial areas such as communication equipment, aerospace electronics and portable devices. Therefore, many new transformerless dc-dc topologies and dc voltage step-up theories have been reported in recent years, and their main aim is to improve the voltage boost ability in a simple structure[1-4]. The super-lift dc-dc converters[5] analyzed in this paper are a series of advanced step-up dc-dc power conversion topologies based on the super-lift (SL) technique.

Compared with conventional dc-dc converters, super-lift converters can implement the output voltages by increasing stage by stage along a geometric progression and obtain higher voltage transfer gains. They are divided into various categories according to their power stage numbers, such as the elementary circuit (single power stage), re-lift circuit (two power stages), triple-lift circuit (three power stages) etc. Assuming that there are n power stages connected in series for voltage lift, we get the generalized topology of the super-lift converters as shown in Fig. 1(a). The circuit has one switch S, n inductors, $2n$ capacitors, and ($3n-1$) diodes. Obviously, it is different from the topologies of conventional cascade boost converters due to their single-switch structures and operation principles. The number of power switches in the conventional cascade boost converters is n (n power stages). However, only one switch is required in this circuit. In addition, more diodes are involved in the process of network switching. When S turns on, D_1, D_3, D_4, $D_6 \ldots D_{3m-2}$, $D_{3m} \ldots D_{3n-2}$ are on, and D_2, $D_5 \ldots D_{3m-1} \ldots D_{3n-1}$ are off. When S turns off, D_1, D_3, D_4, $D_6 \ldots D_{3m-2}$, $D_{3m} \ldots D_{3n-2}$ are off, and D_2, $D_5 \ldots D_{3m-1} \ldots D_{3n-1}$ are on. The equivalent circuits during switching-on and –off are shown in Fig. 1(b) and (c), respectively.

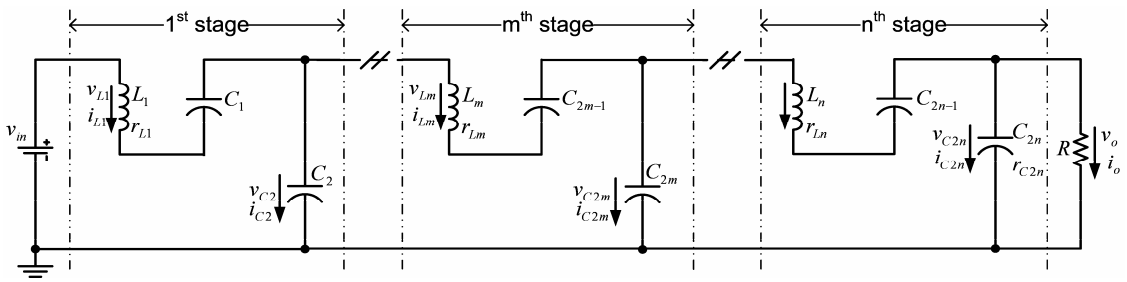
Manuscript received Dec. 4, 2008; revised Sept. 5, 2009
†Corresponding Author: zhumiao@pmail.ntu.edu.sg
Tel: +65-97911817, Meiden Power Solutions Ltd., Singapore
* Nanyang Technological University, Singapore



(a) Topology



(b) Equivalent circuit during switching-on (ideal condition)



(c) Equivalent circuit during switching-off (ideal condition)

Fig. 1. Generalized topology of the super-lift converter with *n* power stages.

For the m^{th} $(1 \le m \le n)$ power stage, during the switching-on of a given switching cycle T, inductor L_m and capacitor C_{2m-1} constitute a parallel-connected pump circuit (SL pump)[5] to absorb the energy from the capacitor C_{2m-2}. For the first power stage, the input source charges the pump circuit. During switching-off, L_m is in series with C_{2m-1}. The energy stored in the pump circuit is transferred to the capacitor C_{2m} and the next power stage. All capacitors with odd subscripts (C_{2m-1}) are termed the storage capacitor. All capacitors with even subscripts (C_{2m}) are termed support capacitors. As a series of new topologies, the super-lift converters presently lack theoretical analysis and modelling, and therefore an effective and generalized analytical method is required to perform the steady-state, large- and small-signal analysis for stimulating their industrial applications.

The analytical and modelling methods reported in recent decades mainly include the state-space averaging method, the average-switch method, the energy-based method and the graphical method[6-12]. Although all of these modelling methods have been discussed and applied to many cases, they are still rather tedious for circuit designers, especially when the converter circuit contains a large number of elements or many power stages. All of the above methods cannot model super-lift converters directly because they have not considered the SL technique

adopted in each SL pump circuit and the effects caused by the forward voltage drop of each diode. These two special problems increase the complexity of mathematical modelling significantly. Furthermore, both the steady and transient performances of super-lift converters are subject to the problems mentioned above.

This paper presents a developed switching signal flow graph (SFG) method for modelling super-lift converters. It describes the SL technique by reducing the circuit order in the SFG. The forward voltage drop of the diodes is also introduced into the model. General guidelines of drawing switching SFG for super-lift converters are given, from which a unified dynamic model is obtained. Derivation of the steady-state information and dynamic performance has been discussed. The re-lift circuit is taken as an example to demonstrate the application of the proposed method. Both the simulation and experimental results are provided to verify the analytical results.

2. Developed Switching SFG Method for Super-Lift Converters

The proposed method is a combination of conventional flow graph theory and the special characteristics of SL techniques. The following sections are carried out under the following assumptions:

a) The converter is working in continuous conduction mode (CCM). The power losses are described by the equivalent series resistance (ESR) of each inductor.
b) The ESR of the capacitors and stray capacitances are neglected except the output capacitor.
c) All capacitors are large enough that the ripple voltage across the capacitors can be negligible in one cycle for the average value discussion.
d) The switching actions of the switch are ideal.
e) All the forward voltage drop values of the diodes are the same and defined as V_D.
f) The filter corner frequency is much smaller than the switching frequency f_s.

For any given voltage or current parameter, the capital letter represents its average values, and the small letter represents its instantaneous values. The corresponding perturbations are represented by the small letters with a hat symbol. The directions of the voltages and currents are defined and shown in the corresponding figures.

2.1 Drawing switching SFG

According to the basic rules of switching SFG theory[10-12], two SFGs G_1 and G_2 are drawn from the operation of the converter, which correspond to switching-on and switching-off modes, respectively. Then these two sub-graphs are combined to form the following switching SFG:

$$G = kG_1 + \bar{k}G_2 \tag{1}$$

where k and $\bar{k}$ are switching functions as:

$$k = \begin{cases} 1 & 0 < t < dT \\ 0 & otherwise \end{cases} \qquad \bar{k} = 1 - k$$

Equation (1) introduces two basic switching branches, k branch and $\bar{k}$ branch[10]. The corresponding transmittance of the k branch is equal to the duty ratio d while the corresponding transmittance of the $\bar{k}$ branch is equal to (1-d), which is usually expressed by $\bar{d}$. The steady-state, large- and small-signal models can be obtained from G by a systematic procedure. It is noted that the transmittance labelled on the branch is a real gain or complex gain between two nodes. Such gains can be expressed in terms of the transfer function between two nodes.

For drawing the switching SFG of a super-lift converter with n power stages, the developed method presents the following general guidelines:

2.1.1 Guideline(1) for nodes configuration

Neglecting the definitions of the voltage and current nodes of each storage capacitor (C_1, $C_3 \ldots C_{2n-1}$) in the pump circuits, we define the sequence of the basic nodes, which are determined according to the sequence of the elements appearing in the circuit, inductor ($L_1, L_2 \ldots L_n$) or support capacitor (C_2, $C_4 \ldots C_{2n}$). Each inductor current node i_{Lm} is connected from its corresponding inductor voltage node v_{Lm}, and the transmittance takes into consideration the ESR of each inductor expressed by $1/(sL_m + rL_m)$. Each capacitor voltage node v_{C2m} is

connected from its corresponding capacitor current node i_{C2m}, and the transmittance is expressed by $1/(sC_{2m})$.

2.1.2 Guideline(2) for drawing switching-on SFG

The corresponding SFG for switching-on, G_1 is referred to in Fig. 2(a). For the switching-on mode shown in Fig. 1(b), the charging process of each capacitor in the pump circuit can be neglected. This is due to the above-mentioned assumption (c). Therefore, these storage capacitors, C_1, C_3,…,C_{2n-1}, are taken as voltage controlled voltage sources (VCCS) in the SFG, and the voltage values across them are defined as a series of voltage nodes. These nodes are determined directly by the input source node v_{in} and the corresponding voltage nodes of the support capacitors (C_2, C_4,…C_{2n-2}). Then the number of the capacitors considered in the SFG has been reduced by *50%*.

Then we can check the connection branches existing in the switching-on mode. Since the capacitor charging current in each pump circuit is neglected, this neglected current should be reconsidered when the current feedback loop from the node of i_{Lm} to the node $i_{C(2m-2)}$ is being constructed. The support capacitor C_{2m-2} charges L_m and C_{2m-1} simultaneously, so a transmittance labeled on the current feedback branch is added to reflect the summation of the charging currents i_{Lm} and $i_{C(2m-1)}$. For super-lift converters, we have $I_{C2(m-1)} = D^{-1} I_{Lm}$ in the steady state. As a result, the proposed transmittance is equal to $-d^{-1}$.

In addition, the effects caused by the forward voltage drop of the diodes are defined as a series of dc source voltage nodes. They are used to modify the practical voltage values of each passive element. For example, the voltage node $-(n-1)V_D$ is added and connected with the node v_{L1} because the total voltage drop caused by the diodes during the process of charging L_1 is equal to $(n-1)V_D$.

2.1.3 Guideline(3) for drawing switching-off SFG

The corresponding SFG for switching-off, G_2 is referred to in Fig. 2(b). For the switching-off mode shown in Fig. 1(c), the effects caused by the forward voltage drop of the diodes are defined as some additional source nodes. This is because that the different conduction paths in the switching-on and switching-off modes usually contain the different diodes. For example, a new voltage node, $-V_D$ is added and connected with the node v_{L1}, which has never been considered by conventional methods.

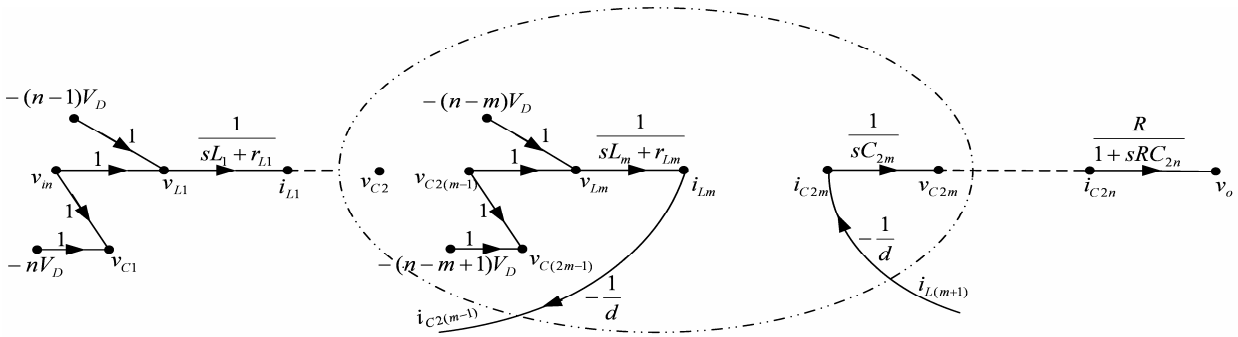
Then we can check the connection branches existing in the switching-off mode. The transmittance labeled on the current feedback branch is changed to -1 because L_m and C_{2m-1} are connected in series during switching-off. It means neglecting $i_{C(2m-1)}$ need not require any additional correction on the current feedback branch from the node of i_{Lm} to the node $i_{C(2m-2)}$.

2.1.4 Guideline(4) for drawing switching SFG

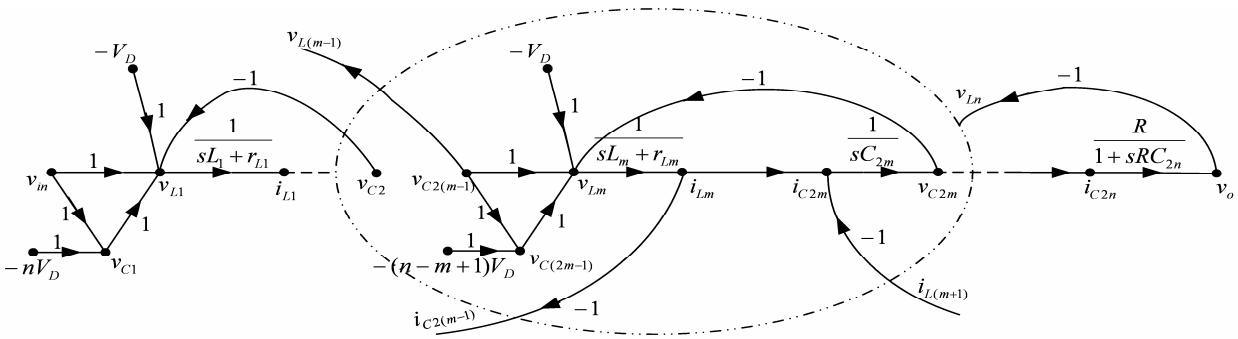
The unified switching SFG is drawn by merging G_1 and G_2 according to (1), which is referred to in Fig. 2(c). Many source nodes are added due to the modelling of the diodes. Then we can check and perform some primary predigestion such as branch moving or reducing the parallel braches which shares the same nodes. Two sorts of source nodes, v_{in} and $-V_D$ are distributed in different positions on the graph. Furthermore, it will result in several new switching branches which can be described by the generalized expressions, $(\alpha k + \beta)$ and $(\alpha \bar{k} + \beta)$. Here, α and β are two generalized and fixed parameters. α is produced by the predigestion of the diodes' voltage nodes and β is produced by the predigestion of sharing branches in the sub-graphs. They will be illustrated in Section 3. Because we have $(-d^{-1}) \times d + (-1) \times \bar{d} = -(1 + \bar{d})$, the transmittance labeled on the current feedback branch is merged to $-(1 + \bar{d})$.

2.1.5 Guideline(5) for graph analysis

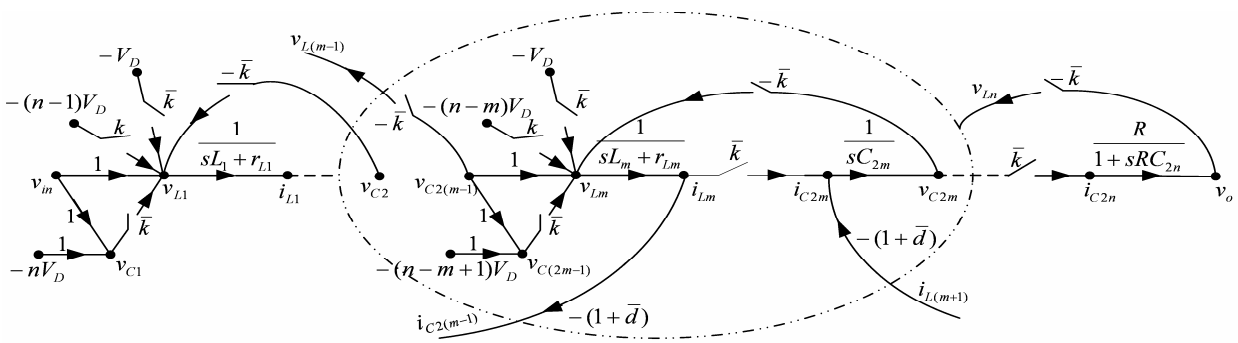
In the obtained switching SFG, the source nodes correspond to the source voltage and the voltage drop caused by the diodes. The mixed nodes correspond to the state variables. Each mixed node can be regarded as a sink node to perform a graph analysis when the relations between the variable and the source voltage are investigated. The main mathematical computational approaches are the graph reduction techniques, the Mason rules and the binary-tree analytical rules [10-12]. The main



(a) Switching-on



(b) Switching-off



(c) Unified switching SFG

Fig. 2. Unified switching SFG of the super-lift converter with *n* power stages.

computer simulation packages are TUTSIM and Matlab. The detailed graph analysis depends on the derivation of steady-state, large- and small-signal models from the switching SFG, which will be introduced in the following sections.

2.2 Derivation of large-signal models and steady-state information

The switching SFG can be utilized to derive a graphical representation of large-signal and steady-state models by substituting for the switching branches existing in the graph. Here, the switching branches in the switching SFG will be developed to the branches with the averaging transmittance. For super-lift converters, the averaging transmittance of their generalized switching branches are $(\alpha d + \beta)$ and $(\alpha \bar{d} + \beta)$ respectively. Hence, the corresponding large-signals carried through the switching branches can be expressed by:

$$y(s) = (\alpha d + \beta)x(s) \qquad \text{for } \alpha k + \beta \text{ branch} \qquad (2)$$

$$y(s) = [\alpha(1-d) + \beta]x(s) \qquad \text{for } \alpha\bar{k} + \beta \text{ branch} \qquad (3)$$

where x and y represent the input and output nodes (signals) of the switching branch.

The graphical representations of (2) and (3) are substituted for the switching branches in the switching SFG as shown in Fig. 2(c). Then, the graphical representation of the linear large-signal model in the s-domain is obtained directly.

It is convenient to obtain the steady-state model from the aforementioned large-signal model. In the graphical representation of the large-signal model, all the source nodes are assumed to be constant and all the mixed nodes (state variables) are fixed to their average values. In addition, all the transmittances labeled on the branches are simplified by setting $s \to 0$. Then a graphical representation of the steady-state model is obtained, which is used to derive the steady-state information.

2.3 Derivation of small-signal models

From the large-signal expressions (2) and (3) presented in the previous section, the corresponding small-signal expressions for the generalized switching branches can be derived. It is assumed that there exist small perturbations $\hat{x}(t)$, $\hat{d}(t)$ and $\hat{y}(t)$ near the operating points X, D and Y, i.e.

$$d(t) = D + \hat{d}(t) \qquad (4)$$

$$x(t) = X + \hat{x}(t) \qquad (5)$$

$$y(t) = Y + \hat{y}(t) \qquad (6)$$

The time domain expression of (2) and (3) are:

$$y(t) = (\alpha d + \beta)x(t) \qquad \text{for } \alpha k + \beta \text{ branch} \qquad (7)$$

$$y(t) = [\alpha(1-d) + \beta]x(t) \qquad \text{for } \alpha\bar{k} + \beta \text{ branch} \qquad (8)$$

By substituting (4), (5), and (6) into (7) and (8), we get the following equations:

$$Y + \hat{y}(t) = (X + \hat{x}(t))[\alpha(D + \hat{d}(t)) + \beta] \qquad (9)$$

$$Y + \hat{y}(t) = (X + \hat{x}(t))[\alpha(1 - D - \hat{d}(t)) + \beta] \qquad (10)$$

By neglecting the second-order perturbations and performing a Laplace transformation, we get the corresponding small-signals carried through the switching branches expressed by:

$$\hat{y}(s) = \alpha X\hat{d}(s) + (\alpha D + \beta)\hat{x}(s) \qquad \text{for } k + \lambda \text{ branch} \qquad (11)$$

$$\hat{y}(s) = -\alpha X\hat{d}(s) + [\alpha(1-D) + \beta]\hat{x}(s) \text{ for } \bar{k} + \lambda \text{ branch} \qquad (12)$$

The graphical representations of (11) and (12) are substituted for the switching branches in the switching SFG, and consequently, the representation of the small-signal model in the s-domain can be obtained.

2.4 Summary of the proposed method

From the foregoing introduction, the main characteristics of the proposed method are summarized.

1) This method is proposed to solve the problems associated with the modelling of SL techniques adopted in advanced dc-dc topologies. It is noted that the transmittance labeled on the current nodes' branch should reflect the correct quantity relations between the inductor and capacitor currents.
2) The forward voltage drop of each diode is considered. Hence, several source nodes are introduced so as to increase the analytical precision, especially for the steady-state information.
3) The definition of transmittance labeled on the current feedback branch has taken into consideration the circuit characteristics of SL pump circuits.
4) The obtained graphical expressions of graphical models can be programmed into TUTSIM or Matlab to observe the dynamical behaviors conveniently. The analytical expressions for various relations among the circuit variables can also be derived easily.
5) Compared with other methods, the proposed method needs fewer mathematical calculations. General calculation rules (graph reduction techniques and the Mason rules) can be utilized for systemic analysis.

This method can be considered as a developed graphical representation of the state-space averaging technique, and

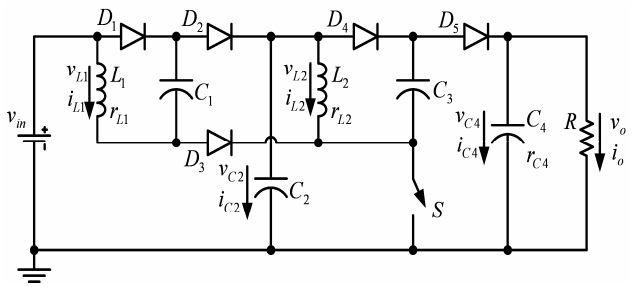


Fig. 3. Re-lift circuit of super-lift circuits.

the models derived from these two methods are equivalent. Since it is generally believed that state-space averaging models do not introduce significant error when f_s is sufficiently higher than the natural frequency of the converter, the proposed models can be expected to be accurate (up to about one third of the switching frequency).

3. Case Study: Re-lift Circuit

In this section, the proposed method will be applied to the re-lift circuit as shown in Fig. 3.

3.1 Steady-state and large-signal models

The switching SFG of the re-lift circuit is drawn from Fig. 2(c) and shown in Fig. 4(a). There are three close loops and five generalized switching branches in Fig. 4(a). We get the graphical expression of the large-signal model as shown in Fig. 4(b) according to the proposed method. There are three generalized switching branches in Fig. 4(b). One is $(\bar{k}+1)$, where the corresponding parameters $\alpha=\beta=1$. One is $(2\bar{k})$, where $\alpha=2$ and $\beta=0$. And one is $(2\bar{k}+1)$, where $\alpha=2$ and $\beta=1$. In addition, there is one source node v_{in} and two source nodes $-V_D$ ($-V_D/s$ is the expression in the s-domain) distributed in it. Therefore, the complicated calculation difficulties existing in the conventional methods are avoided through constructing the flow graph. For example, to get the steady-state information of V_o/V_{in}, assuming $s\to 0$ and using the Mason rules, we analyze the graph from three individual paths that start from different source nodes and end at the same mixed node. We have:

$$\frac{V_o}{V_{in}}=\frac{v_o(s)}{v_{in}(s)}\bigg|_{s\to 0}+\sum_{n=1}^{2}\left[\frac{v_o(s)}{-v_D(s)}\bigg|_{s\to 0}\times\left(-\frac{V_D}{V_{in}}\right)\right]_n \tag{13}$$

where n is the number of the node $-V_D$ in the large-signal model and it corresponds to the individual path.

The result of (13) is then obtained by the Mason rules, and is tabulated in Table 1 with the other main steady-state information. The ideal performance is also provided for reference. The corresponding analytical results of the elementary circuit are proved in the appendix (see Table 3).

Table 1. Steady-State Information of Re-lift Circuit.

$\frac{V_o}{V_{in}}$	$=\frac{(1+\bar{D})^2}{\Phi_R}-\theta\left[\frac{4\bar{D}^2+3\bar{D}+1}{\Phi_R}\right]\approx\left(\frac{1+\bar{D}}{\bar{D}}\right)^2$
$\frac{V_{C2}}{V_{in}}$	$=\frac{\bar{D}(1+\bar{D})\left(\frac{r_{L2}}{R\bar{D}^2}+1\right)}{\Phi_R}-\theta\left[\frac{\bar{D}(1+2\bar{D})+\frac{r_{L2}}{R}\frac{(1+2\bar{D})}{\bar{D}}-\frac{r_{L1}}{R}\frac{2(1+\bar{D})}{\bar{D}}}{\Phi_R}\right]$ $\approx\frac{1+\bar{D}}{\bar{D}}$
$\frac{I_{L2}}{V_{in}}$	$=\frac{(1+\bar{D})^2}{R\bar{D}\Phi_R}-\theta\left[\frac{4\bar{D}^2+3\bar{D}+1}{R\bar{D}\Phi_R}\right]\approx\frac{(1+\bar{D})^2}{\bar{D}^3R}$
$\frac{I_{L1}}{V_{in}}$	$=\frac{(1+\bar{D})^3}{R\bar{D}^2\Phi_R}-\theta\left[\frac{(1+\bar{D})(4\bar{D}^2+3\bar{D}+1)}{R\bar{D}^2\Phi_R}\right]\approx\frac{(1+\bar{D})^3}{\bar{D}^4R}$

where $\theta=\frac{V_D}{V_{in}}$ and $\Phi_R=\frac{r_{L2}}{R}+\frac{r_{L1}}{R}\left(\frac{1+\bar{D}}{\bar{D}}\right)^2+\bar{D}^2$.

Since D_3 and S have large current stresses, the averaging current of D_3 during switching-on, $I_{D3\text{-}on}$ is obtained for ready reference. We have:

$$\begin{aligned}I_{D3-on}&=I_{L1}\\&=\left\{\frac{(1+\bar{D})^3}{R\bar{D}^2\Phi_R}-\theta\left[\frac{(1+\bar{D})(4\bar{D}^2+3\bar{D}+1)}{R\bar{D}^2\Phi_R}\right]\right\}V_{in}\end{aligned} \tag{14}$$

The averaging current of S during switching-on, $I_{S\text{-}on}$ is obtained as:

$$\begin{aligned}I_{S-on}&=I_{L1}+I_{L2}\\&=\frac{1+2\bar{D}}{\bar{D}}\left\{\frac{(1+\bar{D})^2}{R\bar{D}\Phi_R}-\theta\left[\frac{4\bar{D}^2+3\bar{D}+1}{R\bar{D}\Phi_R}\right]\right\}V_{in}\end{aligned} \tag{15}$$

The detailed analytical procedure using the Mason rules to analyze the graph will be demonstrated in the following

section on deriving small-signal models.

3.2 Small-signal models

The graphical expression of the small-signal model is shown in Fig. 4(c), and it has two different sorts of source nodes. They include one node of $\hat{v}_{in}(s)$ and nine nodes of $\hat{d}(s)$ distributed in different positions. Unlike the large-signal SFG model as shown in Fig. 4(b), Fig. 4(c) considers the effects caused by the ESR of the output filter r_{C4} by changing the transmittance labelled on the branch $<\hat{i}_{C4}\ ,\ \hat{v}_o>$ from the previous $R/(1+sRC_4)$ to the current $R(1+sC_4r_{C4})/[1+sC_4(R+r_{C4})]$.

For example, the derivation of the input-to-output transfer function is demonstrated here. Neglecting all source nodes $\hat{d}(s)$ and the branches connected to them, we use the Mason rules to search the forward paths and the close loops. From the source node $\hat{v}_{in}$ to the mixed node $\hat{v}_o$, the forward path is searched and defined as P_1 ($<\hat{v}_{in}\ \hat{v}_{L1}\ \hat{i}_{L1}\ \hat{i}_{C2}\ \hat{v}_{C2}\ \hat{v}_{L2}\ \hat{i}_{L2}\ \hat{i}_{C4}\ \hat{v}_o>$). The transmittance of this forward path P_1 is obtained as:

$$P_1=\frac{(1+\overline{D})^2\overline{D}^2R(1+sr_{C4}C_4)}{[1+s(R+r_{C4})C_4](sL_1+r_{L1})(sL_2+r_{L2})sC_2}$$

There are three individual loops L_1 ($<\hat{v}_{L1}\ \hat{i}_{L1}\ \hat{i}_{C2}\ \hat{v}_{C2}\ \hat{v}_{L1}>$), L_2 ($<\hat{i}_{C2}\ \hat{v}_{C2}\ \hat{v}_{L2}\ \hat{i}_{L2}\ \hat{i}_{C2}>$) and L_3 ($<\hat{v}_{L2}\ \hat{i}_{L2}\ \hat{i}_{C4}\ \hat{v}_o\ \hat{v}_{L2}>$) in the graph. The corresponding loop transmittances are:

$$L_1=\frac{-\overline{D}^2}{(sL_1+r_{L1})sC_2},\qquad L_2=\frac{-(1+\overline{D})^2}{(sL_2+r_{L2})sC_2}$$

$$L_3=\frac{-\overline{D}^2R(1+sr_{C4}C_4)}{(sL_2+r_{L2})[1+s(R+r_{C4})C_4]}$$

Note that there are two non-touching loops (L_1 and L_3). Hence, the determinant Δ is equal to ($1-L_1-L_2-L_3+L_1L_3$). Since all three loops have a common branch, the cofactor of the defined forward path, Δ_1 is equal to 1. Therefore, the overall gain between $\hat{v}_o$ and $\hat{v}_{in}$, or the transfer function is given by:

$$\left.\frac{\hat{v}_o}{\hat{v}_{in}}\right|_{\hat{d}(s)=0}=\frac{1}{\Delta}\sum_k P_k\Delta_k=\frac{P_1\Delta_1}{\Delta} \tag{16}$$

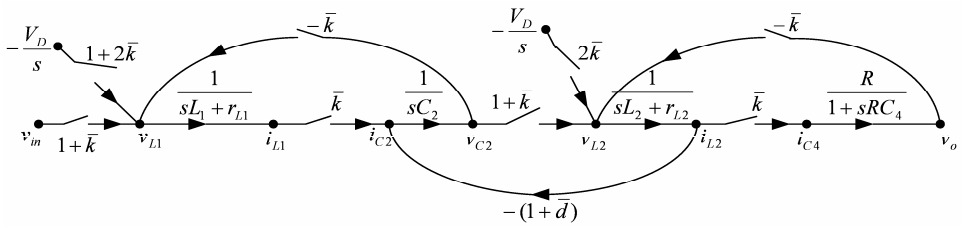
It is noted that the final result obtained from (16) does not reflect the effects caused by the diodes. This is because the transmittances labelled on the branches from the source node $\hat{v}_{in}(s)$ to any mixed node do not cover any information about V_D. Since the diodes will affect the practical steady-state performance significantly as referred to in Table 1, in the derivation of (16), we replace the ideal voltage transfer gain with the non-ideal voltage transfer gain as shown in Table 1 to modify the practical results.

Similarly, neglecting the source nodes $\hat{v}_{in}(s)$ and the branches connected to it, the analytical form of the control-to-output transfer functions ($\hat{v}_o/\hat{d}$, $\hat{i}_{L2}/\hat{d}$ and $\hat{i}_{L1}/\hat{d}$) can also be obtained. Because there are several source nodes $\hat{d}(s)$ in different positions, we can derive the relations between the output node and the different nodes $\hat{d}(s)$ respectively, and can sum them up to get the entire control-to-output transfer function. Furthermore, because the transmittances labelled on the branches from each node $\hat{d}(s)$ to the corresponding output node include information about V_D, the obtained control-to-output transfer functions reflect the effects caused by the diodes and need no further modification.

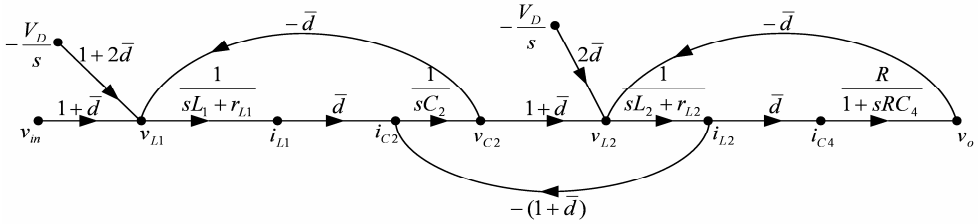
The detailed analytical forms of small-signal transfer functions of the re-lift circuit are tabulated in Table 2. The corresponding analytical results of the elementary circuit are proved in the appendix (see Table 4).

3.3 Simulation and experimental verification

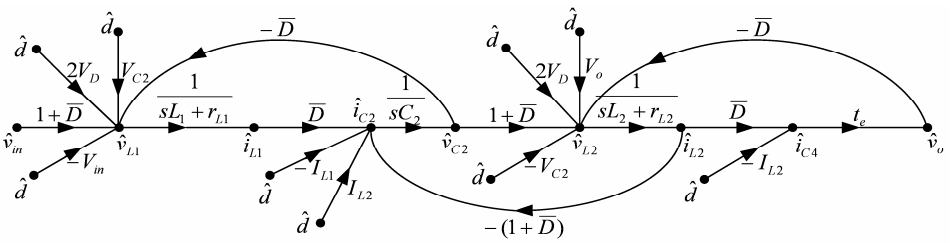
To illustrate a comprehensive application of the proposed method, the following design example is considered. Referring to Fig. 3, we choose the circuit parameters f_s=50kHz, d=0.5, L_1=L_2=500μH, C_1=C_2=C_3=220μF, C_4=50μF, R=10Ω and v_{in}=5V. There are some power losses, assuming that the ESR of the inductor r_{L1}=r_{L2}=0.1Ω and the forward voltage drop of the diodes V_D=0.85V. We get the steady-state performance by using the calculation equations in Table 1. The averaging load voltage is V_o=23.6V and the averaging inductor



(a) Switching SFG



(b) Large-signal model



(c) Small-signal model, where: $t_e = \dfrac{R(1+sC_4r_{C4})}{1+sC_4(R+r_{C4})}$

Fig. 4. Switching SFG of the re-lift circuit.

Table 2. Analytical Forms of Small-Signal Models of Re-lift Circuit.

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{M_p\overline{D}^4R(1+sr_{C4}C_4)}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\overline{D}^2+(sL_1+r_{L1})(1+\overline{D})^2]+\overline{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\overline{D}^2]}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{(1+\overline{D})[A_1+A_2(sL_1+r_{L1})]+A_3[\overline{D}^2+(sL_1+r_{L1})sC_2]-A_4[(sL_1+r_{L1})(sL_2+r_{L2})sC_2+(sL_2+r_{L2})\overline{D}^2+(sL_1+r_{L1})(1+\overline{D})^2]}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\overline{D}^2+(sL_1+r_{L1})(1+\overline{D})^2]+\overline{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\overline{D}^2]}$$

$$\frac{\hat{i}_{L2}(s)}{\hat{d}(s)} = \frac{A_5(1+\overline{D})\overline{D}+A_6(sL_1+r_{L1})+(A_7+A_4\overline{D})[\overline{D}^2+(sL_1+r_{L1})sC_2]}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\overline{D}^2+(sL_1+r_{L1})(1+\overline{D})^2]+\overline{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\overline{D}^2]}$$

$$\frac{\hat{i}_{L1}(s)}{\hat{d}(s)} = \frac{A_5(sL_2+r_{L2})[sC_2+(1+\overline{D})^2]+A_1sC_2-A_2\overline{D}^2-A_6\overline{D}(sL_2+r_{L2})+(A_7+A_4\overline{D})(1+\overline{D})\overline{D}}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\overline{D}^2+(sL_1+r_{L1})(1+\overline{D})^2]+\overline{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\overline{D}^2]}$$

Where:

$$M_p = \frac{(1+\overline{D})^2}{\Phi_R} - \theta\frac{4\overline{D}^2+3\overline{D}+1}{\Phi_R}\bigg|_{r_{L1}=r_{L2}=0} = (\frac{1+\overline{D}}{\overline{D}})^2 - \theta\frac{4\overline{D}^2+3\overline{D}+1}{\overline{D}^2},$$

$$\Delta_p = [1+s(R+r_{C4})C_4](sL_1+r_{L1})(sL_2+r_{L2})sC_2,$$

$$A_1 = (V_{C2}+2V_D-V_{in})\overline{D}^2R(1+sr_{C4}C_4), \qquad A_2 = (I_{L2}-I_{L1})\overline{D}R(1+sr_{C4}C_4)$$

$$A_3 = (V_o+2V_D-V_{C2})\overline{D}R(1+sr_{C4}C_4), \qquad A_4 = I_{L2}R(1+sr_{C4}C_4)$$

$$A_5 = (V_{C2}+2V_D-V_{in})[1+s(R+r_{C4})C_4], \qquad A_6 = (I_{L2}-I_{L1})[1+s(R+r_{C4})C_4]$$

$$A_7 = (V_o+2V_D-V_{C2})[1+s(R+r_{C4})C_4]$$

currents are $I_{L2}=4.7A$ and $I_{L1}=14A$.

The circuit is simulated in the PSIM with the above-mentioned parameters to verify the theoretical results. All parasitic parameters are included, and the simulation results are shown in Fig. 5. Both simulation and experimental results are in a good agreement with the theoretical results derived from the proposed method.

For an illustration of the transient performance, the theoretical large-signal SFG models described by Fig. 4 are programmed into the Matlab to observe the large-signal global behaviors. For the case where the input voltage is changed from *5V* to *8V* and back to *5V* after an interval, the simulation curve for the output voltage is shown in Fig. 6(a), from which it is seen that the model is close to an overdamped high order system. The experimental curve is provided in Fig. 6(b) to validate the simulation results. It is seen that the actual transient performance can be simulated by the proposed method exactly.

In Fig. 7, the new derived small-signal model is compared with the practical measured results. The measured points of the control-to-output frequency response at *D=0.5* are compared with the predictions of the derived model. Since the proposed small-signal model shown in Table 2 takes the parasitic parameters into account, the reduction of the practical dc gain is included. Therefore, as the figure shows, the derived model predicts almost exactly the same frequency response as the experiment up to one third of the switching frequency.

4. Conclusions

A developed switching SFG method is presented in this paper. This method is applied to the theoretical modelling and analysis of super-lift dc-dc converters, and successfully overcomes the complexity problems caused by the SL technique and the diode effects. The tedious circuit analysis is changed to a systematic process of construction and analysis on flow graphs. The general guidelines for drawing switching SFG and derivation of models are summarized. By the verification of simulation and experimental results, it is shown that the proposed method is an effective approach for super-lift converters. Furthermore, this method can be extended to all the other

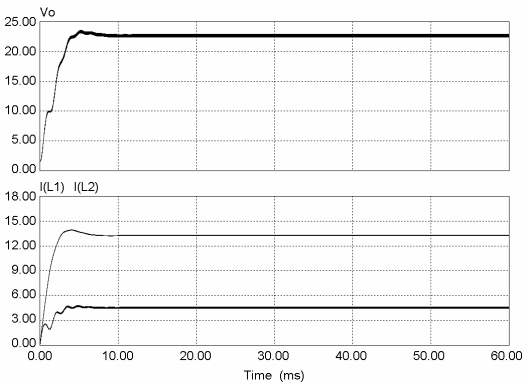
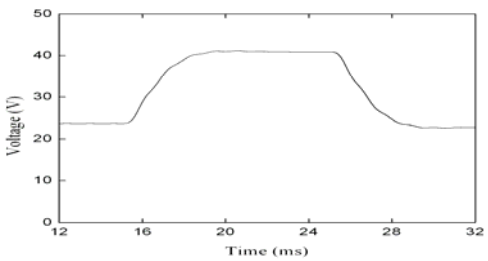
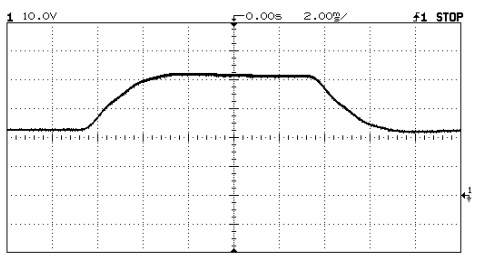


Fig. 5. The simulation results in PSIM: load voltage, inductor currents.



(a) Simulation curve obtained from proposed method



(b) Experimental curve

Fig. 6. Curves of the transient process.

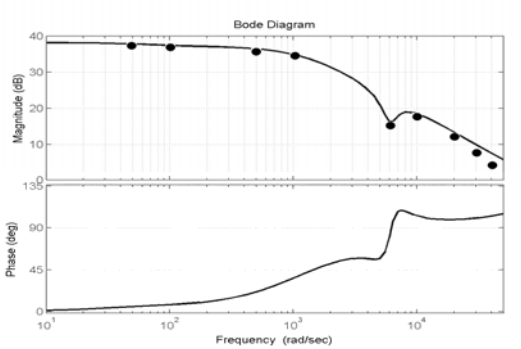


Fig. 7. Control-to-output frequency responses of the re-lift circuit predicted the proposed model (The dots represent the practical measured results).

dc-dc converters with the consideration of diodes and the SL technique.

Appendix

Table 3. Steady-state Information of Elementary Circuit.

$\frac{V_o}{V_{in}}$	$= \frac{1+\bar{D}}{\Phi_E} - \theta\frac{2\bar{D}}{\Phi_E} \approx \frac{1+\bar{D}}{\bar{D}}$
$\frac{I_L}{V_{in}}$	$= \frac{1+\bar{D}}{\bar{D}R\Phi_E} - \theta\frac{2}{R\Phi_E} \approx \frac{1+\bar{D}}{\bar{D}^2R}$

Where: $\theta = \frac{V_D}{V_{in}}$ and $\Phi_E = \frac{r_L}{R\bar{D}} + \bar{D}$

Table 4. Analytical Forms of Small-Signal Models of Elementary Circuit.

$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{M_p\bar{D}^2R(1+sr_{C2}C_2)}{(SL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2R(1+sr_{C2}C_2)}$
$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{(1+sr_{C2}C_2)[(V_o+2V_D-V_{in})\bar{D}R-I_LR(sL+r_L)]}{(sL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2R(1+sr_{C2}C_2)}$
$\frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{[1+s(R+r_{C2})C_2](V_o+2V_D-V_{in})+I_L\bar{D}R(1+sr_{C2}C_2)}{(sL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2R(1+sr_{C2}C_2)}$

References

[1] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits and Systems Magazine*, Vol. 1, No. 4, pp. 37-42, 2001.

[2] B. Axelrod, et. al., **"**Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc PWM converters," *IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications,* Vol. 55, No. 2, pp. 687-696, Mar. 2008.

[3] M. Zhu, et. al., "Series SEPIC implementing voltage lift technique for dc-dc power conversion," *IET Power Electronics*, Vol. 1, No. 1, pp. 109-121, Mar. 2008.

[4] M. Zhu, et. al., "Voltage-lift-type Cûk converters: topology and analysis," *IET Power Electronics*, Vol. 2, No. 2, pp. 178-191, Mar. 2009.

[5] F.L. Luo, et. al., "Positive output super-lift converters," *IEEE Trans. on Power Electronics*, Vol. 18, No. 1, pp. 105-113, Jan. 2003.

[6] J. Sun, et. al., "Averaged modelling of PWM converters operating in discontinuous conduction mode," *IEEE Trans. on Power Electronics*, Vol. 16, No. 4, pp. 482-492, Jul. 2001.

[7] V. Vorperian, "Simplified analysis of PWM converter using model of PWM switch, Part I: continuous conduction mode," *IEEE Trans. on Aerospace and Electronics Systems*, Vol. 26, No. 3, pp. 490-496, 1990.

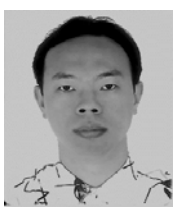
[8] K.C. Tam, et. al., "A wavelet-based piecewise approach for steady state analysis of power electronics circuits," *International Journal of Circuit Theory and Applications,* Vol. 34, No. 5, pp. 559-582, Sept. 2006.

[9] M. Zhu**,** et. al., "Transient analysis of multi-state dc-dc converters using system energy characteristics," *International Journal of Circuit Theory and Applications,* Vol. 36, No. 3, pp.327-344, May 2008.

[10] K.M. Smedley, et. al., "Switching flow-graph nonlinear modeling technique," *IEEE Trans. on Power Electronics*, Vol. 9, No. 4, pp. 405-413, Jul. 1994.

[11] M. Veerachary, "Signal flow graph modelling of multi-state boost dc-dc converters," *IEE Proc. Electr. Power Appl.*, Vol. 151, No. 5, pp. 583–589, Sept. 2004.

[12] M. Zhu, et. al., "Graphical analytical method for power dc/dc converters: averaging binary tree structure representation," *IEEE Trans. on Power Electronics*, Vol. 22, No. 2, pp. 701-705, Mar. 2007.



Miao Zhu received the B.Sc. degree in Electrical Engineering from Southeast University, China, in 2001. He finished his Ph.D. studies in 2008, and received the Ph.D. degree from Nanyang Technological University, Singapore, in 2009, with the thesis title of "Advanced DC-DC Power Conversion Topologies and Mathematical Analytical Methods". During 2001–2002, he was an Assistant Engineer at Wuxi Power Supply Company, National Power Grid of China. Since 2008, he has been with Meiden Power Solution Ltd, Singapore, as a research engineer. He is a regular reviewer for a number of academic journals, and has published nearly 20 papers in various international journals and conferences. His present research areas include power converters, power quality and renewable energy systems.

Fang Lin Luo received the B.Sc. degree from Sichuan University, China, and the Ph.D. degree from Cambridge University, U.K., in 1986. He was with the Chinese Automation Research Institute of Metallurgy (CARIM), China, as a Senior Engineer after his graduation from Sichuan University. He was with the Entreprises Saunier Duval, Paris, France, as a Project Engineer from 1981 to 1982. He was with Hocking NDT,

Ltd., Allen-Bradley IAP, Ltd. and Simplatroll, Ltd., U.K. as a Senior Engineer. Now, he is with Nanyang Technological University, Singapore. He has published eight academic books and more than 240 papers in various journals and conferences. His present research interests are motor drives and power converters. He was the General Chairman of the IEEE ICIEA'06 and ICIEA'08. Currently, he is an Associate Editor for the *Journal of Power Electronics*, the *IEEE Trans. on Power Electronics* and the *IEEE Trans. on Industrial Electronics*.