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A Single-Stage AC/DC Converter with Low Voltage Stresses and Reduced Switching Losses

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ABSTRACT

This paper proposes a high-efficiency single-stage ac/dc converter. The proposed converter features low voltage stresses and reduced switching losses. It operates at the boundary of discontinuous- and continuous-conduction modes by employing variable switching frequency control. The turn-on switching loss of the switch can be reduced by turning it on when the voltage across it is at a minimum. The voltage across the bulk capacitor is independent of the output loads and maintained within the practical range for the universal line input, so the problem of high voltage stress across the bulk capacitor is alleviated. Moreover, the voltage stress of the output diodes is clamped to the output voltage, and the output diodes are turned off at zero-current. Thus, the reverse-recovery related losses of the output diodes are eliminated. The operational principles and circuit analysis are presented. A prototype circuit was built and tested for a 150 W (50 V / 3 A) output power. The experimental results verify the performance of the proposed converter.

Keywords: Single-stage, Power factor correction (PFC), Variable frequency, Reverse-recovery, Power efficiency

1. Introduction

Recently, power factor correction (PFC) techniques have gained much attention in low-power off-line power supply development due to the requirements imposed by the European standard IEC 61000-3-2[1-3]. Two-stage converters exhibit good performances in high power factor and tight output voltage regulation. They have a front-end PFC stage[4-6] and a downstream dc/dc conversion stage [7-9]. The front-end PFC stage is used to achieve a unity power factor and low total harmonic distortion. The boost stage roughly regulates the bulk capacitor voltage at around 380 V to 400 V for the universal line input. The downstream dc/dc converter is used to realize output regulation with galvanic isolation and a fast dynamic response. Since the bulk capacitor voltage is nearly constant, dc/dc converter design can be easily optimized, and the size of the bulk capacitor minimized. However, this two-stage conversion approach results in extra costs and raises circuit complexity[10]. In low-power applications, for which cost is the dominant issue, such an approach loses its appeal.

To overcome these drawbacks, single-stage approaches have been investigated in recent literature[11-27]. By integrating two power conversion stages into one, single-stage single-switch ac/dc converters reduce the component count and cost. Therefore, they have gained much

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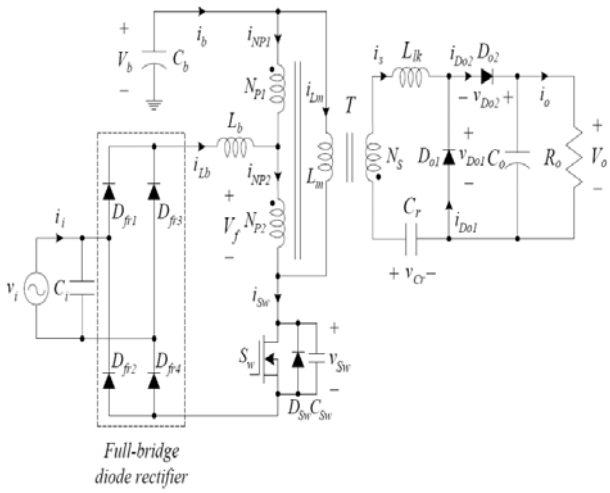
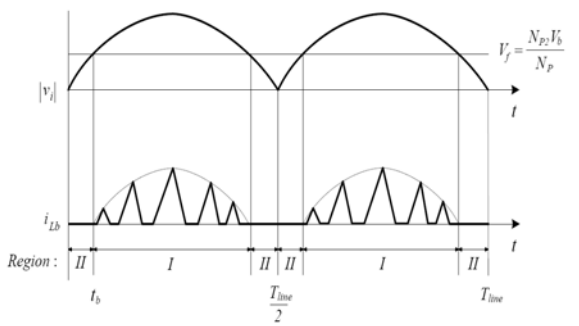


(a)



(b)

Fig. 1. Proposed single-stage converter. (a) Circuit diagram. (b) Operation regions.

attention in low-power industrial applications. Single-stage approaches are a cost-effective method for applications with power levels lower than 200 W when the bulk capacitor voltage is well controlled below 450 V for the universal line input. Thus, bulk capacitor voltage feedback using a coupled winding structure has been investigated to reduce bulk capacitor voltage within the practical range[15-17]. However, if the PFC cell operates in the discontinuous- conduction mode (DCM) and the dc/dc conversion cell operates in the continuous- conduction mode (CCM), a serious problem of high voltage stress across the bulk capacitor occurs at light loads. This is caused by an unbalanced power flow between the input source and the output load[22]. Some researchers have proposed effective methods to avoid high voltage stress across the bulk capacitor at light loads[23-26]. They suggest that both the PFC cell and the dc/dc conversion cell must operate in the DCM. If the loads become light, the input power decreases as the duty cycle decreases. Since no unbalanced power exists between the input source and the output load, bulk capacitor voltage is independent of load variations. However, DCM operation of the dc/dc conversion cell causes increased conduction losses as the output loads increase. Moreover, since previous single-stage single-switch converters employ conventional flyback[22, 23] or forward converter topologies[24, 25], higher-rated semiconductors should be used for the output diodes due to high voltage stress.

This paper proposes a high-efficiency single-stage ac/dc converter. The proposed converter features low voltage stresses and reduced switching losses. It operates at the boundary of DCM and CCM to overcome the drawback of high conduction loss. The switch is controlled by the variable switching frequency method[28]. The turn-on switching loss of the switch is reduced by turning on the switch when its voltage is at a minimum. Bulk capacitor voltage feedback is realized by using a tapped transformer. Bulk capacitor voltage is maintained in the practical range for the universal line input and it is shown to be independent of the output load. The voltage stress of the output diodes is clamped to the output voltage, and the output diodes are also turned off at zero-current. Thus, the reverse-recovery related losses of the output diodes are eliminated. The operational principles and circuit analysis are presented. The proposed converter is validated by building and testing a 150 W (50 V / 3 A) prototype circuit.

2. Operational Principle and Circuit Analysis

Fig. 1(a) shows a circuit diagram for the proposed converter. The basic circuit configuration on the primary side includes the line input voltage v_i, an input filtering capacitor C_i, four fast-recovery diodes $D_{fr1} \sim D_{fr4}$, a boost inductor L_b, a tapped transformer T, a bulk capacitor C_b, and a switch S_w. The diodes $D_{fr1} \sim D_{fr4}$ constitute a full-bridge diode rectifier. The switch S_w is ideal, except for the output capacitor C_{Sw} and the internal diode D_{Sw}.

The tapped transformer T is utilized to limit the bulk

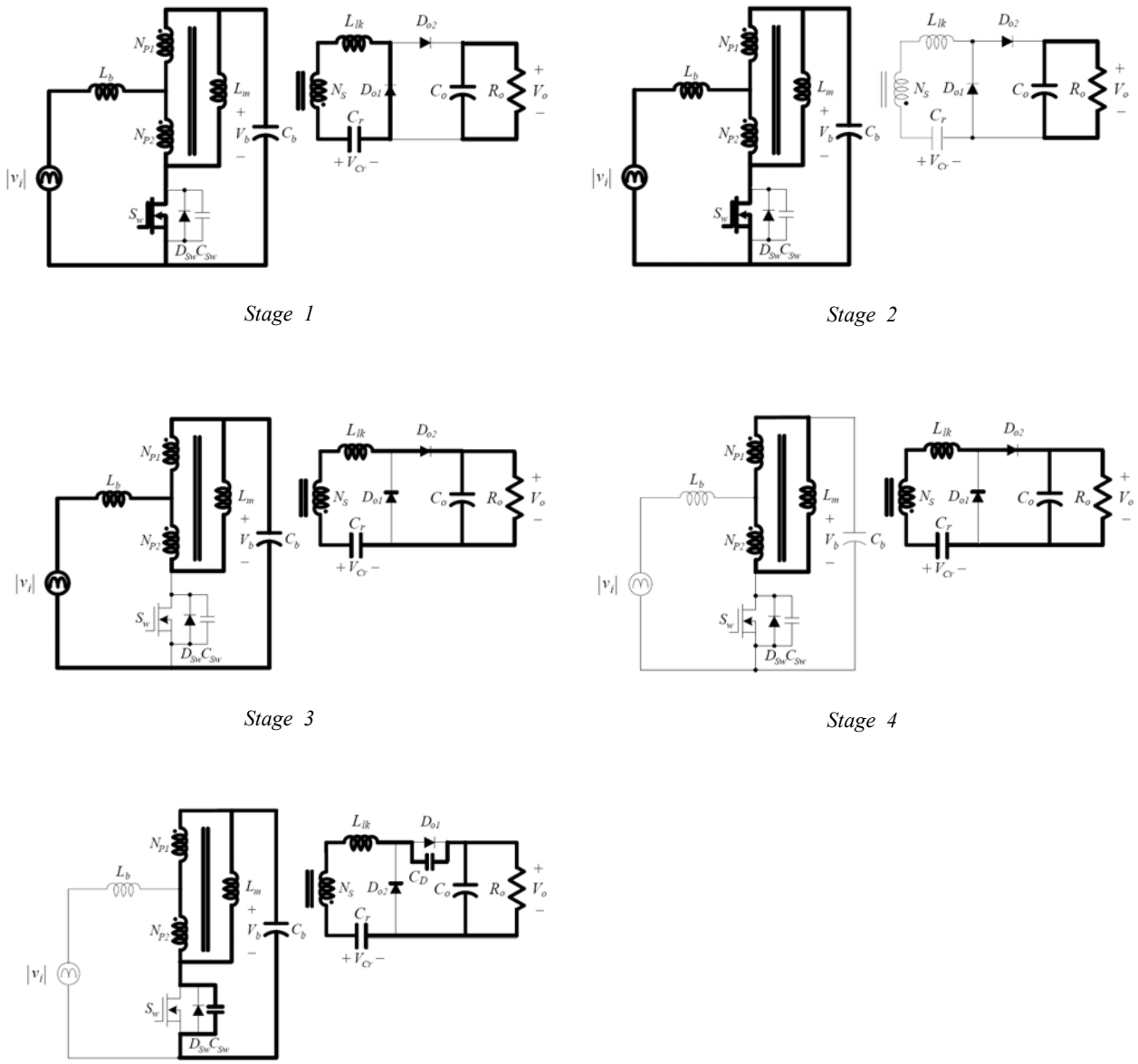


Fig. 2. Operational stages of the proposed converter.

capacitor voltage V_b. It is modeled on an ideal transformer which has a magnetizing inductor L_m and a leakage inductor L_{lk}. The turns ratio n of T is defined as $n = N_S/N_P$ where $N_P = N_{P1} + N_{P2}$. The bulk capacitor voltage feedback value V_f is given by:

$$V_f = \frac{N_{P2}}{N_P} V_b \tag{1}$$

The circuit configuration on the secondary side includes the leakage inductor L_{lk}, a resonant capacitor C_r, two output diodes D_{o1} and D_{o2}, and an output capacitor C_o. R_o is the output resistance. The capacitors C_b, C_r, C_o are large enough so that the voltages V_b, V_{Cr}, and V_o are constant during one switching period T_s.

The proposed converter has two operation regions, as

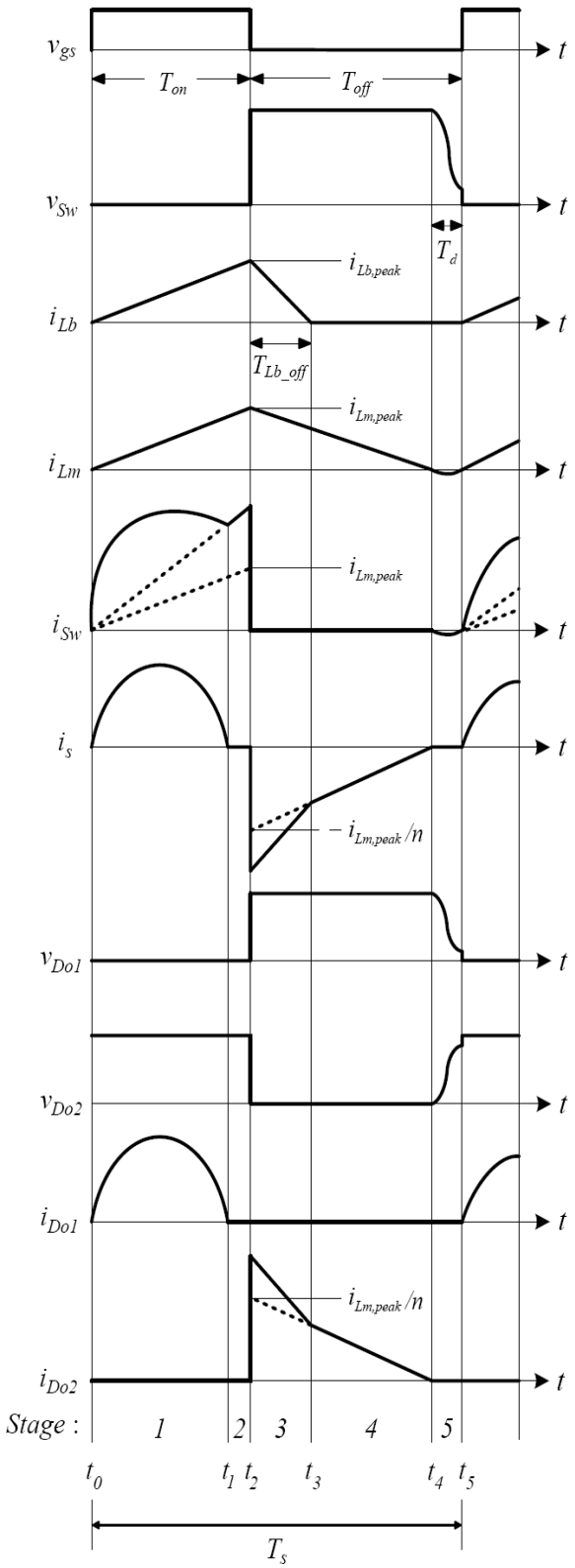


Fig. 3. Theoretical waveforms of the proposed converter. during one switching period T_s.

shown in Fig. 1(b). The line input voltage v_i is given by $\sqrt{2}\,V_i \sin\omega t$. V_i is the root-mean-squared value. ω is the angular line frequency where $\omega = 2\pi / T_{line}$. T_{line} is one period of the line input voltage. $|v_i|$ is the rectified line input voltage. When $|v_i|$ is higher than V_f, the converter works in *Region I*. When $|v_i|$ is lower than V_f, the converter works in *Region II*. Only the operation principle in *Region I* is described in this section. A description of the operation principle in *Region II* can be analogously inferred and will not be discussed here. Figs. 2 and 3 show the operational stages and theoretical waveforms of the proposed converter during T_s. The boost inductor current i_{Lb} is assumed to be discontinuous. Since the proposed converter operates at the boundary of DCM and CCM, the currents i_{Lb}, i_{Lm}, i_{Sw}, and i_s are zero before S_w is turned on.

Stage 1 [t_0, t_1]: At $t = t_0$, S_w is turned on. The magnetizing inductor current i_{Lm} increases linearly as:

$$i_{Lm}(t) = i_b(t) + \frac{N_{P2}}{N_P} i_{Lb}(t) = \frac{V_b}{L_m}(t - t_0) \tag{2}$$

The boost inductor current i_{Lb} is expressed as:

$$i_{Lb}(t) = \frac{(|v_i| - V_f)}{L_b}(t - t_0) \tag{3}$$

The energy from these two sources is stored in the magnetic field of the transformer. A part of the magnetizing energy is supplied from the bulk capacitor, while a part of the energy is supplied directly from the line. On the secondary side, a current path including L_{lk}, D_{o1}, C_r, and the secondary winding of T is formed. The input power is transferred to the capacitor C_r in a resonant manner. The secondary current i_s flows as:

$$i_s(t) = i_{Do1}(t) = \frac{V_{Cr} + nV_b}{Z_{r1}} \sin\omega_{r1}(t - t_0) \tag{4}$$

where the impedance Z_{r1} and angular frequency ω_{r1} of this resonance are given by:

$$Z_{r1} = \sqrt{\frac{L_{lk}}{C_r}} \tag{5}$$

$$\omega_{r1} = \frac{1}{\sqrt{L_{lk} C_r}} \tag{6}$$

Due to the magnetic coupling between N_{P1} and N_{P2}, the currents i_{NP1} and i_{NP2} are expressed as:

$$i_{NP1}(t) = -\frac{N_{P2}}{N_P} i_{Lb}(t) + \frac{N_S}{N_P} i_s(t) \tag{7}$$

$$i_{NP2}(t) = \frac{N_{P1}}{N_P} i_{Lb}(t) + \frac{N_S}{N_P} i_s(t) \tag{8}$$

The switch current i_{Sw} increases linearly as:

$$\begin{aligned} i_{Sw}(t) &= i_{Lm}(t) + i_{NP2}(t) \\ &= \frac{V_b}{L_m}(t - t_0) + \frac{N_{P1}(|v_i| - V_f)}{N_P L_b}(t - t_0) + \frac{N_S}{N_P} i_s(t) \end{aligned} \tag{9}$$

Stage 2 [t_1, t_2]: At $t = t_1$, the series-resonance between L_{lk} and C_r is terminated. Since the diode current i_{Do1} is zero, the output diode D_{o1} can be turned off at zero-current. Zero-current turn-off of the diode D_{o1} removes its reverse-recovery problem. Since the secondary current i_s is zero, the switch current i_{Sw} is the sum of the currents i_{Lb} and i_{Lm}.

Stage 3 [t_2, t_3]: At $t = t_2$, S_w is turned off. Since the output capacitor C_{Sw} of S_w has a small value, C_w charges immediately. D_{o2} enters a conduction state. A current path including L_{lk}, D_{o2}, C_o, C_r, and the secondary winding of T is formed. The energy stored in the capacitor C_r is transferred to the output load. Since the reverse-voltage across D_{o1} is V_o, the voltage across the secondary winding of T is $V_o - V_{Cr}$. The magnetizing inductor current i_{Lm} decreases linearly as:

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{V_o - V_{Cr}}{n L_m}(t - t_2) \tag{10}$$

The boost inductor current i_{Lb} decreases linearly as:

$$i_{Lb}(t) = i_{Lb}(t_1) - \frac{V_b + N_{P1} V_{Cr} / N_S - |v_i|}{L_b}(t - t_1) \tag{11}$$

Due to the magnetic coupling between N_{P1} and N_S, the secondary current i_s flows as:

$$i_s(t) = \frac{i_{Lm}(t)}{n} + \frac{N_{P1} i_{Lb}(t)}{N_S} \tag{12}$$

The output power is supplied from two different sources. The energy associated with the magnetizing current i_{Lm} is obtained from the energy stored in L_m, while the energy associated with the boost inductor current i_{Lb} is drawn directly from the line.

Stage 4 [t_3, t_4]: At $t = t_3$, the boost inductor current i_{Lb} is zero. Since the output power is supplied only from L_m, the secondary current i_s flows through the output diode D_{o2} as $i_s(t) = i_{Lm}(t) / n$.

Stage 5 [t_4, t_5]: At $t = t_4$, the energy stored in L_m is completely discharged, and the secondary current i_s is zero. Since the diode current i_{Do2} is zero, the output diode D_{o2} can be turned off at zero-current. Zero-current turn-off of the diode D_{o2} removes its reverse-recovery problem. The magnetizing inductor L_m and the equivalent capacitor $C_{eq} = C_{Sw} + C_D / n^2$ begin to resonate as:

$$i_{Lm}(t) = \frac{V_b - v_{Sw}(t_4)}{Z_{r2}} \sin \omega_{r2}(t - t_4) \tag{13}$$

$$v_{Sw}(t) = V_b + \frac{V_{Cr}}{n} \cos \omega_{r2}(t - t_3) \tag{14}$$

where the impedance Z_{r2} and angular frequency ω_{r2} of this resonance are given by:

$$Z_{r2} = \sqrt{\frac{L_m}{C_{eq}}} \tag{15}$$

$$\omega_{r2} = \frac{1}{\sqrt{L_m C_{eq}}} \tag{16}$$

The capacitor C_D is the equivalent parasitic capacitor of the output diodes D_{o1} and D_{o2}. This mode is terminated after the half-resonant period $T_d = \pi / \omega_{r2}$. Since the capacitors C_{Sw} and C_D are very small, this half-resonant period will be very short. The switch S_w is turned on when its voltage is $V_b - V_{Cr} / n$. Thus, the switch voltage reaches its minimum value and its switching loss can be reduced. If the switch voltage v_{Sw} decreases to zero, the switch S_w can be turned on at the zero-voltage condition and its turn-on switching loss can be eliminated.

Since the proposed converter operates at the boundary of DCM and CCM, the following relation can be obtained:

$$i_{Lm,peak} = \frac{V_b}{L_m} T_{on} = \frac{V_{Cr}}{nL_m} T_{off} \tag{17}$$

and the relation between the on-time T_{on} and the off-time T_{off} is:

$$\frac{T_{on}}{T_{off}} = \frac{m}{n} \tag{18}$$

where $m = V_{Cr}/V_b$. The volt-second balance on the magnetizing inductor L_m gives the following relation between the bulk capacitor voltage V_b and the resonant capacitor voltage V_{Cr}:

$$V_b T_{on} = \frac{nL_m V_{Cr}}{n^2 L_m + L_{lk}} \left(T_{off} - T_d \right) \tag{19}$$

The volt-second balance on the leakage inductor L_{lk} gives the following relation:

$$\left(nV_b - V_o + V_{Cr} \right) T_{on} + \frac{L_m V_{Cr}}{n^2 L_m + L_{lk}} = 0 \tag{20}$$

If the leakage inductor L_{lk} is much smaller than the reflected inductor $n^2 L_m$, and T_d is negligible compared to T_{on} and T_{off}, (19) and (20) can be simplified as:

$$V_{Cr} = \frac{nV_b T_{on}}{T_{off} - T_d} \cong \frac{nV_b T_{on}}{T_{off}} \tag{21}$$

$$V_o = nV_b + V_{Cr} \tag{22}$$

From (21) and (22), the relation between the output voltage V_o and the bulk capacitor voltage V_b is obtained as:

$$\frac{V_o}{V_b} = \frac{nT_s}{T_{off}} \tag{23}$$

From (21), (23), and the fact that $T_s = T_{on} + T_{off}$, V_{Cr} can be represented as:

$$V_{Cr} = V_o - nV_b \tag{24}$$

For zero-current turn-off of the output diode D_{o1}, the following condition should be satisfied:

$$2\pi \sqrt{L_{lk} C_r} < T_{on} \tag{25}$$

The switching period T_s is related to the output load. Since the switching period T_s decreases at light loads, zero-current turn-off of the output diode will not be achieved. However, at light loads, the reverse-recovery related loss is not significant since the amount of diode current i_{Do1} is small.

Since the boost inductor current i_{Lb} is discontinuous, the peak boost inductor current $i_{Lb,peak}$ can be expressed as:

$$i_{Lb,peak} = \frac{|v_i| - V_f}{L_b} T_{on} \tag{26}$$

The volt-second balance of the boost inductor L_b gives:

$$\left(|v_i| - V_f \right) T_{on} = \left(V_b + N_{P1} V_{Cr} / N_S - |v_i| \right) T_{Lb\_off} \tag{27}$$

The time duration of *Stage 3*, T_{Lb_off}, is expressed as:

$$T_{Lb\_off} = \frac{|v_i| - V_f}{V_b + N_{P1} V_{Cr} / N_S - |v_i|} T_{on} \tag{28}$$

The average boost inductor current $i_{Lb,avg}$ during T_s is:

$$i_{Lb,avg} = \frac{i_{Lb,peak}\left(T_{on} + T_{Lb\_off}\right)}{2T_s} \quad (29)$$

Using (24), (26), (28), and (29), the current $i_{Lb,avg}$ is expressed as:

$$i_{Lb,avg} = \left(\frac{V_{Cr}}{m+n}\right)\left(\frac{|v_i| - V_f}{2L_bV_b}\right)\left(\frac{V_b + N_{P1}V_{Cr}/N_S - V_f}{V_b + N_{P1}V_{Cr}/N_S - |v_i|}\right)T_{on} \quad (30)$$

The input energy E_{in} absorbed during a half line cycle is an integral of the product of line input voltage and average boost inductor current at the same time. Thus:

$$E_{in} = \int_{t_b}^{\frac{T_{line}}{2}-t_b} |v_i| i_{Lb,avg} dt \quad (31)$$

$$= \int_{t_b}^{\frac{T_{line}}{2}-t_b} |v_i| \left(\frac{V_{Cr}}{m+n}\right)\left(\frac{|v_i| - V_f}{2L_bV_b}\right)\left(\frac{V_b + N_{P1}V_{Cr}/N_S - V_f}{V_b + N_{P1}V_{Cr}/N_S - |v_i|}\right)T_{on} dt$$

The boundary time, t_b, is given by:

$$t_b = \frac{1}{\omega}\sin^{-1}\left(\frac{V_bN_{P2}}{\sqrt{2}V_iN_P}\right) \quad (32)$$

Since the average output current $i_{o,avg}$ is the average value of the output diode current i_{Do},

$$i_{o,avg} = \frac{ni_{Lm,peak}}{2T_s}T_{off} + \frac{N_{P1}i_{Lb,peak}}{2N_ST_s}T_{Lb\_off} \quad (33)$$

Using (17), (24), (26), (28), and (33), the current $i_{o,avg}$ is expressed as:

$$i_{o,avg} = \left[\frac{n^2V_b}{L_m} + \frac{N_{P1}V_{Cr}\left(|v_i| - V_f\right)^2}{N_SL_bV_b\left(V_b + N_{P1}V_{Cr}/N_S - |v_i|\right)}\right]\frac{T_{on}}{2(m+n)} \quad (34)$$

The output energy E_{out} during a half line cycle is given by:

$$E_{out} = \frac{V_oi_{o,avg}T_{line}}{2}$$

$$= \frac{V_oT_{on}T_{line}}{4(m+n)}\left[\frac{n^2V_b}{L_m} + \frac{N_{P1}V_{Cr}\left(|v_i| - V_f\right)^2}{N_SL_bV_b\left(V_b + N_{P1}V_{Cr}/N_S - |v_i|\right)}\right] \quad (35)$$

During a half line cycle, the input energy E_{in} is equal to the output energy E_{out} at steady state. Thus, the input-output energy balance gives:

$$\frac{2}{T_{line}}\int_{t_b}^{\frac{T_{line}}{2}-t_b} |v_i| \left(\frac{|v_i| - V_f}{V_b}\right)\left(\frac{V_b + N_{P1}V_{Cr}/N_S - V_f}{V_b + N_{P1}V_{Cr}/N_S - |v_i|}\right)dt =$$

$$= \frac{n^2L_bV_b}{L_mV_{Cr}} + \frac{N_{P1}\left(|v_i| - V_f\right)^2}{N_SV_b\left(V_b + N_{P1}V_{Cr}/N_S - |v_i|\right)} \quad (36)$$

where $V_{Cr} = V_o - nV_b$. Equation (36) shows that the bulk capacitor voltage V_b is independent of the output load. V_b is determined by the input voltage, the output voltage, and the circuit parameters of n, N_{P1} / N_S, and L_b / L_m. Since the output load has no impact on the bulk capacitor voltage, the bulk capacitor voltage V_b can be maintained at desirable levels with a proper design.

3. Experimental Results

The feasibility of the proposed converter was verified by building and testing a prototype circuit. The output voltage and maximum output power of the converter were specified as V_o = 50 V and $P_{o,max}$ = 150 W. The proposed converter operates at the boundary of DCM and CCM by detecting the demagnetization of T, as described in [19]. The switching frequency can be changed by employing a variable switching frequency control to detect the moment when the switch voltage v_{Sw} is at its minimum by the resonance between the magnetizing inductor L_m and the equivalent capacitor C_{eq}. The major components and parameters of the prototype circuit are presented in Table 1. A photograph of the implemented prototype is shown in Fig. 4.

Fig. 5 shows the measured input current and voltage for 150W of output power. The measured power factor was 0.91 with 92.4 % efficiency at 120 V_{rms} of input voltage and 0.87 with 92.5 % efficiency at 220 V_{rms} of input voltage. Fig. 6 shows the experimental waveforms of the

Table 1. Parameters and Components of the Prototype.

Parameter	Symbol	Value
Input voltage	V_i	90 ~ 265 V_{rms}
Output voltage	V_o	50 V
Switching frequency	f_s	40 ~120 kHz
Primary winding turns	N_{P1}, N_{P2}	20 turns, 20 turns
Secondary winding turns	N_S	6 turns
Magnetizing inductor	L_m	500 μH
Leakage inductor	L_{lk}	1.37 μH
Boost inductor	L_b	170 μH
Resonant capacitor	C_r	6.6 μF / 100V
Bulk capacitor	C_b	220 μF / 450V
Input filtering capacitor	C_i	220 nF / 630V
Output capacitor	C_o	680 μF / 63V
Component	**Symbol**	**Part name**
Primary switch	S_w	SPP11N50C3
Output diodes	D_{o1}, D_{o2}	MBR20100
Fast-recovery diodes	D_{fr1} ~ D_{fr4}	FR105

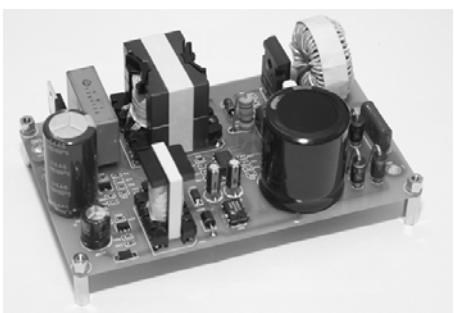
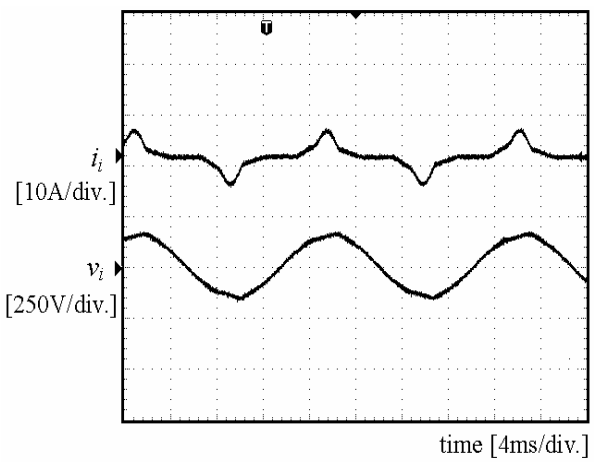


Fig. 4. Photograph of the implemented prototype circuit.

switch voltage v_{Sw}, the switch current i_{Sw}, and the secondary current i_s at 120 V_{rms} of input voltage. The switch S_w is turned on after half-resonance between the magnetizing inductor L_m and the equivalent capacitor C_{eq}, as shown in Fig. 6(a). Since the switch voltage v_{Sw} decreases to the minimum voltage before S_w is turned on, the switching loss is considerably reduced. Fig. 6(b) shows that the converter operates at the boundary of DCM and CCM. The diode current i_{Do1} is zero before switch S_w is turned on. The boost inductor current i_{Lb} is transferred to the secondary side during the turn-off period of the switch. Fig. 7 shows the experimental waveforms of the voltages v_{Do1} and v_{Do2} across the diodes D_{o1} and D_{o2} and the currents i_{Do1} and i_{Do2} at 120 V_{rms} of input voltage at full load. It can be seen that the diode voltages v_{Do1} and v_{Do2} are clamped to the output voltage V_o, and that each output diode can be turned off at zero-current. Thus, the diode reverse-recovery related losses are eliminated. The experimental waveforms of the voltages and currents



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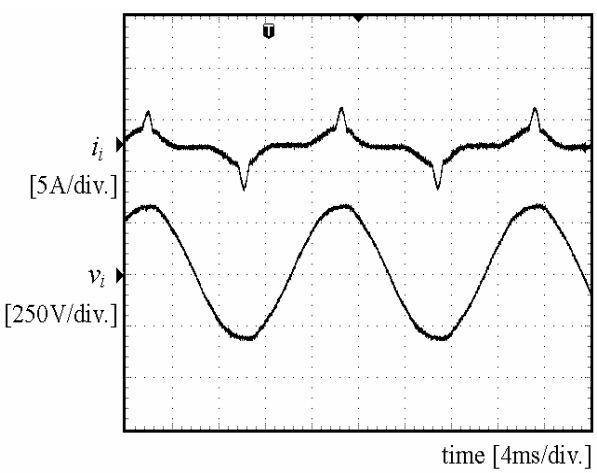
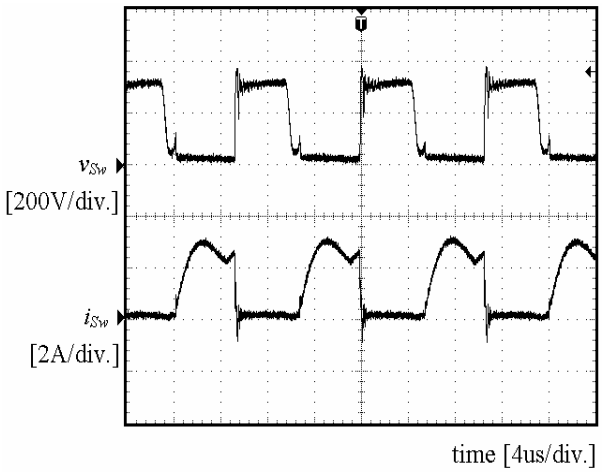


(b)

Fig. 5. Experimental waveforms of the input current i_i and input voltage v_i. (a) at 120 V_{rms} line voltage. (b) at 220 V_{rms} line voltage.



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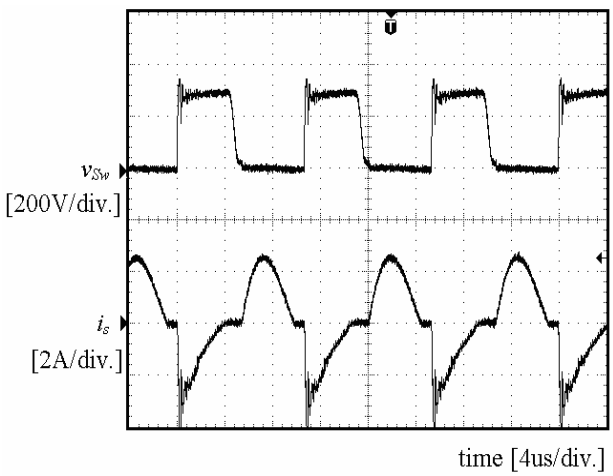
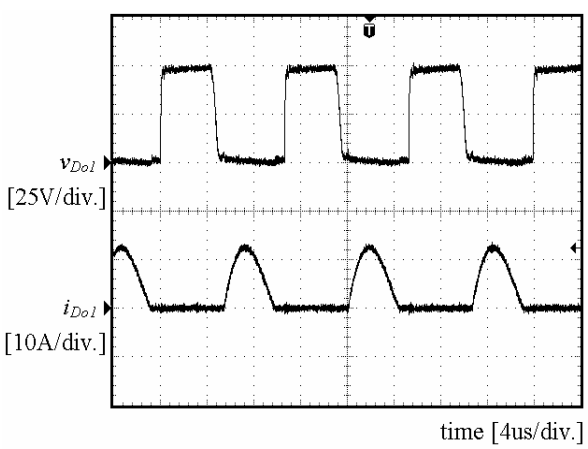


(b)

Fig. 6. Experimental waveforms of the switch voltage v_{Sw}, switch current i_{Sw}, and secondary current i_s. (a) Switch voltage v_{Sw} and switch current i_{Sw}, (b) Switch voltage v_{Sw} and secondary current i_s.



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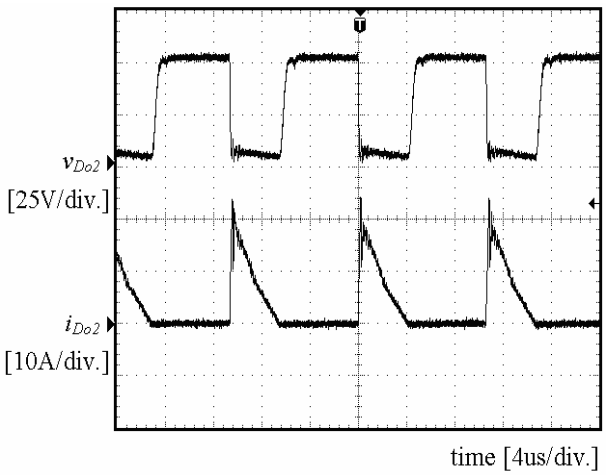

(b)

Fig. 7. Experimental waveforms of the diode voltages v_{Do1} and v_{Do2} and diode currents i_{Do1} and i_{Do2}. (a) Diode voltage v_{Do1} and current i_{Do1}. (b) Diode voltage v_{Do2} and current i_{Do2}.

Table 2. Measured power factor, bulk capacitor voltage, efficiency, and switching frequency range.

V_i	PF	V_b	Efficiency	f_s
90 V_{rms}	0.92	131 V	92.2 %	55 kHz
120 V_{rms}	0.91	175 V	92.4 %	77 kHz
150 V_{rms}	0.90	223 V	92.5 %	89 kHz
180 V_{rms}	0.88	262 V	92.7 %	95 kHz
220 V_{rms}	0.87	345 V	92.5 %	107 kHz
265 V_{rms}	0.85	387 V	92.3 %	113 kHz

agree with the theoretical waveforms in Fig. 2. Fig. 8 shows the experimental waveforms of the bulk capacitor voltage V_b, the output voltage V_o and the output current i_o at 120 V_{rms} of input voltage for the step variation of the output load current. These waveforms show that fast output voltage regulation is achieved and that the bulk capacitor voltage is constant for the step load variation.

Table 2 summarizes the measured full-load power factor (PF), bulk capacitor voltage V_b, efficiency, and the range of the switching frequency f_s. As can be seen from Table 2, the maximum bulk capacitor voltage is

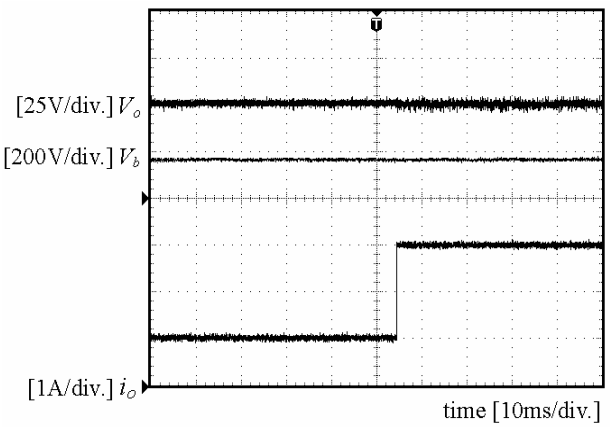

Fig. 8. Experimental waveforms of the output voltage V_o, bulk capacitor voltage V_b, and output current i_o for the step load change.

maintained well below 400 V. The minimum efficiency, which occurs at low line, is above 92 %.

4. Conclusions

This paper proposes a high-efficiency single-stage ac/dc converter with low voltage stresses and reduced switching losses. Variable frequency control reduces the turn-on switching loss of the primary switch by turning on the switch at its minimum voltage. The voltage stress of the output diodes is clamped to the output voltage. The output diodes are turned off at zero-current. Thus, the reverse-recovery related losses of the output diodes are eliminated. The bulk capacitor voltage was shown to be independent of the output loads. The bulk capacitor voltage was maintained at the practical range for universal line input. The power efficiency was measured to be over 92 % with a high power factor for universal line input.

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