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A Study on the Characteristics of Voltage Distribution of Stacked YBCO Coated Conductors in Series Connection

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Abstract-- **In order to apply superconducting electric machineries such as a Superconducting Fault Current Limiter (SFCL) to the power grid, the single module should be connected in series to have reasonable size. Superconducting tapes in the module also should be stacked to satisfy requirements such as large operation current of the power grid. This is because a single superconducting tape has restricted applicable current capacity. Moreover especially in SFCL at the fault, there should be equal voltage distribution in series-connected SFCL modules. In this paper, we investigated the voltage distribution in fault current of series-connected YBCO coated conductors (CC). Depending on characteristics of the CC samples such as critical current, even voltage distribution could be achieved or not. In addition, the effect of stacked CC on the change of voltage distribution comparing to non-stack cases in series connection was confirmed by experiments. As the CC stacked, voltage difference could be reduced.**

1. INTRODUCTION

At the present day, the power grid has enlarged its scale rapidly. However the bigger the electric power system becomes, the more serious problem the fault current has. Therefore fault current limiter which reduces the high fault current of the system is indispensable.

With development of the second generation wire, Coated Conductors (CC), a superconducting fault current limiter (SFCL) has been regarded as the powerful solution for limiting the fault current [1]. CCs are high temperature superconductor (HTS) material that can reduce operation costs because of using liquid nitrogen as a refrigerant. Moreover, the stabilizer of the CC has high resistance. This resistance of the stabilizer could not only limit large amount of the fault current at first peak but also reduce the fault current rapidly within a few cycles through bypassing superconductor's fault current to the stabilizer.

It would be too bulky for a single SFCL to withstand voltage of the power grid hence SFCLs should be connected in-series [2]. In addition, Stacks of CCs could increase amount of transport current [3]. However, the characteristics of CC are inhomogeneous along the wire. Therefore critical current of the CC cannot maintain uniformity as the wire becomes longer. In fault condition, this inhomogeneity induces uneven voltage distribution when the CC elements are connected in series [4, 5]. These unequal quench characteristics could make damage for inferior side in connection.

In this paper, we induced fault current to the series connected CC short samples. The experiment investigated that different critical currents of the samples affected voltage distribution. Furthermore, CCs were stacked on the samples to verify that they could change the voltage distribution of non-stacking CCs. Even in the case of ill-balanced voltage distribution because of different critical current value of samples, it was also confirmed that stack of CC could reduce the voltage difference.

2. EXPERIMENTAL DETAILS

2.1. HTS wire Short Samples

In this paper, the CC wire, "344S Superconductors (344S)", manufactured by AMSC® was used for experiments. This wire uses YBCO as the HTS material. Ni alloy is used for substrate. The stabilizer of this wire is stainless steel and this material has very high resistivity which is appropriate for limiting fault current effectively. Table I shows the specifications of the 344S.

In this paper, five CC samples were used. Except for a last sample, a sample 5, samples had similar critical current shown in Table II. 1μV/cm criterion was used to determine the critical current.

2.2. Series Connected Samples including Stack

The experiment consisted of two cases. The first case, Case I, was conducted with samples having similar critical current. The Case II was conducted with samples having

TABLE I
SPECIFICATIONS OF USED CC.

Spec	Sample
Manufacturer (model)	AMSC® (344S)
Width	4.4 mm
Total Thickness	0.150 mm
Substrate Thickness	0.075 mm
Stabilizer Thickness	0.05 mm

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TABLE II
SPECIFICATIONS OF EACH SAMPLE.

	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
I_c(A)	100	98	97	98	72
Voltage Tap Length(mm)	100	100	100	100	100

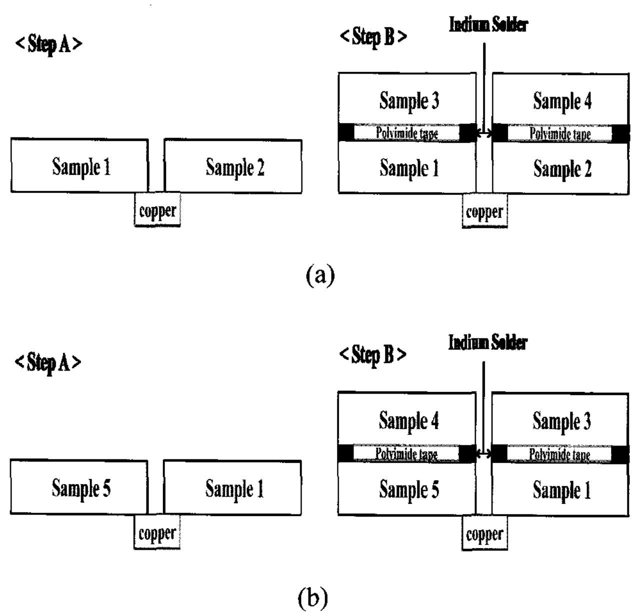

Fig. 1. Preparation of samples : (a) Case I, (b) Case II.

different critical current. Each case had two steps, A and B. In step A, two CC samples were connected in series by the copper plate as shown in Fig. 1. After step A, we stacked samples above samples of step A. Therefore, the stacked sample made parallel connection with previous sample of step A. After the stack, two pairs of stacked samples were connected in series by the copper plate just as in step A. This is a step B.

Consequently in Case I-A, a sample 1 and a sample 2 were connected in series. In Case I-B, a sample 3 and a sample 4 were stacked above the sample 1 and the sample 2 respectively and they were connected in series as shown in Fig. 1(a). In this case, we measured voltage distribution between CC samples and their stack that had analogous critical current. In Case II-A, there was a critical current gap between two CC samples. A sample 5 and the sample 1 were connected in series. After experiment Case II-A, the sample 4 and the sample 3 were stacked on the sample 5 and the sample 1 in Case II-B in order to make up disproportion from previous uneven critical current condition. The arrangement of samples in Case II is shown in Fig. 1(b). Specifications of each sample are shown in table II.

For measuring voltage of CC samples at quenches, voltage taps had been soldered on the middle point of each sample. In step B, voltage taps added on ends of CC samples above copper plates to monitor total voltage of stacked CC samples. The sample holder was made of glass fiber reinforced plastic shown in Fig. 2.

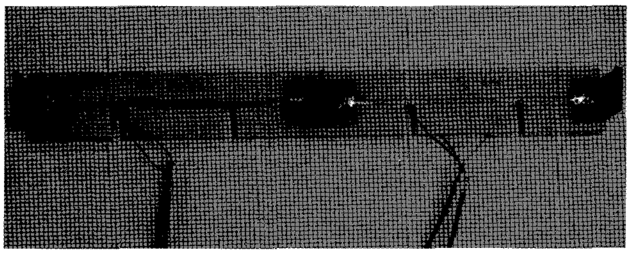

Fig. 2. Sample holder for series connection and stack.

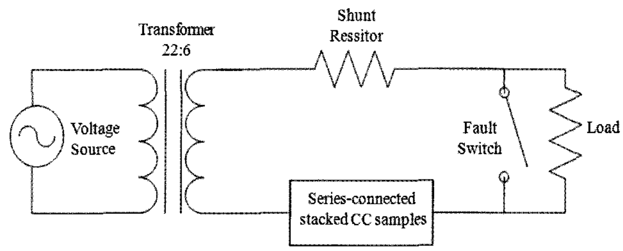

Fig. 3. The circuit diagram for the short circuit test.

2.3. Experimental Setup

The circuit diagram for the short circuit test is illustrated in Fig. 3. Short circuit tests were performed with increasing AC voltage by 70V which made temperature of the CC samples reached 300 K during the short circuit test. A fault switch was opened in the normal operation. When the fault switch closed, the fault current was generated for 0.1s, 6 cycles in 60 HZ. This fault current applied CC samples and made them quenched. The current in normal operation was controlled by a Load resistance and set its magnitude to 70% of minimum critical current of the CC samples. Sample holders with CC samples were immersed into liquid nitrogen which temperature was 77 K. All of the voltage of CC samples including at a moment of quenching was measured and analyzed.

3. RESULT AND DISCUSSION

3.1. Case I-A

In this paper, the critical current and stack condition of the samples were significant variables of affecting voltage distribution during the fault current. Fig. 4 shows the voltage response to the fault current of Case I-A to be applied 19.09 Vrms. As having seen from the waveform, the sample 1 and the sample 2 had even voltage distribution because of their comparable critical current. The first peak voltage of the sample 1 and the sample2 was 4.46 V and 4.4 V each. The last peak voltage of the sample 1 and sample 2 at fault duration were measured -4.92 V and -5.04 V. In Case I-A, the maximum voltage difference between two samples was 0.12 V and the minimum difference was 0.06 V. This result indicated even voltage distribution condition and this results were compared to other experiments.

3.2. Case I-B

In Case I-B, the samples having similar critical current

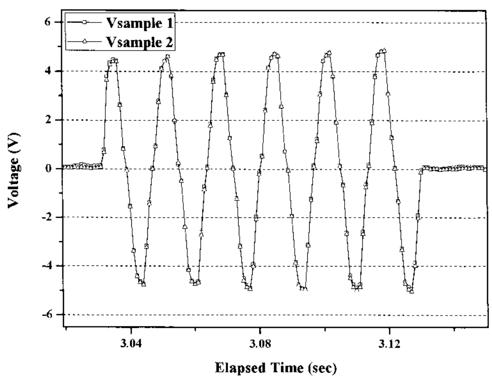

Fig. 4. Voltage distribution at fault to be applied 19.09 V_{rms} in Case I-A.

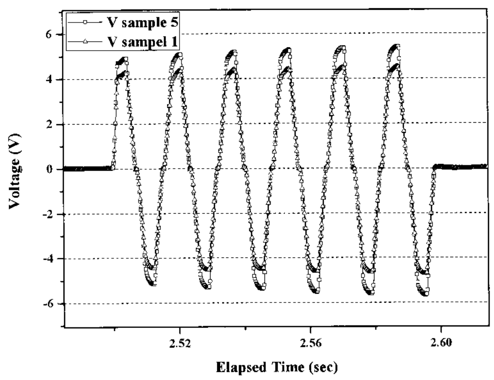

Fig. 6. Voltage distribution at fault to be applied 19.09 V_{rms} in Case II-A.

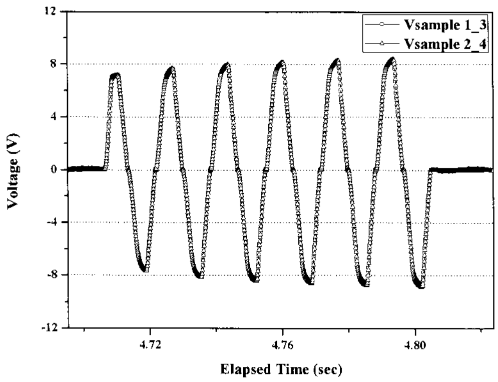

Fig. 5. Total voltage distribution of stacked samples to be applied 19.09 V_{rms} in CASE I-B.

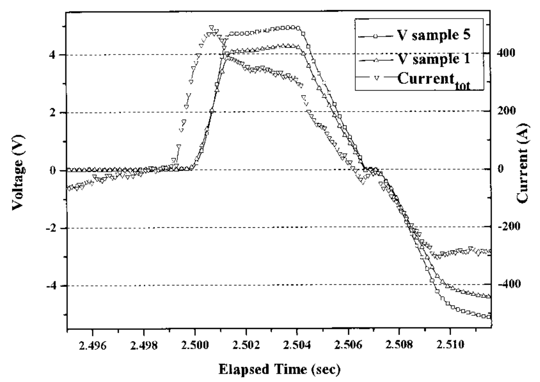

Fig. 7. Voltage and current waveforms of the first peak to be applied 19.09 V_{rms} in Case II-A.

were stacked on the samples of step A. The result is shown in Fig. 5. This is total voltage of stacked samples as explained in 2.2. The first peak voltage of the stacked samples, sample3 above on the sample1, was 7.19 V and sample2 above on the sample 4 was 7.15 V. At the last peak, the former voltage was -8.65 V and the latter one was -8.84 V. The voltage difference was similar to step A.

3.3. Case II-A

As the result of Case II-A, voltage difference between the sample 5 which had significant small critical current and the sample 1 getting bigger than the Case I-A. The output voltage of samples during the fault showed disparity in Fig. 6. The first peak voltage of the sample 5 and the sample1 was 4.7 V and 4.11 V respectively. The last peak voltage of the sample 5 was -5.66 V and the voltage of the sample 1 was -4.72V. In Case II-A, the maximum voltage difference between two samples was 0.94 V at the last peak and the minimum difference was 0.59 V at the first peak.

Fig. 7 is the peak of the first half cycle of the fault current and voltage output of the samples. This waveforms show that two samples had different quench behaviors. The fault current rose up to 494 A peak and the difference of the voltage of the sample 5 and the sample 1 had 0.59 V. During the fault current generated, over voltage was loaded on the sample 5 and under voltage was on the sample 1.This unequal behavior continued to the cycles and even the voltage difference became bigger.

3.4. Case II-B

In Case II-B, the uneven voltage distribution became reduced as shown in Fig. 8. This shows total voltage of the two stacked samples each. As fault current cycles passed, the voltage distribution condition became enhanced. The voltage of the stacked samples, the sample 4 stacked on the sample 5, at the first peak was 7.5 V and the sample 3 stacked on the sample 1, was 7.19 V. The voltage difference was 0.31 V that would not well balanced as much as in Case I-A. However in the last peak, the former voltage was -8.89 V and the latter one was -8.86 V. There was only 0.03V difference of voltage between stacked samples. Moreover Comparing to the Fig. 6, the absolute value of the uneven voltage distribution was reduced.

Fig. 9 shows the voltage of each sample at the last peak in Case II-B. The sample 4 which was stacked on the sample 5 had largest voltage value. This was because the sample 4 brought over-voltage which was loaded to the sample 5. The over current of the sample 5 was bypassed to the sample 4 through the stack. Therefore, the sample 4 had more voltage output than other samples and the other samples had similar voltage output.

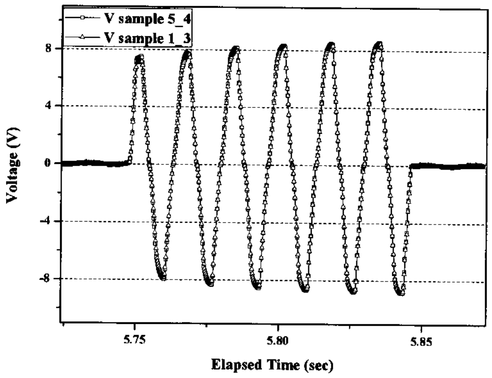

Fig. 8. Total voltage distribution of stacked samples to be applied 19.09 V_{rms} in CASE II-B.

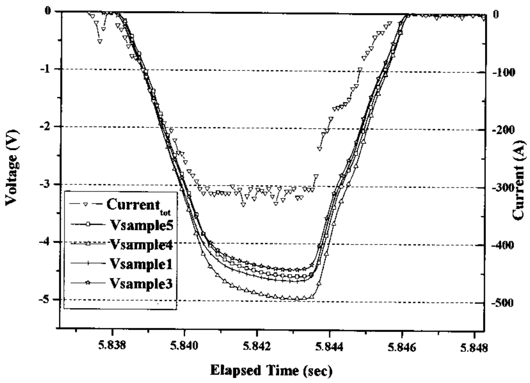

Fig. 9. Last peak voltage of the each sample and total current applied 19.09 V_{rms} in CASE II-B.

3.5. Summary

Fig. 10 shows the maximum line voltage difference between samples to be applied various voltages. With increasing applied voltage, line voltage difference mainly increases. As the result of experiments, Case I-A had the lowest difference of voltage and Case II-A had the largest values. Change of voltage distribution was affected by stacking CCs whether previous non-stack samples had even distribution or not. In Case I, stacked samples had more voltage dissimilarity than non-stack condition although this difference was less than Case II. In Case II, stack of normal sample can reduce the difference of voltage distribution of non-stack condition. Therefore, stack condition could change the voltage difference of non-stack condition. Especially in uneven voltage distribution condition, stacking CC which had normal critical current could reduce the former voltage disparity.

4. CONCLUSION

This paper deals with voltage distribution between stack CC samples connected in series. Because of Inhomogeneous characteristics of CC wire or possible degradation during operation of SFCLs, series-connected

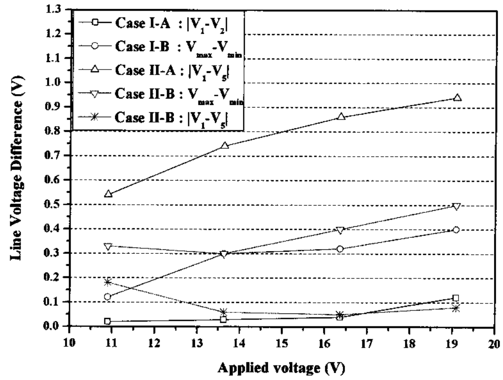

Fig. 10. Tendency of line voltage difference at last peak of all Cases of the experiments with increasing applied voltage.

HTS wire could have different characteristic like critical current. This difference could cause uneven quench behavior and disparity of voltage distribution. However, in stack condition, these unequal distributions would be reduced as the result of the experiment. In the future, our research group will investigate that quench characteristics and voltage distribution of series-connected CC magnets with having more stacks.

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