A Novel High Performance Scan Architecture with Dmuxed Scan Flip-Flop (DSF) for Low Shift Power Scan Testing

Jung-Tae Kim†, Insoo Kim*, Keon-Ho Lee*, Yong-Hyun Kim*, Chul-Ki Baek*, Kyu-Taek Lee and Hyoung Bok Min***

Abstract – Power dissipation during scan testing is becoming an important concern as design sizes and gate densities increase. The high switching activity of combinational circuits is an unnecessary operation in scan shift mode. In this paper, we present a novel architecture to reduce test power dissipation in combinational logic by blocking signal transitions at the logic inputs during scan shifting. We propose a unique architecture that uses dmuxed scan flip-flop (DSF) and transmission gate as an alternative to muxed scan flip-flop. The proposed method does not have problems with auto test pattern generation (ATPG) techniques such as test application time and computational complexity. Moreover, our elegant method improves performance degradation and large overhead in terms of area with blocking logic techniques. Experimental results on ITC99 benchmarks show that the proposed architecture can achieve an average improvement of 30.31% in switching activity compared to conventional scan methods. Additionally, the results of simulation with DSF indicate that the power-delay product (PDP) and area overhead are improved by 28.9% and 15.6%, respectively, compared to existing blocking logic method.

Keywords: Low power testing, power dissipation, scan flip-flop, shift mode, switching activity

1. Introduction

Scan design is the most widely adopted testing of VLSI circuits because it is a test methodology that allows one to control and observe all internal nodes in a synchronous design. Full-scan circuit is one form of design suitable for testability (DFT) techniques. In full-scan design, all functional flip-flops are replaced with scan cells, which are then configured as one or more shift registers during the shift operation. Generally, power dissipation during the test mode is significantly higher than that during the normal functional mode. Power dissipation can create problems such as difficulties with portable systems, increased product costs, and a decrease of total yield [1, 2, 3, 4]. Scan testing is classified as shift and capture mode. Test stimuli are loaded serially during the shift mode operation, while internal responses are loaded into scan flip-flops in parallel during the capture mode operation. In terms of power dissipation, circuit damage and reliability degradation are mostly caused by overheating due to shift power dissipation. On the other hand, excessive capture power dissipation can also lead to significant yield loss. For example, some fail chips work without any problems in the functional set test [4, 5].

Excessive switching activity during the test mode occurs due to the fact that all circuit flip-flops are active. And during the shifting of the test result, each flip-flop receives its input from the one preceding it. The functional operation of a circuit, on the other hand, typically necessitates reading and updating a few flip-flops every cycle, resulting in much lower switching activity in the circuit under test [6]. In [7, 8], the authors significantly describe a power dissipation model for CMOS logic circuits. The power dissipation of a gate g is approximated as:

$$P_g \approx \frac{1}{2} N_g f C_L V^2{}_{DD} \quad (1)$$

where N_g is the transition count of a gate g with a loading capacitance C_L and f is the operating frequency. For simplicity, the model uses the assumptions found in [9]. According to the paper, the power dissipation is proportional to the total transition count. The effective methods researched show how we can dramatically reduce the total transition count without performance degradation. Adding blocking logics into the output path of the scan flip-flops to prevent the propagation of switching activity to the logic gates and offers an effective and simple solution to significantly reduce the test power. However, such techniques result in performance degradation as they

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necessitate gate delay insertion on critical paths. The commonly used metrics in low-power design are power, the power-delay product, and the energy-delay product. Power alone is a questionable metric because it can be reduced simply by computing more slowly [10]. Consequently, we present a new scan testing approach aimed at the reduction of shift power dissipation and performance degradation.

In this paper, we propose a new scan architecture that changes the scan flip-flops and adds an extra circuit to flip-flops data input. More specifically, our contributions include the following:

1. We present an elegant signal blocking technique, referred to as DSF, to reduce switching activity in the combinational logic during scan shift mode.
2. The proposed architecture is effective compared to other blocking methods in terms of reducing power dissipation and delay penalty.
3. The area overhead for the DSF method is also lower than the existing blocking methods.

The rest of this paper is organized as follows. In Section 2, we briefly review some previous work on test power reduction. We present a new scan architecture which reduces the switching activity during the shift mode test in Section 3. Experimental and simulation results for ITC99 benchmark circuits are presented in Section 4. Finally, the conclusion and future work are given in Section 5.

2. Previous work

Several techniques have been proposed to reduce scan test power [2]. Previous techniques for reducing switching activity have focused mostly on reducing shift power dissipation during test operation. Typical approaches to shift power reduction include test scheduling [11], test vector manipulation [12, 13], scan chain modification [14, 15], clocking scheme manipulation [16], and circuit modification [17, 18]. They may be broadly classified as ATPG-based methods and Scan architecture-based methods. Incorporating power optimizations into ATPG algorithms typically results in test application time prolongation and the generation of complex test vectors. The simplest method to reduce test power are signal blocking techniques. In [17] and [18], an extra blocking gate is inserted to hold the outputs of all the scan cells at constant values during scan shifting. However, the main disadvantage of these approaches is the large area overhead, as additional logic is added to every scan cell. Moreover, it may degrade circuit performance due to the extra logic added between the scan cell outputs and the combinational logic.

3. Proposed Scan Architecture for Reducing Shift Power Dissipitation

During the scan shift operation, which leads to undesirable switching activity in the combinational logic, it is this switching activity that leads to excessive dynamic power during scan shift. The basic idea behind the proposed scan architecture is to replace a muxed scan flip-flop with a combination of novel dmuxed flip-flop and the transmission gate. This method effectively reduces shift power dissipation by blocking the switching activity of combinational logic during the shift operation. Fig. 1 shows conventional muxed scan flip-flop.

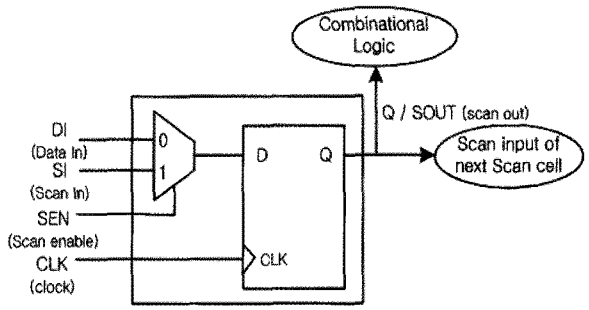
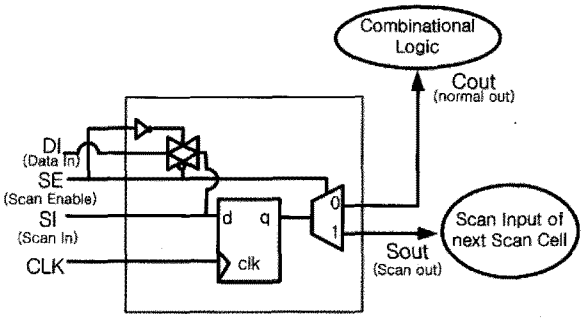
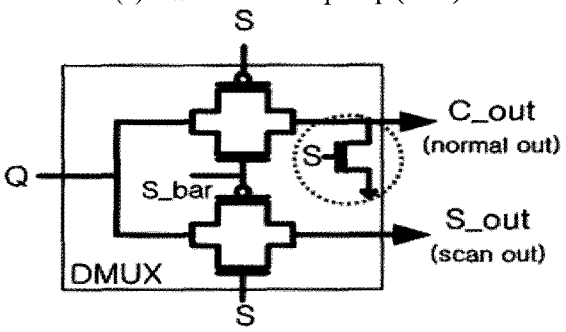


Fig. 1. Conventional scan flip-flop (Muxed scan flip-flop)

Fig. 2 presents the proposed DSF and dmux scheme. During the scan capture mode (SE = 0), the proposed scan flip-flop's operation is identical to the conventional muxed scan flip-flop, whereas the proposed scan flip-flop has a blocked influence toward combinational logic in the scan shift mode (SE = 1).



(a) Dmuxed scan flip-flop (DSF)



(b) NMOS pull-down dmux

Fig. 2. Proposed scan flip-flop and dmux scheme

At this time, the proposed scan flip-flop reduces power dissipation by blocking the switching activity of combinational logic during shift operation. During the

entire scan shift mode, DSF is controlled by the scan enable signal and the input of the combinational path is fixed to a low value by adding an NMOS pull-down transistor (as shown in Fig. 2(b)). Fig. 3 shows the operation path in the capture mode (SE = 0). The transmission gate and dmux of DSF are controlled by only a scan enable (SE) signal. Fig. 4 presents the operation path in the shift mode (SE = 1) and the dotted line means that the propagation of switching activity into the logic gates is blocked for low power testing.

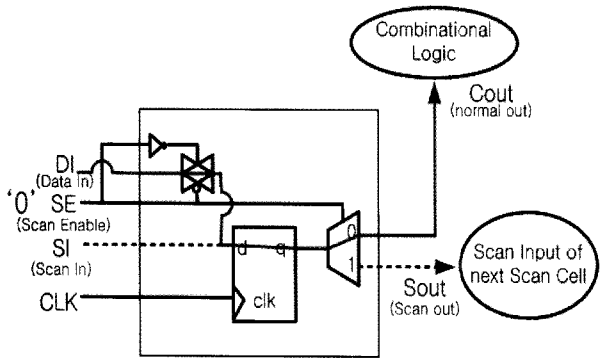


Fig. 3. Scan capture mode operation of DSF

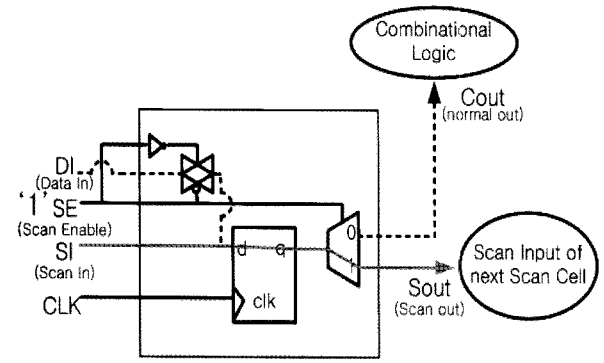


Fig. 4. Scan shift mode operation of DSF

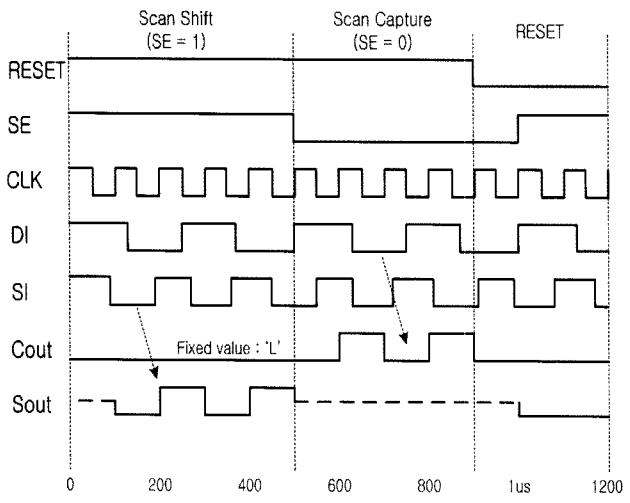


Fig. 5. Timing waveform of proposed scan flip-flop (DSF)

Fig. 5 shows the waveform of the proposed scan flip-flop. In the capture mode (SE = 0), the data input (DI) signal transfers to combinational logic through normal output (Cout). In the shift mode (SE = 1), the scan input (SI) signal connects to scan output (Sout) and the SI does not affect the Cout. Fig. 6 presents the scan chain architecture which consists of the proposed circuit (Dmux and Transmission gate) and Flip-Flop. In this paper, we propose a method which reduces the test power dissipation by blocking the unnecessary switching activity of combinational circuits.

4. Experimental and Simulation Results

The proposed shift power reduction architecture has been applied to several fully-scanned circuits in the ITC99 benchmark [19] set. For exact comparison, the gate-based blocking methods [17], [18] are also implemented in our experiments. In order to estimate the shift power reduction of the DSF method, we run a commercial tool to generate some ATPG patterns for each circuit. The sum of the total number of transitions at every signal line during scan shifting is used as an approximation to measure the scan shift power consumption.

Table 1 shows comparison results of the blocking methods. In Table 1, the total number of transitions and the percentage reductions of switching activity for each case are shown under "# of Transition of The Blocking Methods", and "Transition Reduction (%)", respectively.

From Table 1, it can be seen that the DSF method, the ANDB method in [18], and the MUX method in [17] reduce the average transition by 30.31%, 30.13%, and 34.87%, respectively. The MUX method in [17] to prevent the propagation of switching activity to logic gates holds the previous value by using the feedback path. On the other hand, the ANB method in [18] and the DSF method fix the logic value as "Low" during the scan shift operation.

Although the transition count varies with the operation of combinational circuits, we can experimentally indicate that the MUX method in [17] is slightly more effective than the DSF method for the low switching activities, as shown in Fig. 7. We evaluated the performance of a single scan cell in the normal operation mode because the blocking techniques result in performance degradation. In Fig. 8, the blocking methods show the data path of simulation. Table 2 compares the area overhead, delay, power and PDP (power-delay product) performance among the scan cells of several blocking methods, including the DSF method. Our simulation conditions are based on the 0.18-um process technology, the 100-MHz operating frequency and the 1.8-V supply voltage. All the power, cell delay, PDP, and area parameters were normalized by those of the proposed scan cell. We can observe from Table 2 that compared to the ANDB and MUX method, the DSF method is superior with respect to all parameters (power, delay, PDP, area). The results of simulation with DSF indicate that the power-delay product (PDP) and area

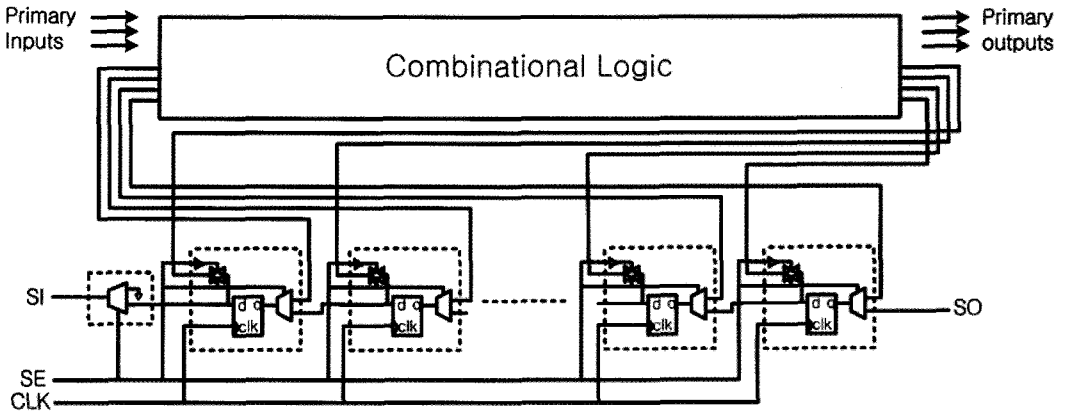


Fig. 6. Proposed scan chain architecture

Table 1. Comparison of the D method with the exhaustive method about switching activities in the benchmark circuits

Circuit	# of Gates	# of PI	# of PO	# of F/F	# of Patterns	# of Transition of The Blocking Methods				Transition Reduction (%).		
						Conv.	MUX [17]	ANDB [18]	DSF	vs. MUX [17]	vs. ANDB [18]	vs. DSF
B01	49	2	2	5	21	1876	1415	1586	1574	24.57	15.46	16.10
B02	28	1	1	4	14	766	538	618	611	29.77	19.32	20.23
B03	160	4	4	30	39	63302	43104	39640	39631	31.91	37.38	37.39
B06	56	2	6	9	20	3437	2370	2859	2853	31.04	16.82	16.99
B07	441	1	8	49	88	406186	227246	221374	221374	44.05	45.50	45.50
B08	183	9	4	21	57	63088	39873	45445	45441	36.80	27.97	27.97
B09	170	1	1	28	48	52134	38936	37476	37453	25.32	28.12	28.16
B10	206	11	6	17	69	55125	36038	42759	42754	34.62	22.43	22.44
B12	1076	5	6	121	185	5193401	3494622	3722436	3722373	32.71	28.32	28.32
B15	8922	36	70	449	618	262456474	110344236	105078007	105077923	57.96	59.96	59.96
Avg.	1129	7	11	73	116	26829579	11422838	10919220	10919199	34.87	30.13	30.31

overhead are improved by 14.12% and 3.57%, and 28.90% and 15.63%, respectively, compared to existing MUX and ANDB method. In Table 2, the advantage of the DSF method is shown in terms of percentages of improvement over other methods. The percentage of improvement is calculated as the percentage of reduction in PDP and area overhead from the other methods (pf_{OTHERS}) to the DSF method (pf_{DSF}), as shown in Eq. (2).

$$\%improvement = 100 * (pf_{OTHERS} - pf_{DSF}) / pf_{DSF} \quad (2)$$

A third set of experiments was performed in order to estimate the PDP performance as the change of operating frequency. As shown in Fig. 9, the performance of the DSF method is superior to other existing blocking methods and the performance gap increases in proportion to the operating frequency. Additionally, Fig. 10 shows the results that the PDP performance of the DSF method is improved by 14.12% and 28.90%, respectively, compared to the MUX and the ANDB method

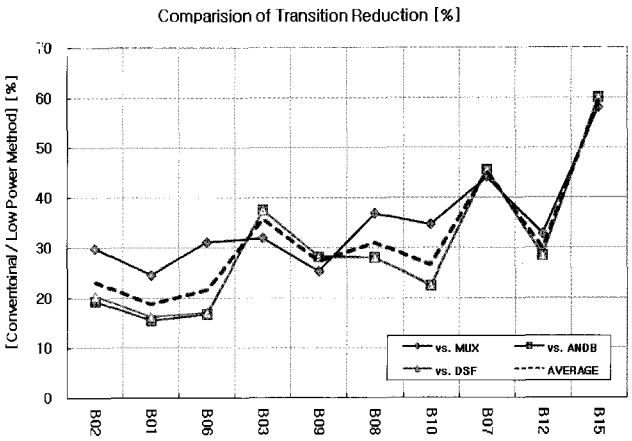
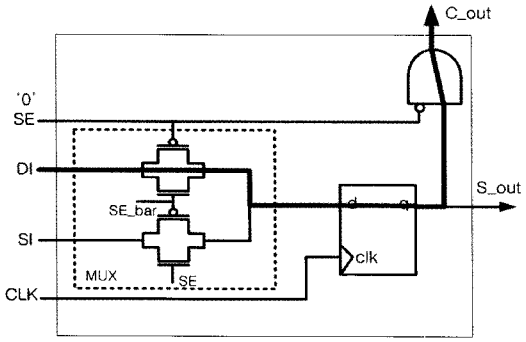


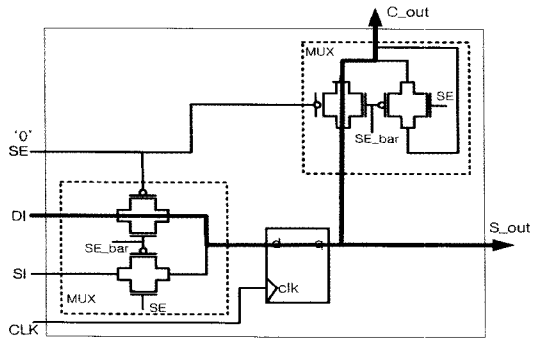
Fig. 7. Transition reduction of benchmark circuits according to blocking methods

Table 2. Comparison of area, delay, power, and PDP among several blocking methods applied to a single scan cell (at the 100-MHz operation frequency)

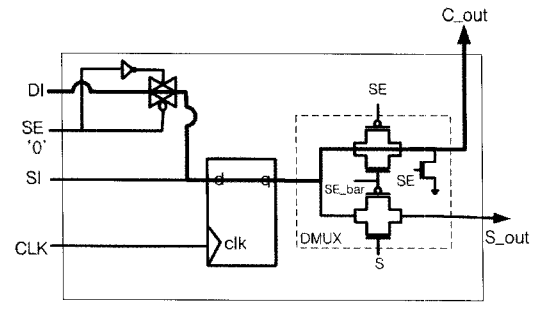
Method	Performance					vs. DSF	
	# of Tr (Scan cell)	Power (uW)	Delay (ns)	PDP (Power-Delay Product)	Area	Improvement of PDP(%)	Improvement of Area(%)
ANDB	32	1.32	1.06	1.41	1.19	28.90	15.63
MUX	28	1.14	1.02	1.16	1.04	14.12	3.57
DSF	27	1.00	1.00	1.00	1.00	0.00	0.00



(a) ANDB



(b) MUX



(c) DSF

Fig. 8. The data path of scan cell (normal mode)

From Figs. 9 and 10 it can be seen that the DSF method dramatically reduced the performance degradation problem compared to other blocking methods. These results demonstrate the effectiveness of the DSF method to large industrial designs.

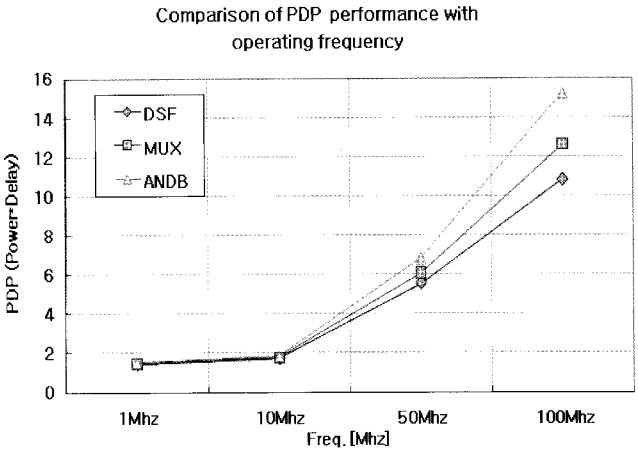


Fig. 9. Comparison of PDP performance with operating frequency

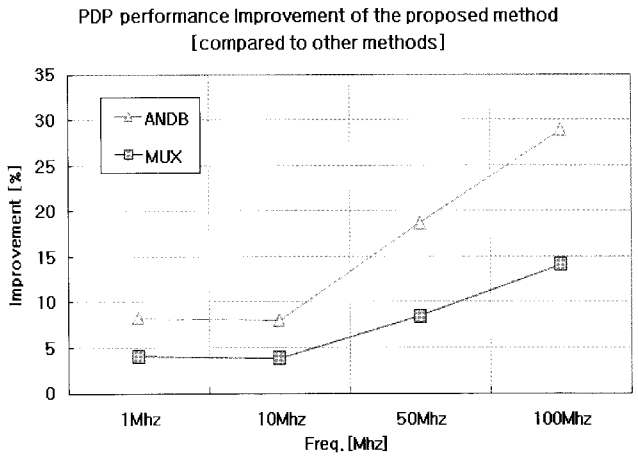


Fig. 10. PDP performance improvement of the DSF method with operating frequency (compared to other methods)

5. Conclusion

This paper presents a novel scan architecture for the reduction of power dissipation during scan shift testing. We replaced the muxed scan flip-flop with dmuxed scan flip-flop (DSF). Compared to existing methods using ATPG, the proposed technique can achieve a reduction in average power dissipation without complex test pattern generation. In this paper, we contribute to the reduction of switching activity as a result of the blocking influence to combinational circuits during the scan shift mode. Additionally, the proposed method dramatically reduced the performance degradation problem in the blocking methods. Experimental results on ITC99 benchmarks show that our method effectively reduces power dissipation. For future work we would like to run more experiments that evaluate the area overhead and timing delay. We also would like to optimize the circuit's performance.

Acknowledgements

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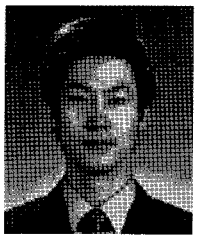

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