논문 2009-46SD-12-12

상보형 전하이동 경로를 갖는 표준 CMOS 로직 공정용 고효율 전하펌프 회로

(Complementary Dual-Path Charge Pump with High Pumping Efficiency in Standard CMOS Logic Technology)

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요 약

전하펌프의 성능은 공급전압에 의해 크게 영향을 받는다. 본 논문에서는 표준 twin-well CMOS 로직 공정으로 제작 가능하며, 낮은 공급전압에서도 높은 효율을 갖는 새로운 전하펌프 회로를 제안하고 검증하였다. 제안한 전하펌프는 이중의 전하 전달 경로와 간단한 2-phase 클락을 사용한다. 한 주기의 펌핑 사이클 동안 각 펌핑 단에서 입력전압을 2배로 승압하며, 상보적으로 연결된 PMOS 트랜지스터를 전달 스위치로 사용하여 트랜지스터의 문턱전압에 의한 전압강하 없이 승압된 전압을 다음 승압 단으로 전달한다. 시뮬레이션과 측정을 통해 제안한 전하펌프를 검증하였으며, 동일한 공정조건에서 제작 가능한 기존 전하펌프들 보다 높은 출력전압과 큰 전류 구동능력 그리고 더 높은 전력효율을 가진다는 것을 확인하였다.

Abstract

In this paper, we present a new charge pump circuit feasible for the implementation with standard twin-well CMOS process technology. The proposed charge pump employs PMOS-switching dual charge-transfer paths and a simple two-phase clock. Since charge transfer switches are fully turned on during each half of clock cycle, they transfer charges completely from the present stage to the next stage without suffering threshold voltage drop. During one clock cycle, the pump transfers charges twice through two pumping paths which are operating alternately. The performance comparison by simulations and measurements demonstrates that the proposed charge pump exhibits the higher output voltage, the larger output current and a better power efficiency over the traditional twin-well charge pumps.

Keywords : charge pump, dual charge-transfer path, two-phase clock, twin-well CMOS technology

I. Introduction

The charge pump which generates a higher voltage than the power supply is used to various applications such as EEPROM, flash memory[1~2] or high performance analog circuit[3~4]. As the power supply voltage scales down, the demand for pumping efficient charge pump is getting stronger.

Most of charge pumps in integrated circuits are based on the Dickson's architecture[5] because the design is simple. In the Dickson's charge pump circuit shown in Fig. 1(a), CLK and /CLK are two out-of-phase clocks with amplitude VDD and are capacitively coupled to alternate nodes along the diode-connected NMOS series. The two-phase clock increases the voltage of subsequent nodes as the pumping capacitors are successively charging and

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※ 이 논문은 2006년 정부(교육과학기술부)의 재원으로 한국연구재단의 지원을 받아 수행된 연구임 (KRF-2006-331-D00321).
접수일자: 2008년10월10일, 수정완료일: 2009년12월3일

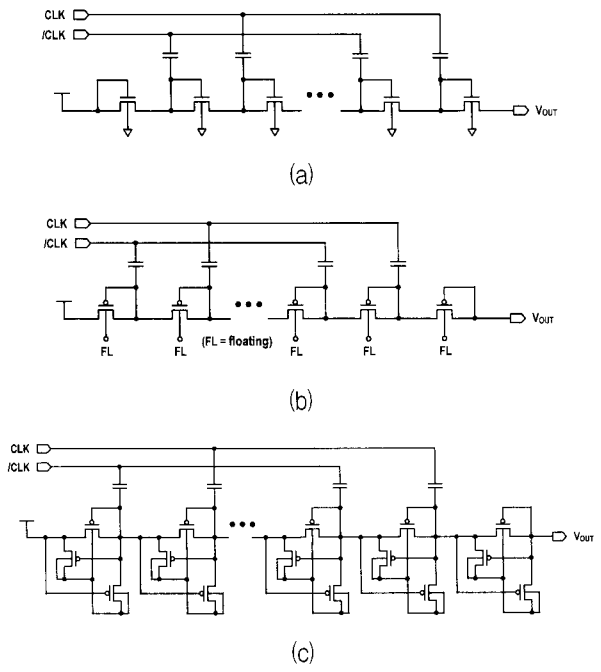


그림 1. (a) Dickson 전하펌프, (b) 플로팅-웰 전하펌프, (c) 바디-컨트롤 전하펌프

Fig. 1. (a) Dickson's charge pump, (b) Floating-well charge pump (FWCP), (c) Body-controlled charge pump (BCCP).

discharging during each half of the clock cycle. However, as the voltage of each stage increases by the charge pumping, the threshold voltage of the diode-connected NMOS increases due to the transistor body effect. Thus, the pumping efficiency is degraded when the number of pumping stages is increased. In order to counter this body effect problem, the floating-well charge pump (FWCP)[6] and the body-controlled charge pump (BCCP)[7] are proposed. They are shown in Fig. 1(b) and Fig. 1(c), respectively. But they can not overcome completely the problem associated with threshold voltage drop which is inherent in the diode-connected charge transfer transistor. Four-phase clock[8], voltage doubler[9] or charge recycling architecture[10] may be considered to cancel the charge loss due to the threshold voltage drop. But they need complex clock generator with additional boot-strapping circuits, and/or triple-well CMOS technology to alleviate body effect in the NMOS pass transistor.

In this work, a new charge pump circuit, named PMOS-switching dual-path charge pump (PDCP), is proposed. The main charge transfer switches are made with PMOS and operate with two-phase clock like the previous twin-well charge pumps. But it avoids completely the problem associated with threshold voltage drop of charge transfer transistor.

Ⅱ. Proposed Charge Pump

Fig. 2 depicts the proposed PDCP. Two-phase clocks (CLK, /CLK) with the amplitudes of V_{DD} are symmetrically connected to pumping capacitor (C_P). They are coupled alternatively when the stages are stacked. Each charge transfer stage has two pumping current paths, but the input of first stage and the output of final stage are connected together.

At the first stage whose inputs (N_{A0}, N_{B0}) are connected to V_{DD}, a stationary situation is reached after the initial transient. During the first half cycle, CLK = 0 and /CLK = V_{DD}, the initially V_{DD} precharged B1 node becomes $2V_{DD}$ by coupling of the pumping capacitor, and the node C1 becomes the ground level. This makes M11, M12 and M13 off, and M10 on. Therefore, the node A1 is precharged to V_{DD}. At this moment, M16, M17 and M18 are turned on by the node A1 voltage, but M15 whose gate and body voltage become $2V_{DD}$ is turned off. Therefore, the node B1 voltage of $2V_{DD}$ is transferred to N_{B1}. During the second half cycle, CLK = V_{DD} and /CLK = 0, the node A1 is boosted to $2V_{DD}$ and the node D1 becomes the ground level. Thus, M16, M17 and M18 are off, and M15 is on. Therefore, the node B1 is precharged to V_{DD}. Then, M11, M12 and M13 are turned on by the node B1 voltage, but M10 whose gate and body voltages become $2V_{DD}$ is turned off at this moment. As the result, the node A1 voltage of $2V_{DD}$ is transferred to N_{A1} during the second half cycle.

The second stage whose input voltage is 2VDD operates in a similar manner to the first stage. When CLK is 0 and /CLK is VDD, the node B2 is precharged to $2V_{DD}$, while the node A2 is in boosting

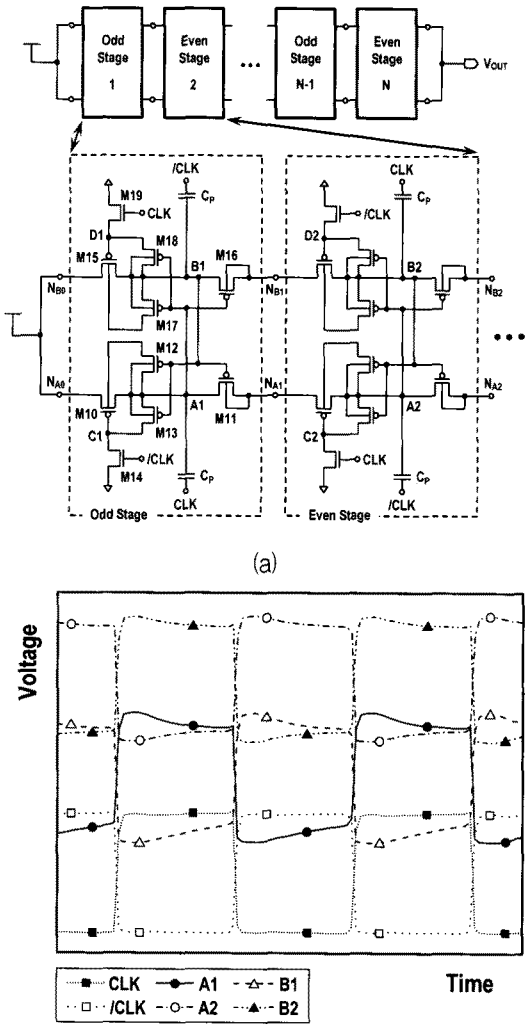


그림 2. PMOS 스위칭 이중 경로 전하펌프: (a) N-단의 구성, (b) 내부 전압파형

Fig. 2. PMOS-switching dual-path charge pump: (a) configuration of N-stage charge pump, (b) internal voltage waveforms.

state and transfers 3VDD to N_{A2}. Similarly, when CLK is V_{DD} and /CLK is 0, the node A2 is precharged to $2V_{DD}$, while the node B2 is in boosting state and transfers $3V_{DD}$ to N_{B2}. In this way, two out-of-phase clocks make the precharge and boosting operation alternately. Each stage operates contrary with the adjacent stages.

In the last stage, a final output voltage of $(N+1)V_{DD}$ is supplied from the previous stage alternately for each half cycle. The output node can maintain a high boosting voltage constantly.

In the proposed charge pump architecture, each charge transfer stage has two pumping current paths which are alternately derived by two-phase clock. At high clock frequency, the undesired charge feedback loss by the clock overlap may degrade the pumping efficiency. To make things work properly, we must avoid overlap in the gate signals of main charge transfer switches (M10, M15, M11, M16, ...). This can be done simply by adding asynchronous delays between two clock signals (CLK, /CLK) from the original clock source.

One concerning point might be that the well bodies of PMOS charge transfer devices (M10, M15, ...) switched by auxiliary PMOS devices (M12, M17, ...) are floated during each half clock cycle. The results may generate a transient substrate current, but do not affect pumping operation[6]. Another concerning point is that the proposed charge pump is limited by the breakdown voltage of NMOS switches (M14, M19, ...). The maximum drain-source and gate-drain voltages of the transistors exceed the power supply voltage. They should be high-voltage endurable devices with thick gate oxide and high breakdown voltage.

III. Performance Evaluation

1. Simulation and Comparisons

For evaluation of the proposed PDCP and its comparison to the traditional twin-well charge pumps (FWCP, BCCP), circuit simulations have been performed using a 0.35-μm 3.3-V standard logic CMOS device model. Their results are shown in Figs. 3-5. The threshold voltages of NMOS and PMOS transistors are 0.68 V and -0.71 V respectively. The breakdown voltages of both transistors are about 9 V. The load capacitance of each charge pump circuit is 30 pF. For fair comparison, the pumping capacitor in each stage must be same. Thus, the pumping capacitor of PDCP is set to 7.36 pF, while the pumping capacitor of FWCP and BCCP is set to 14.72 pF, respectively. The clock period is 50 ns. All parasitic capacitances

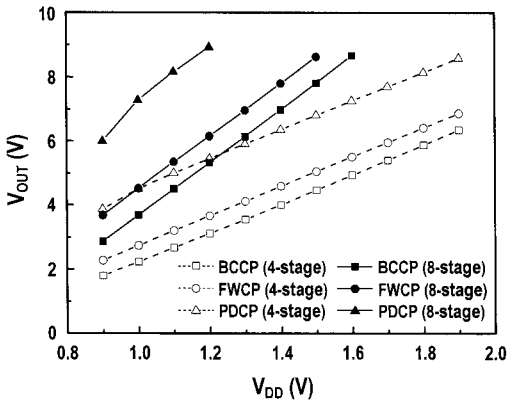


그림 3. 공급전압에 따른 출력전압 시뮬레이션
Fig. 3. Simulated output voltage as function of supply voltage.

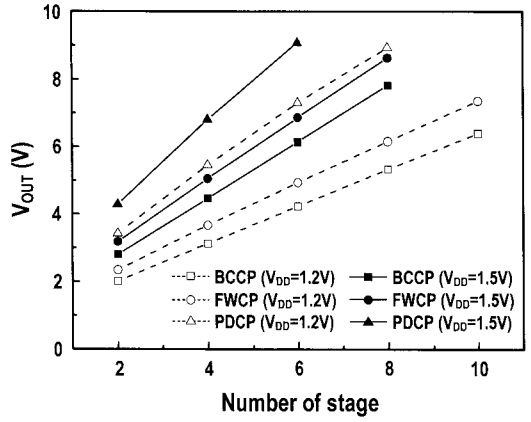


그림 4. 단수에 따른 출력전압 시뮬레이션
Fig. 4. Simulated output voltage as function of numbers of stage.

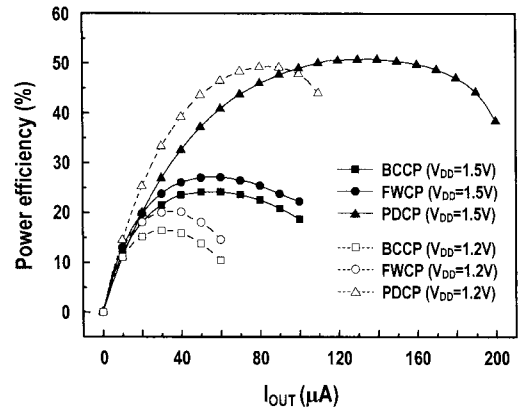


그림 5. 4단 전하펌프의 출력전류에 따른 전력효율 시뮬레이션
Fig. 5. Simulated power efficiency as function of output current in 4-stage charge pumps.

are included in the simulations.

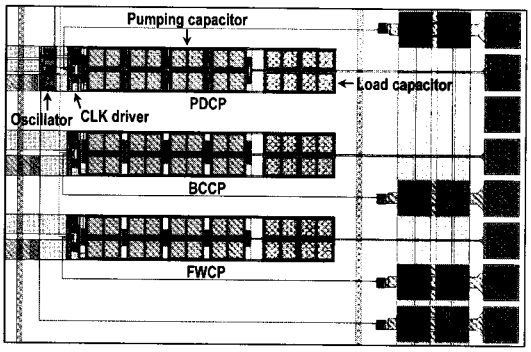
Figs. 3 and 4 show V_{DD} dependence and stage number dependence on pumping output voltage. For each clock cycle, the charge transfer transistors in PDCP are fully turned on to transfer charges from the present stage to the next stage. However, the charge transfer devices in FWCP and BCCP are diode-connected MOS transistors. They suffer charge loss due to the threshold voltage drop during transferring charges. Thus, the voltage gain (= V_{OUT}/V_{DD}) of PDCP is higher than that of FWCP and BCCP. It is more pronounced in low power supply near the transistor threshold voltage. The voltage gain of PDCP for 8-stage pump is 6.7 at V_{DD} = 0.9 V, while those of FWCP and BCCP are 4.1 and 3.2 respectively. It is at least 60 % higher.

Fig. 5 plots the power efficiency over a range of output current in 4-stage charge pumps. The proposed charge pump shows higher efficiency at a large output current above 30 μA. For VDD = 1.5 V, the maximum power efficiencies of FWCP and BCCP are 27 % and 24 % respectively, while the maximum power efficiency of PDCP is 51 %. The peak efficiency of PDCP is approximately double compared with that of the conventional charge pumps. It is also worth noting that the peak value of PDCP is nearly independent from the supply voltage value.

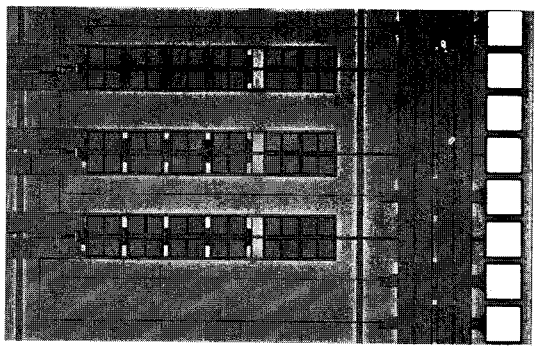
2. Test Chip Fabrication and Measurements

To validate the improvement achievable with the proposed charge pump, the above 4-stage PDCP, 4-stage FWCP and 4-stage BCCP have been fabricated and measured. All pumps were integrated in a 0.35-μm 3.3-V logic standard twin-well CMOS technology. Fig. 6 shows the photograph of implemented charge pumps. Pump switches are in the middle of the pumping capacitors. Since most of charge pump area is occupied by pumping capacitor and load capacitor, the layout areas of charge pumps are almost same. The core area of each 4-stage charge pump without load capacitor is 330-μm × 80-μm.

Fig. 7 shows transient output waveforms with V_{DD} = 1.5 V and no output load current. The output



(a)



(b)

그림 6. 4단 전하펌프의 사진:
(a) 레이아웃, (b) 제작된 칩 다이

Fig. 6. Microphotograph of 4-stage charge pumps:
(a) layout, (b) fabricated chip die.

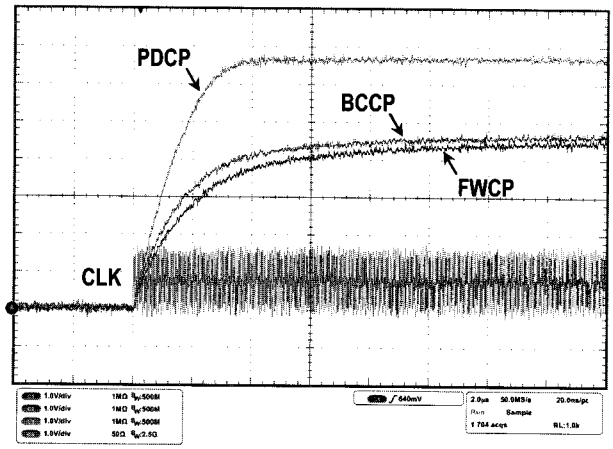


그림 7. 공급전원이 1.5 V 이고 출력 부하전류가 없을 때 4단 전하펌프의 초기 출력전압 측정결과 (전압: 1 V/div, 시간: 2 μs/div, 클락 주기: 50 ns)

Fig. 7. Measured initial output voltage for 4-stage pumps with V_{DD} = 1.5 V and no output load current (voltage: 1 V/div, time: 2 μs/div, clock period: 50 ns).

voltage of FWCP measures about 0.5 V less than that of simulation. It seems due to that the simulated

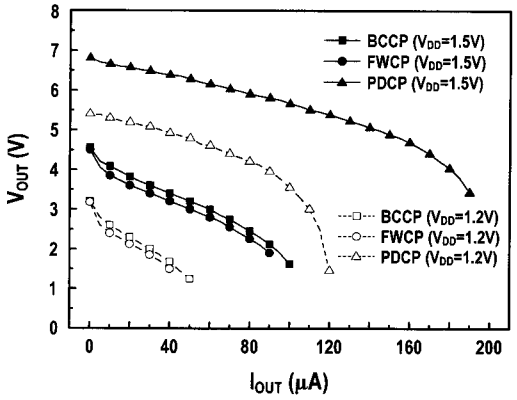


그림 8. 4단 전하펌프의 출력전류에 따른 출력전압 측정 결과

Fig. 8. Measured output voltage as function of output current in 4-stage charge pumps.

floating-well voltages at each pumping stage discord with those of real pump operation. In addition, the output voltage of PDCP measures 6.7 V. This value is practically lower than the ideal 4-stage value ($5V_{DD}$ = 7.5 V) because of stray capacitances in each pumping stage. Nevertheless, the PDCP provides the higher output voltage and smaller rise time than those of other charge pumps. The final output of PDCP with 30-pF capacitive load and 20-MHz clock frequency is settled downed in 5 μs after starting the pump operation, while those of FWCP and BCCP take much longer.

The output current drivability is another important performance factor in charge pump circuits. The measured output voltages with different output currents are compared in Fig. 8. Since the proposed charge pump has two alternate pumping paths transferring charges to the output node, the PDCP shows better performance. For the same output current, the PDCP generates much higher output voltage compared with two other circuits. Moreover it exhibits smaller output voltage drop while the output current increases.

Ⅳ. Conclusion

We have described a pumping efficient charge pump which employs PMOS-switching dual

charge-transfer paths and a simple two-phase clock. The proposed charge pump transfers charges through two pumping paths to the output node alternately without suffering threshold voltage drop. The test circuits for the proposed and traditional charge pumps have been fabricated in a standard twin-well CMOS technology. The layout areas of each charge pump are almost same, but the proposed charge pump provides the higher voltage gain, the larger current drivability and the higher power efficiency over the previous ones. It also exhibits much fast output rising at initial pumping transient. These properties make the proposed charge pump architecture suit for low-voltage memory or analog applications.

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