Pentacene Thin Film Transistors with Various Polymer Gate Insulators

Jae-Kyoung Kim*, Jung-Min Kim*, Tae-Sik Yoon*, Hyun Ho Lee, D. Jeon**** and Yong-Sang Kim†**

Abstract – Organic thin film transistors with a pentacene active layer and various polymer gate insulators were fabricated and their performances were investigated. Characteristics of pentacene thin film transistors on different polymer substrates were investigated using an atomic force microscope (AFM) and x-ray diffraction (XRD). The pentacene thin films were deposited by thermal evaporation on the gate insulators of various polymers. Hexamethyldisilazane (HMDS), polyvinyl acetate (PVA) and polymethyl methacrylate (PMMA) were fabricated as the gate insulator where a pentacene layer was deposited at 40, 55, 70, 85, 100 oC. Pentacene thin films on PMMA showed the largest grain size and least trap concentration. In addition, pentacene TFTs of top-contact geometry are compared with PMMA and SiO_2 as gate insulators, respectively. We also fabricated pentacene TFT with Poly (3, 4-ethylenedioxythiophene)-Polysturene Sulfonate (PEDOT:PSS) electrode by inkjet printing method. The physical and electrical characteristics of each gate insulator were tested and analyzed by AFM and I-V measurement. It was found that the performance of TFT was mainly determined by morphology of pentacene rather than the physical or chemical structure of the polymer gate insulator

Keywords: Organic Thin-Film Transistors, Pentacene, PMMA, Ink-Jet printing

1. Introduction

Organic thin-film transistors (OTFTs) have been studied with much interest over the past decade due to their attractive features such as low cost, low temperature processing and mechanical flexibility. Nowadays, owing to these excellent properties, there are a lot of potential applications, such as smart cards, RFID tags and flexible displays, etc [1], [2]. Typically, organic semiconductors have been investigated for applications of TFTs. Among the various organic semiconductors, pentacene-based TFTs have been showing the best performance especially in terms of their electrical properties such as mobility, threshold voltage and on-off ratio [3]-[6]. Recently, in pentacene TFTs, more attention was paid to the gate insulator due to its importance. They have recently reported the use of organic materials with low dielectric constants such as benzocyclobutene, poly-vinyl phenol, poly-paraphenylene-vinylene, etc. For these polymers used as gate dielectrics, the electrical performances of pentacence TFTs are similar to those obtained using inorganic dielectrics (such as thermal silicon dioxide and silicon nitride by plasma-enhanced CVD). Although its mechanism is not fully understood, the electrical conductance of organic semiconductors is known to be sensitive to morphology and grain structure of the organic semiconductors [7]. It indicates that properties of an organic semiconductor thin film will depend not only on the growth condition but also on its substrate.

In this work, we studied the morphology of pentacene thin films of different materials for gate insulators using an atomic force microscope (AFM) and X-ray diffraction (XRD). Three different polymer materials, hexamethyldisilazane (HMDS), polyvinyl acetate (PVA) and polymethyl methacrylate (PMMA) are adopted and compared. Also, the active layer of pentacene is deposited at 40, 55, 70, 85, 100 ℃. The pentacene TFTs with inverted-staggered structure were fabricated and the electrical performance was investigated by conventional I-V measurement. From these results, greater understanding of the conduction mechanism of organic semiconductors and the characteristics of pentacene TFTs were available with different polymer gate insulators.

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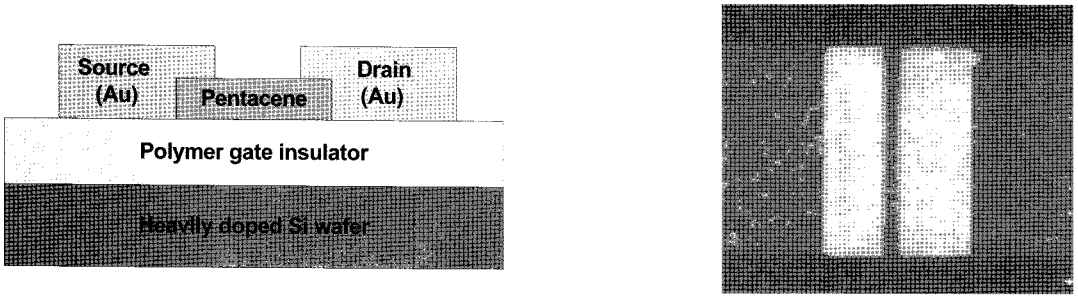
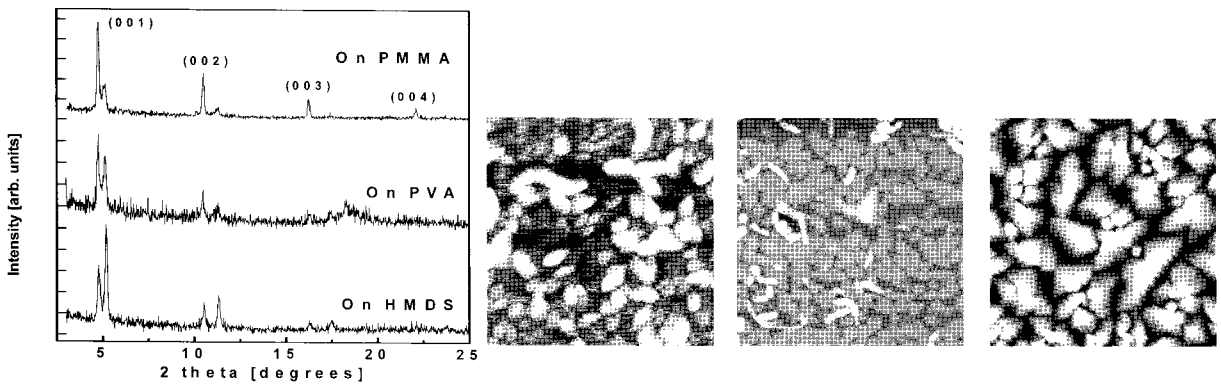


(a) (b)

Fig. 1. Schematic structure of the pentacene TFT: (a) schematic cross-section of a pentacene TFT, (b) a photograph of a pentacene patterned TFT with pentacene in the channel area only.

2. Experiments

For characterization of different polymer substrates, electrical performances of OTFTs were examined. The pentacene thin film was deposited respectively on HMDS, PVA and PMMA polymer substrates at various temperatures. Polymer layers were deposited by spin coating, and pentacene thin film was subsequently deposited by thermal evaporation. The pentacene (purchased from Aldrich) was used as received without further purification. The pentacnene TFTs were fabricated in an inverted-staggered structure as shown in Fig. 1. A heavily doped Si wafer was used both as a substrate and a gate electrode. For comparison between polymer and oxide gate insulators, a 100nm thick SiO_2 was prepared on the heavily doped Si by chemical vapor deposition with tetraethoxysilane. The SiO_2 surface was treated with HMDS by spin coating, which had been used to improve the quality of the pentacene/insulator interface. The PMMA (950K, purchased form Microchem) was deposited with a thickness of 260 ㎚ by spin coating and baked at 100 ℃ for 20 min on a hotplate. The pentacene active layer was patterned through the first shadow mask by thermal evaporation at a rate of 0.1 Å /s and its thickness was about 100 ㎚. The source and drain electrodes, a 80 ㎚ thick Au layer were deposited through the second shadow mask by thermal evaporation. All evaporation processes were carried out at pressure below 10-7 Torr. The pentacene TFTs thereby obtained have a channel length (L) and width (W) of 100 and 4000 ㎛, respectively. We also fabricated organic S/D electrode (PEDOT:PSS) by an inkjet printing method. Poly (3, 4-ethylenedioxythiophene)- Polysturene Sulfonate (PEDOT:PSS), is used for S/D and gate electrodes by an inkjet printing method. Though PEDOT:PSS is most widely used as an electrode material among various polymer materials, it has a low conductivity, hence is unsuitable for an electrode as it is. To increase its conductivity, dimethyl sulfoxide (DMSO) was mixed with the PEDOT:PSS. A surfactant, triton X-100, which facilitates the spreading of PEDOT:PSS on pentacene, was also added. After inkjet printing, it was baked at 100 ℃



(a) (b) (c) (d)

Fig. 2. XRD patterns (a) and AFM images of pentacene film deposited on (b) HMDS, (c) PVA and (d) PMMA. Pentacene thin film deposited at 85 ℃ and has an average thickness of 100 ㎚, 10 ㎛ x 10

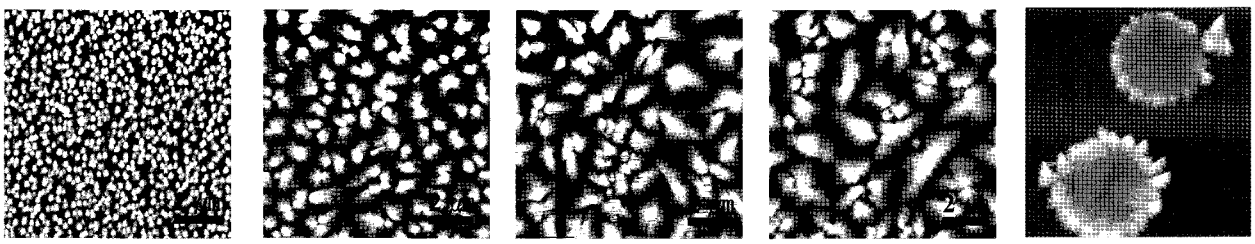


Fig. 3. AFM images of pentacene thin film depending on substrate temperature for the PMMA layer, $T_{sub.}$= 40 ℃, 55 ℃, 70 ℃, 85 ℃, 100 ℃, from left to right.

for an hour on a hotplate. The surface morphology of the pentacene thin films was investigated by AFM (XE-100, Park systems) and XRD (X'Pert PRO MRD, Phillips). Electrical characteristics were investigated using Keithley 237. All measurements were performed at room temperature. All experiments were perfomed under the atmospheric environment.

3. Result and Discussion

Fig. 2 shows the XRD patterns and AFM images of the pentacene thin film deposited on the HMDS, PVA and PMMA layer. The grain size of the pentacene deposited on the PMMA layer is the largest as shown in Fig. 2(b), (c), and (d). Since the carrier mobility is very sensitive to the molecular ordering of the pentacene and the carrier trapping at grain boundary, the larger grain size of pentacene on PMMA will result in higher field-effect mobility [8]. The structural orientation of pentacene thin films on three different polymer layers were analyzed using XRD (Fig 2(a)). Typically, a uniform film is known to be desirable for a high mobility of TFTs [9]. The pentacene film on PMMA shows a cleaner four diffraction peaks indexed as (00l), while those on PVA and HMDS show other interfering (hkl) peaks as well as (001) peaks.

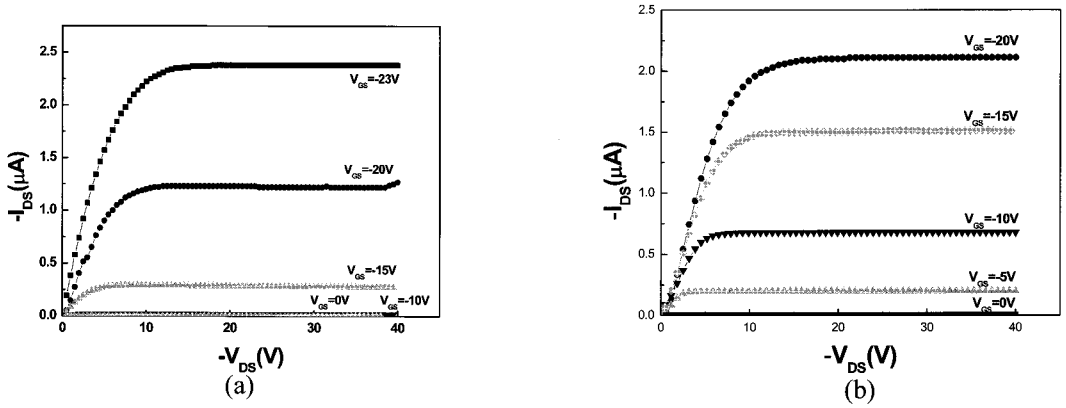


Fig. 4. Output characteristics of pentacene TFTs using the PMMA (a) and SiO_2 (b) as gate insulator.

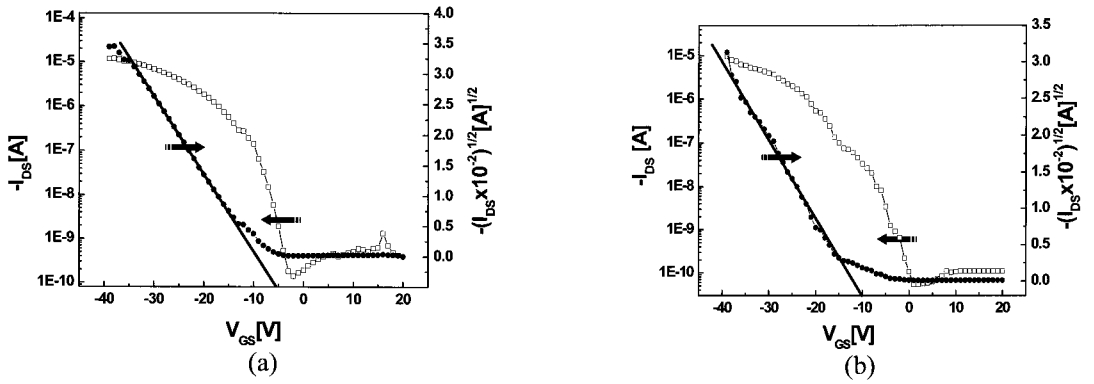
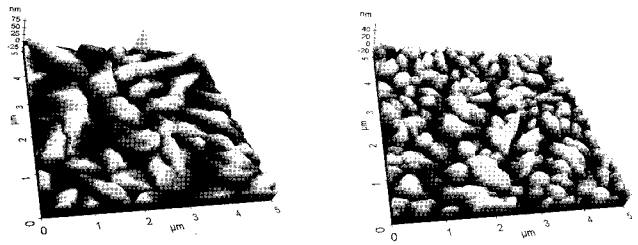


Fig. 5. Transfer characteristics of pentacene TFTs using the PMMA (a) and SiO_2 (b) as gate insulator.

It indicates that pentacene molecules grow more vertically with denser molecular packing on the PMMA layer than on PVA and HMDS [10]. Fig. 3 shows the AFM images of pentacene thin film on the PMMA layer depending on growth temperature. The pentacene inter-molecular bonding was stronger at a higher temperature than pentacene-substrate adhesion. Thus, the average grain size increased as the pentacene growth temperature increased [11]. However, when the temperature is too high, such as 100℃, the grain structure is disrupted as shown in Fig. 3 due to the re-evaporation of pentacene film at 100℃ [12]. The same morphological behaviors were observed on HMDS and PVA layers, too. The grain size of pentacene thin film in our work is largest when deposited on the PMMA layer at Tsub.= 85 ℃. We have also fabricated pentacene TFTs with PMMA and SiO_2 gate insulator (L=200 ㎛, W=4000 ㎛). Fig. 4 compares the drain-source current (I_{DS}) vs. drain-source voltage (V_{DS}) characteristics at various gate-source voltage (V_{GS}) for pentacene TFTs using PMMA and SiO_2 as the gate insulator. The I_{DS} of pentacene TFTs were obtained by V_{DS} sweeping from 0 to -40 V with the swept step of 0.5 V at the different V_{GS}. The conduction values at low V_{DS} are initially high, and decrease with increasing V_{DS}, indicating a good ohmic-contact between pentacene and source and drain electrodes. Fig. 5 shows transfer characteristics, V_{GS} swept from 20 to -40 V with the swept step of 0.5 V at the V_{DS} of -15 V, respectively. A higher field-effect mobility, μFET= 0.153 cm_2/Vs, a subthreshold voltage of 0.228 V/dec, a threshold voltage V_{th}= -5 V and on/off current ratio of $>10^5$ were obtained for pentacene TFTs with PMMA gate insulators. For the pentacene TFTs with the SiO_2 gate insulator, μFET= 0.105 cm_2/Vs, a subthreshold voltage of 0.325 V/dec, a threshold voltage V_{th}= -10 V and on/off current ratio of $>10^5$ were obtained. The TFT of PMMA gate insulator gave higher mobility and lower threshold voltage than that of SiO_2 gate insulator.



(a) (b)

Fig. 6. Pentacene thin-film layer deposited on (a) PMMA and (b) TEOS oxide

Fig. 6 shows the AFM images of pentacene grain on PMMA and SiO_2. In Fig. 6, topographic images of the pentacene film deposited on PMMA and SiO_2 show that pentacene layers grown on SiO_2 show grain structures with much smaller sizes. The result of Fig. 6 proves the results of Fig. 5. Or, the higher mobility and lower threshold voltage with the PMMA gate insulator were contributed from a larger grain size of pentacene than with the SiO_2 gate insulator. In order to achieve high carrier mobility, it would be necessary to reduce the number of grain boundaries per unit area [13]. Summarizing, it is shown that the pentacene could favor the PMMA surface for big crystalline grains, which consequently leads to improved field-effect mobilities. We have also fabricated pentacene TFTs with SiO_2 (100nm) and PMMA (260nm) double gate insulator (L=250 ㎛, W=1000) and PEDOT:PSS electrodes [Fig 7].

The drain current (I_{DS}) of pentacene TFTs, where the drain-source voltage (V_{DS}) was swept from 0 to -30 V with the swept step of 0.5 V at the different gate-source voltage (V_{GS}), is shown in Fig. 7(a). The conduction values at low V_{DS} shows an ohmic-contact characteristic

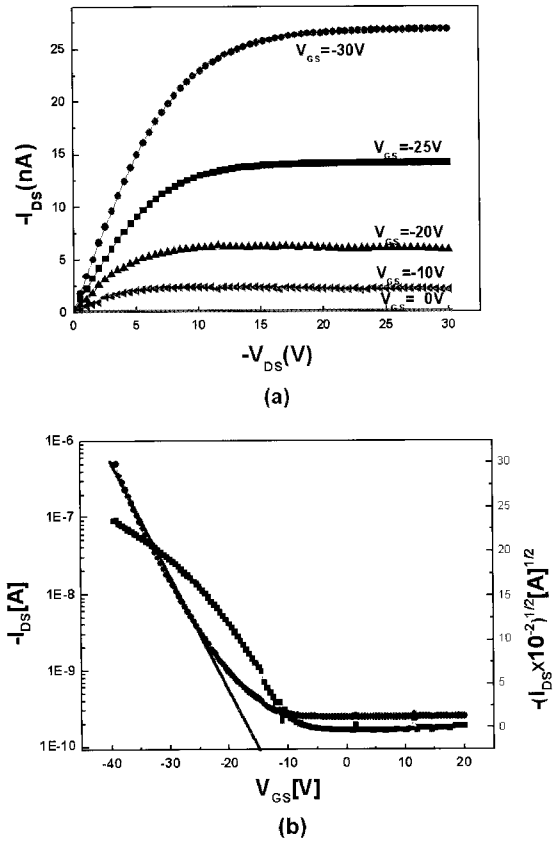


Fig. 7. Electrical characteristics of pentacene TFTs by ink-jet printing electrode : (a) output characteristics and (b) transfer chracteristics

between pentacene and source and drain electrodes though the current values are lower than previous devices (Fig. 4, 5) due to a thicker gate insulator. Fig. 7 (b) shows transfer characteristics, when the V_{GS} swept from 20 to -40 V with the step of 0.5 V at the V_{DS} of -20 V. From the experimental data a field-effect mobility μFET= 0.023 cm_2/Vs, a subthreshold voltage of 0.49 V/dec, a threshold voltage Vth= -18 V and on/off curent ratio of $>10^3$ are obtained for pentacene TFTs with PMMA gate insulators.

4. Conclusion

We studied the characteristics of pentacene on HMDS, PVA and PMMA polymer substrates at different substrate temperatures. The grain size of pentacene thin film is largest when petacene was deposited on the PMMA layer at Tsub.= 85 ℃. The pentacene TFTs with PMMA gate insulator shows the high field-effect mobility of μFET= 0.153 cm^2/Vs, the threshold voltage of -5 V and the on/off current ratio larger than 10^5, compared with the pentacene TFTs with SiO_2 gate insulator (μFET= 0.105 cm^2/Vs, a threshold voltage Vth= -10 V and on/off current ratio of $>10^5$). We have also demonstrated pentacene TFT with PEDOT:PSS S/D electrode by an inkjet printing method. This study can be extended for understanding other gate insulators.

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