Efficient Switch Mode Power Supply Design with Minimum Components for 5W Output Power

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Abstract – This paper presents a flyback technology in power conversion aimed at increasing efficiency and power density, reducing cost and using minimum components in AC-DC conversion. The proposed converter provides these features for square waveforms and constant frequency PWM. It is designed to operate in a wide input voltage range of 75-265VAC RMS with two output voltages of 5V and 20V respectively and full load output power of 5W. The proposed converter is suitable for high efficiency and high power density application such as LCDs, TV power modules, AC adapters, motor control, appliance control, telecom and networking products.

Keywords: Flyback Converter, Efficiency, Output Voltage Regulation, Output Voltage Ripple

1. Introduction

Engineers designing power supplies have been hit in recent years by new requirements or high efficiency. These have been concerned with efficiency performance on light load and full load conditions, and over the full range of line voltages. Strategically, the power conversion industry must welcome this pressure. Certainly, it adds to the cost and engineering efforts in the near term, but it makes the power supply a more respected and valuable product. The significance, however, is that a new way of thinking, a new design methodology, is needed for power converter design. The cost was once the sole goal. The cost has not diminished as a goal, but the target now is to keep the purchase price affordable. The key point is that high efficiency is getting more cost-effective.

The challenge for power converter designers is coming up with optimal topologies that can take full advantage of new devices in order to meet commercial and regulatory realities, and designing efficient products at low cost and reduced size. In terms of these efficient products, primary benefits that can be used to improve a system's performance include: improved reliability, reduced operating cost, reduced size, and high line performance. For improving the efficiency of any converter, transformer and inductor design plays a major role [1]-[2], and should be done very carefully. The flyback converter re-circulates energy to the input, causing an almost constant power loss, which becomes more apparent at low output power to get better efficiency [3]. The flyback converter also requires much fewer components and can help in cost reduction and size. This low power 5W AC-DC converter design uses only 16 passive and active components. If size is a major concern then surface mount device (SMD) components can be used for the proposed converter.

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2. Converter Configuration

Fig. 1 shows a PSIM model of the proposed single-phase, flyback buck-boost AC-DC converter for use in DCM operation. In this 5W high frequency AC-DC converter, the AC input is rectified and filtered by U1, C1 and C2 to create a high voltage DC bus which is connected to transformer Tx1. The inductor L1 forms a pi-filter in conjunction with C1 and C2 to reduce the electromagnetic interference (EMI) effect. The frequency jitter in U2 allows the unit to meet worldwide EMI conducted standards using a simple pi-filter in combination with a small value capacitor C3 and a proper PCB layout. The AC-DC converter operates at a 120kHz switching frequency generated by IC TNY266. This 120kHz PWM signal is applied at the gate terminal of the inbuilt switch (MOSFET) and other terminals are connected as per the pin details that can be seen in the datasheet. The secondary windings are stacked to improve the cross regulation. A 5V output winding is rectified and filtered by D2, C5 with additional filtering provided by L2, C6 to give the $5V_{DC}$ output. The $5V_{DC}$ output voltage is sensed by the sum of the voltage drops across the optocoupler U3 and the zener diode Z1. Resistor R1 (AC gain of the circuit) limits the current through U3, improving its response time to regulate the output voltage. Resistor R2 sets the necessary bias current for Z1. The 20V winding is rectified and filtered by D1, C4 to provide the $20V_{DC}$ output. The primary-to-secondary isolation is provided by using parts/materials (optocoupler/transformer insulation) with the correct level of isolation and creepage distances.

3. Design of Single-Phase Flyback Buck-Boost AC-DC Converter

In flyback converters, it fulfills the role of a couple inductor. There are mainly two criteria to decide the magnetizing inductance of the transformer. The first is to select the inductance in order to ensure the DCM operation from minimum load to maximum load condition. The second criteria depend upon the maximum ripple allowed in the primary. In order to ensure DCM of operation at maximum load, the following condition must be satisfied:

$$L_m < \frac{R_{L\,min}}{4f_s\left(\frac{1}{n}-\frac{V_o}{V_{I\,min}}\right)^2} \quad (1)$$

where L_m is critical inductance, f_s is switching frequency, $R_{L\,min}$ is minimum load resistance across both the output, n is primary to secondary turn ratio of transformer and $V_{I\,min}$ is minimum applied input voltage of the converter.

In order to ensure CCM operation at maximum load, following condition must be satisfied:

$$L_m > \frac{R_{L\,max}}{4f_s\left(\frac{1}{n}-\frac{V_o}{V_{I\,min}}\right)^2} \quad (2)$$

where $R_{L\,max}$ is maximum load resistance across both the output.

The output capacitor is selected on the basis of maximum peak-to-peak ripple (r_v) in output voltage (V_o) and frequency (w) as:

$$C_o > \frac{V_o}{w r_v R_{L\,min}} \quad (3)$$

These equations are used to get design data, which are used in the model of the proposed flyback buck-boost converter in PSIM6.0 to analyze its steady state and the dynamic behavior of the converter. Simulation is carried for a different load condition of 20%, 50% and 100% of rated power. The design procedure is presented here for the DCM mode of operation for the specification given in Table 1.

3.1 Flyback Power Transformer Design

To improve the efficiency of the AC-DC converter, one of the main co-sections has been given a transformer design. The flyback power transformer design is typically an iterative process which requires experience to produce the desired results. A flyback transformer does not act as a true transformer. A flyback transformer first stores energy received from the input power supply (charging portion of a cycle) and then transfer's energy (discharge portion of a cycle) to the output, usually a storage capacitor with a load connected across its terminals. In applications in which a complete discharge is followed by a short period of inactivity (known as idle time) the converter operates in a discontinuous conduction mode (DCM). In applications in which a partial discharge is followed by charging, the converter operates in the continuous conduction mode (CCM). This section describes a general transformer design procedure as applied to this application. Much of the iterative nature of the process is not presented for simplicity. The design procedure one may use is as follows:

(a) Select transformer geometry.
(b) Make assumption of transformer power losses.
(c) Select Transformer Size.
(d) Calculate minimum number of primary turns.
(e) Calculate turns ratio.
(f) Select wire to complete design.
(g) Verify power loss assumptions.

As a starting point, one has to assume that the transformer power losses are approximately 15%. One may arrive at this number by equating transformer losses to 7% of the converter output power. This is a reasonable assumption, but again is very application dependent. Most designs are a compromise between efficiency and size. With this assumption, one may narrow the core size down to a couple of choices based on the procedure of acceptable temperature rise. Finally, EE16 core has been chosen for a transformer design in this work.

The turns ratio (n) for the flyback transformer is defined based on minimum input voltage (V_{INmin}) and Vo' ($V_o' = V_o + D_{drop}$) where D_{drop} is equivalent to a Schottky diode (D2) drop at the secondary side and the desired duty cycle (D).

$$n = \frac{V_{IN\,min}}{V_o'}\frac{D}{(1-D)} \quad (4)$$

The core loss (P_c) of the transformer can be calculated by the given equation and values can be found out from the manufacturer's data sheet.

$$P_c = pV_c \quad (5)$$

where p is the specific loss in watt/cm^3 and Vc is the volume of the core in cm^3.

The inductance value (L) required for the secondary current to ramp from peak to zero at the boundary of continuous and discontinuous mode is as:

$$L = V_O \cdot \frac{\Delta t}{\Delta I} = V_O \cdot \frac{T(1-D)}{\Delta I} \tag{6}$$

where ΔI is the change in current across the inductor at Δt change in time.

Calculate the number of secondary turns (N_S) to provide the desired inductance value:

$$N_S = \frac{L}{\Delta B_{MAX}} \frac{\Delta I}{A_E} \tag{7}$$

where ΔB_{MAX} is the maximum flux density and A_E is the effective core area of the transformer. The number of primary turns (N_P) is now calculated as:

$$N_P = nN_S \tag{8}$$

Now, calculate the gap length (l_g) to achieve the inductance value as:

$$l_g = u_o N_S^2 \frac{A_E}{L} (1 + \frac{l_g}{D})^2 \tag{9}$$

The peak secondary current (I_{Spk}) of the transformer at the boundary condition can be derived from secondary side DC current (I_{SDC}) which is defined as:

$$I_{SDC} = I_{Spk} \frac{(1-D)}{2} \tag{10}$$

The peak secondary from eqn. (10) is as:

$$I_{Spk} = I_{SDC} \frac{2}{(1-D)} \tag{11}$$

The secondary winding side rms current (I_{Srms}) can be calculated as:

$$I_{Srms} = \sqrt{I_{Spk}^2 \frac{(1-D)}{3}} \tag{12}$$

The secondary winding side AC current (I_{Sac}) can be calculated as:

$$I_{Sac} = \sqrt{I_{Srms}^2 - I_{SDC}^2} \tag{13}$$

The secondary side DC resistance (R_{SDC}) can be calculated as:

$$R_{SDC} = \rho \frac{l}{A} \tag{14}$$

where, ρ is a constant, l is length of the wire and A is the cross section area of the wire.

Now secondary side AC resistance (R_{SAC}) can be derived from eqn. (14) for two output windings:

$$R_{SAC} = 2R_{SDC} \tag{15}$$

the primary side peak current (I_{Prms}) can be derived from secondary side peak current which is:

$$I_{Ppk} = \frac{I_{Spk}}{n} \tag{16}$$

Now primary side DC current (I_{PDC}) can be derived from primary side peak current which is:

$$I_{PDC} = I_{Ppk} \frac{D}{2} \tag{17}$$

The primary side rms current (I_{Prms}) can be calculated as:

$$I_{Prms} = \sqrt{I_{Ppk}^2 \frac{D}{3}} \tag{18}$$

The primary side AC current (I_{Pac}) can be calculated as:

$$I_{Pac} = \sqrt{I_{Prms}^2 - I_{PDC}^2} \tag{19}$$

The primary side DC resistance (R_{PDC}) can be calculated as:

$$R_{PDC} = \rho \frac{l}{A} \tag{20}$$

where, ρ is a constant, l is length of the wire and A is area of the wire.

Now primary side AC resistance (R_{PAC}) can be derived from the eqn. (20) for one input winding:

$$R_{PAC} = R_{PDC} \tag{21}$$

The secondary side DC loss (P_{SDC}) and AC loss (P_{SAC}) can be defined as:

$$P_{SDC} = I_{SDC}^2 R_{SDC} \tag{22}$$

$$P_{SAC} = I_{SAC}^2 R_{SAC} \quad (23)$$

Now total secondary winding loss (P_{SW}) can be calculated as:

$$P_{SW} = P_{SDC} + P_{SAC} \quad (24)$$

The primary side DC loss (P_{PDC}) and AC loss (P_{PAC}) can be defined as:

$$P_{PDC} = I_{PDC}^2 R_{PDC} \quad (25)$$

$$P_{PAC} = I_{PAC}^2 R_{PAC} \quad (26)$$

Now total primary winding loss (P_{PW}) can be calculated as:

$$P_{PW} = P_{PDC} + P_{PAC} \quad (27)$$

Now total winding loss (P_W) can be defined as some of the secondary and primary winding loss:

$$P_W = P_{SW} + P_{PW} \quad (28)$$

So the total loss in the transformer (P_T) can be calculated easily and would be:

$$P_T = P_W + P_C \quad (29)$$

4. Modelling and Simulation

Computer simulation is an important tool that aids in the design of circuits. It is then possible to verify whether the simulated results predict a circuit performance that is consistent with the design goals even before the circuit is implemented. On the basis of obtained design, the simulation of the converter is carried out in a discontinuous conduction mode (DCM) operation. Fig. 1 shows the PSIM model of a flyback buck-boost converter in DCM operation. As discussed already, it uses voltage mode control to regulate the output voltages. The converter consists of PWM control using the voltage follower approach. Simulation is carried out for steady state performance from 10% to 100% loading conditions and dynamic performance for sudden application of 100% load and then removal of load (10%-100%-10% load change) in DCM operation. Simulated results are shown in Figs. 2-6 and single-switch flyback converter design results are summarized in Table 1, which includes converter inputs, device variable detail, transformer design parameters and output detail.

5. Experimental Evaluation for Flyback Buck-Boost AC-DC Converter

A 5W single-phase flyback buck-boost AC-DC converter prototype is developed with 5V and 20V output voltages and having a transformer isolation with 120kHz switching frequency in DCM operation. It includes the control supply, overload and overvoltage shutdown protections. The voltage follower approach is applied for the control using chip TNY266 which has an inbuilt switch and PWM generator. The hardware implementation is carried out using the parameters designed and verified through the simulation results. The prototype of the flyback buck-boost converter is developed as per the circuit design for the simulation in Fig. 1 and tested from 10% to 100% loading conditions at input voltages variation of 75V to 265V. The converter shows the voltage regulation for variable input voltage and for load change from 0.5W to 5W. The components used in the hardware implementation of the flyback buck-boost converter are summarized in Table 2 with detailed description. The converter's overall efficiency, including the control circuit, has been measured for prototype as a function of the input voltage at different loading conditions and the result is shown in Table 3. One can see that the flyback converter can achieve an improved efficiency in all the input voltage ranges at the maximum loading condition, which corresponds to the maximum duty-cycle and the worse reverse recovery of the freewheeling diode. The maximum efficiency is achieved 83.9% at maximum loading condition on both outputs. Based on the results summarized in Table 3, the load and line regulation have been calculated for a single-phase flyback AC-DC converter and the results summarized in Table 4 at different line and load conditions.

6. Result and Discussion

Figs. 2-6 show the PSIM6.0 simulated output voltages waveform at 10% to 100% loading condition or at 20mA to 200mA load current in DCM operation. The 20V output voltage at 10% load and 5V output voltage at 10% load are shown in Fig. 2 at 220V input AC voltage. The 20V output voltage at 10% load and 5V output voltage at 100% load are shown in Fig. 3. The 20V output voltage at 100% load and 5V output voltage at 100% load are shown in Fig. 4 at 220V input AC voltage. Finally, 20V output voltage at 100% load and 5V output voltage at 10% load are shown in Fig. 5 at 220V input AC voltage. In all the simulation waveforms the output voltages ripple is observed 300mV (1.5%) at 20V and 40mV (0.8%) at 5V output. The switch voltage and current are shown in Fig. 6 at 100% load in DCM mode, where applied AC input is nominal at 220V.

The prototype flyback buck-boost AC-DC converter in

DCM is tested for different loading conditions with a wide range of input voltage to demonstrate its steady state performance. The input and output ground are designed using an optocoupler and performance improvement is achieved by different experiments. Figs. 7-11 show the experimental results of this converter. The 5V and 20V output voltages are tested at no load, minimum load (20mA) and at maximum load (200mA).

Switching noise is observed in the AC mains current, which is reduced by using an EMI filter. An input π (pi) (C-L-C) filter of 2.2mH and 6.8μF is used to improve the source current waveform. Fig. 7 shows the 20V output voltage at 20mA load and 5V output voltage at 20mA load, where applied input AC is kept at nominal value of 220V. Fig. 8 shows the 20V output voltage at 20mA load and 5V output voltage at 200mA load in DCM operation. Fig. 9 shows the 20V output voltage at 200mA load and 5V output voltage at 200mA load, which is the maximum loading condition of the converter. Finally, 20V output voltage at 200mA load and 5V output voltage at 20mA load are shown in Fig. 10 at nominal 220V input AC voltage. The maximum peak to peak ripple for 5V is observed 50mV (1%) and for 20V is observed 400mV (2%) at 75-265V input AC voltage. These experimental results are very close to the simulation results. The switch voltage and current at 100% load are shown in Fig. 11. The peak voltage of 370V and peak current 220mA across switch are observed under the worst conditions.

7. Useful Hints

The figures and tables are listed in section 4.1 and 4.2 respectively.

7.1 Figures

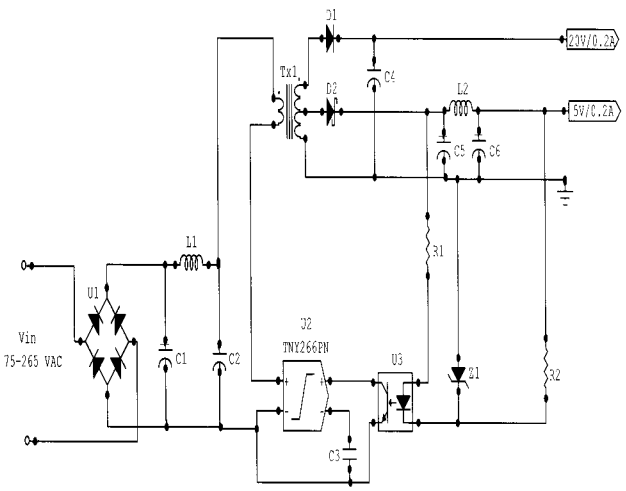

Fig. 1. 5W Flyback AC-DC converter in DCM operation.

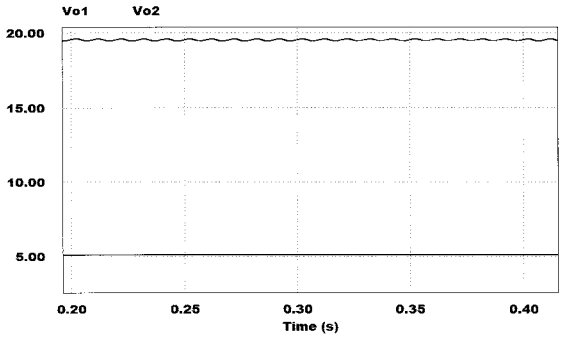

Fig. 2. Output Voltages 20V@20mA and 5V@20mA at 220V AC input.

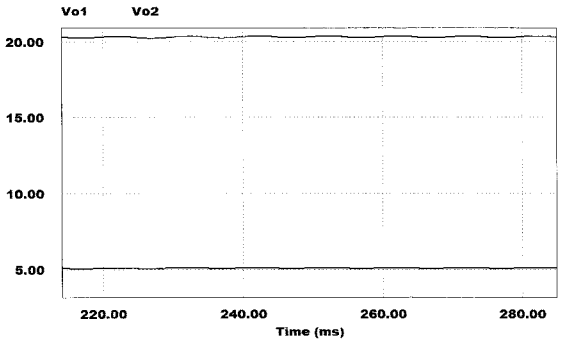

Fig. 3. Output Voltages 20V@20mA and 5V@200mA at 220V AC input.

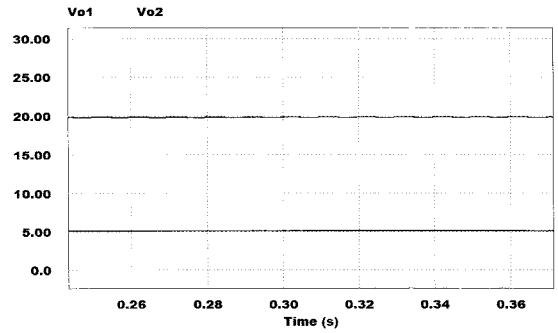

Fig. 4. Output Voltages 20V@200mA and 5V@200mA at 220V AC input.

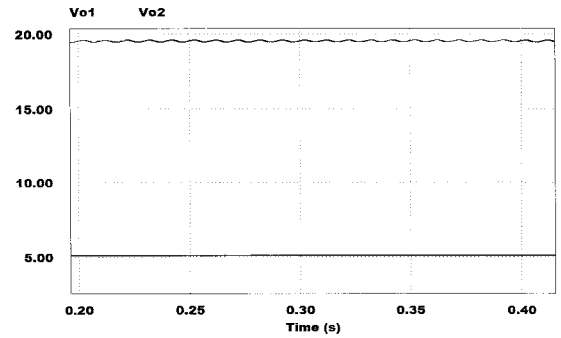

Fig. 5. Output Voltages 20V@200mA and 5V@20mA at 220V AC input.

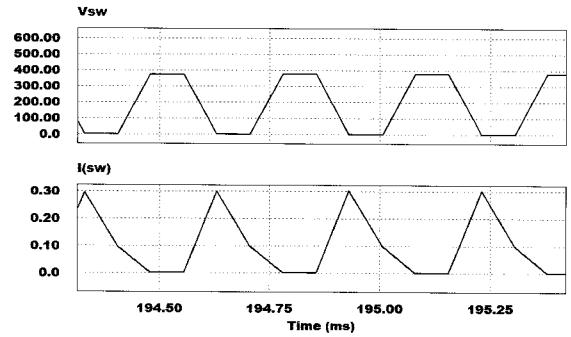

Fig. 6. Switch Voltage and Current at 5V@200mA and 20V@200mA at 220V AC input.

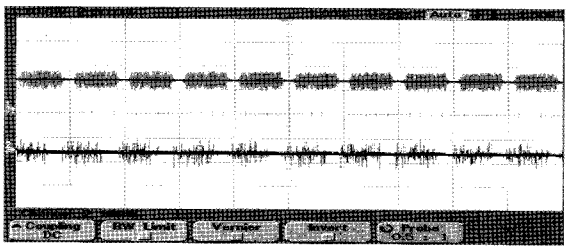

Fig. 7. Output voltages 20V@20mA and 5V@20mA at 220V AC input, Scales: 5V/div, 2V/div and 5ms/div.

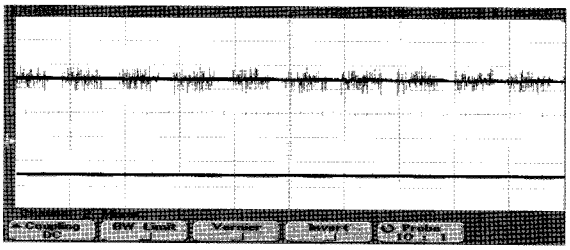

Fig. 8. Output voltages 20V@20mA and 5V@200mA at 220V AC input, Scales: 5V/div, 2V/div and 5ms/div.

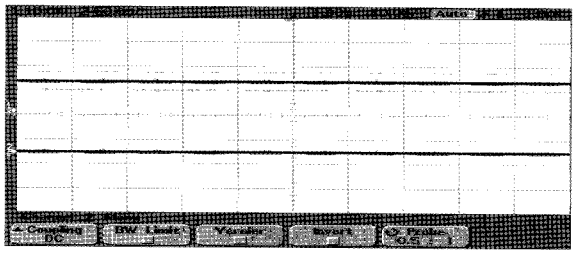

Fig. 9. Output voltages 20V@200mA and 5V@200mA at 220V AC input, Scales: 5V/div, 2V/div and 5ms/div.

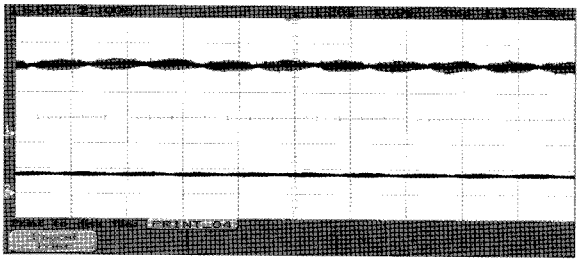

Fig. 10. Output voltages 20V@200mA and 5V@20mA at 220V AC input, Scales: 5V/div, 2V/div and 5ms/div.

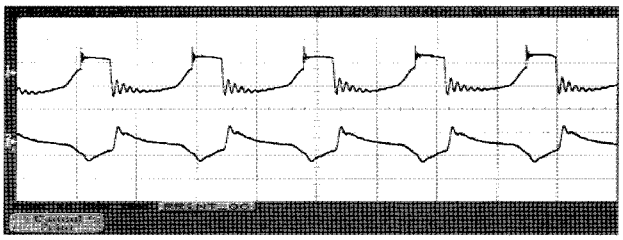

Fig. 11. Switch Voltage and Current 20V@200mA and 5V@200mA at 220V AC input, Scales: 200V/div, 0.2A/div and 5ms/div.

7.2 Tables

Table 1. Design results of single-phase flyback converter

Variable	Value	Description
AC-DC Converter Inputs		
VAC (min)	75V	Minimum Input AC Voltage
VAC (max)	265V	Maximum Input AC Voltage
F_L	50Hz	Line Frequency
η	80%	Estimated Efficiency
C_{IN}	6.8μF	Input Capacitance
V_{min}	82V	Minimum DC Input Voltage
V_{max}	375V	Maximum DC Input Voltage
Device Variable		
TNY266	--	PWM Generator and Switch Regulator
Po	5W	Total Output Power
V_{Drain}	617V	Maximum Drain Voltage
V_{DS}	6.2V	Drain to Source Voltage
f_s	120kHz	Switching Frequency
Transformer Design Parameters		
Core	EE16	Core Type
Core manuf.	Elytone	Core Manufacturer
N_P	200	Number of Primary Turns
L_P	1.03mH	Primary Inductance
l_g	0.414mm	Estimated Gap Length
A_E	19.4mm^2	Effective Core Area
L_L	11.1μH	Primary Leakage Inductance
I_{Prms}	0.13A	Primary rms Current
I_{Ppk}	0.39A	Primary Peak Current
I_{PDC}	78mA	Primary DC Current
I_{Pac}	104mA	Primary AC Current
AWG	35	Primary Wire Gauge
Output_1 (5V)		
V_{o1}	5V	Output Voltage
I_{o1}	200mA	Output Current
PIVS1	21V	Maximum Peak Inverse Voltage
I_{Srms1}	0.52A	Secondary rms Current
I_{Spk1}	1.49A	Secondary Peak Current
I_{SDC1}	298mA	Secondary DC Current
I_{Sac1}	426mA	Secondary AC Current
L_{21}	2.2-20μH	Output Filter Inductance
N_{S1}	9	Number of Secondary Turns
L_{S1}	45μH	Secondary Inductance
Output_2 (20V)		
V_{o2}	20V	Output Voltage
I_{o2}	200mA	Output Current
PIVS2	80V	Maximum Peak Inverse Voltage
I_{Srms2}	0.52A	Secondary rms Current
I_{Spk2}	1.49A	Secondary Peak Current
I_{SDC2}	298mA	Secondary DC Current
I_{Sac2}	426mA	Secondary AC Current
N_{S2}	32	Number of Secondary Turns
L_{S2}	160μH	Secondary Inductance
AWG	30	Secondary Wire Gauge

Table 2. Component specification of single-phase flyback buck-boost converter

No.	Description	Manufac.	Ref.
1	Diode Bridge, 600V, 0.8A	Diodes	U1
2	Electrolytic Capacitor, 6.8μF, 400V	Nippon	C1, C2
3	Inductor, 2.2mH, 0.11A	Panasonic	L1
4	Flyback Transformer	Elytone	Tx1
5	PWM generator, Switch	Power Int	U2
6	Ceramic Capacitor, 0.1μF, 50V	Panasonic	C3
7	Diode, 400V, 1A	Vishay	D1
8	Schottky Diode, 100V, 1A	Fairchild	D2
9	Optocoupler, 80V	Sharp	U3
10	Electrolytic Capacitor, 100μF, 50V	Nippon	C4
11	Electrolytic Capacitor, 220μF, 35V	Nippon	C5
12	Inductor, 18μH, 2A	Panasonic	L2
13	Electrolytic Capacitor, 100μF, 16V	Nippon	C6
14	Zener Diode, 4.3V, 1.5W	ON Semi	Z1
15	Resistor, 100E, 5%, 0.125W	Vishay	R1
16	Resistor, 1K, 5%, 0.125W	Vishay	R2

Table 3. Experimental results of single-phase flyback buck-boost converter at different load

I/P AC (V)	I/P AC (W)	O/P1 DC (V)	O/P1 DC (W)	O/P2 DC (V)	O/P2 DC (W)	Total (W)	Eff. (%)
5V@20mA and 20V@20mA							
75	0.767	5.122	0.1312	19.1	0.3648	0.4960	64.64
220	0.778	5.128	0.1315	19.2	0.3686	0.5001	64.22
265	0.804	5.129	0.1315	19.2	0.3686	0.5002	62.18
5V@200mA and 20V@20mA							
75	2.308	5.077	1.0310	22.2	0.4928	1.5239	66.02
220	2.279	5.08	1.0323	22.4	0.5018	1.5340	67.32
265	2.302	5.08	1.0323	22.4	0.5018	1.5340	66.63
5V@200mA and 20V@200mA							
75	5.884	5.02	1.0080	19.7	3.8809	4.8889	83.09
220	5.935	5.047	1.0189	19.9	3.9601	4.9790	83.90
265	5.975	5.048	1.0193	19.8	3.9204	4.9397	82.67
5V@20mA and 20V@200mA							
75	5.238	5.111	0.1306	18.9	3.5721	3.7027	70.69
220	5.048	5.106	0.1304	18.8	3.5344	3.6648	72.60
265	5.176	5.106	0.1304	18.8	3.5344	3.6648	70.81

Table 4. Load and Line regulation details of single- phase flyback buck-boost converter at different load

Load Regulation (%)			Line Regulation (%)		
I/p(AC)	5V	20V	Load	5V	20V
75V	0.886	3.6	Nominal	-0.097	-0.495
220V	0.944	4.12	Full	0.039	3.6
265V	0.964	4.12			

8. Conclusion

The design of this single-phase flyback buck-boost AC-DC converter has been validated by simulation and test results. The results obtained have shown good output voltage regulation and improved efficiency close to 84% at full load conditions with much reduced output voltage ripple of 1% for 5V and 2% for 20V output. The converter shows good steady state performance from 10% to 100% loading conditions. The simulated and experimental results have revealed the improved performance of the proposed converter in low power applications. The current limiting feature has also been studied and implemented in this converter.

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