Algorithm and Design of Double-base Log Encoder for Flash A/D Converters

Nguyen-Minh Son, In-soo Kim, Jae-ha Choi, Jong-soo Kim

Abstract

This study proposes a novel double-base log encoder (DBLE) for flash Analog-to-Digital converters (ADCs). Analog inputs of flash ADCs are represented in logarithmic number systems with bases of 2 and 3 at the outputs of DBLE. A look up table stores the sets of exponents of base 2 and 3 values. This algorithm improves the performance of a DSP (Digital Signal Processor) system that takes outputs of a flash ADC, since the double-base log number representation does multiplication operation easily within negligible error range in ADC. We have designed and implemented 6 bits DBLE implemented with ROM (Read-Only Memory) architecture in a 0.18 μm CMOS technology. The power consumption and speed of DBLE are better than the FAT tree and binary ROM encoders at the cost of more chip area. The DBLE can be implemented into SoC architecture with DSP to improve the processing speed.

Keywords : Double-base Number System, Double-base Log Encoder, Flash ADC, TIQ ADC, DSP

I. Introduction

In recent emerging technologies such as wireless terminal devices, software defined radio, and bio-imaging applications, an insatiable need has arisen for higher performance DSPs. But the limitation of DSPs in real application results from their massive arithmetic operations. Therefore, number systems are often chosen to reduce the complexity of arithmetic, and consequently, allow DSPs' higher performance. Over the last two or so decades, logarithmic number systems (LNS) and double-base number systems (DBNS) [1-3] have been developed and proven the effectiveness in DSP algorithms. Any number can be expressed with the following DBNS,

$$X = \sum_{i,j}^{k,m} d_{ij} 2^i 3^j \qquad (1)$$

where $d_{ij} \in \{0,1\}$, $i \in (0,k)$ and $j \in (0,m)$ are independent integers. A 2-dimensional table will be used to illustrate the representation scheme as shown Fig. 1. Since *i and j* are independent, any number is represented as indices in 2 dimensions. The base 2 is on the x-axis, while the base 3 is on the y-axis. The details of DBNS can be well defined [1-7].

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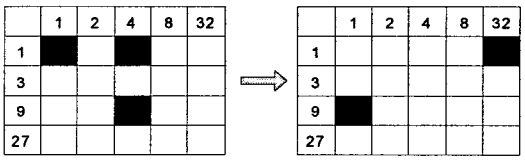


Fig. 1. DBNR and Greedy algorithm

In the 2 dimensional map, the multiplication can be done easily as shifting operation to right or down depending on the multiplier values. However, in case of addition of DBNS more processing steps are required, even though the addition is just overlapping DBNS numbers in the map. That is, the result of addition can yield multiple small squares in the map, if the added result can not be represented into one DBNS number. The Greedy algorithm was already developed to reduce multiple small squares as shown in Fig 1. But it is a NP problem [1-4], and some values can not be reduced into single value. Thus, many adders and stages are required to add such multiple squares [5-7]. Therefore, this study suggests a new DBLE to support real time signal processing in flash ADC, which is known as the fastest ADC.

II. Flash ADC and DSP

There were many efforts to design and implement a fast ADC at low power and chip area consumption in [10-16]. Fig. 2 describes the architecture of a simple DSP and a flash ADC using DBLE to convert analog signal to double-base log number system (DLNS). After

converting analog signals into digital signals based on TIQ (Threshold Inverter Quantization) voltage comparators, 0-1 generator circuits, which only activate one among the 2^n (n is the number od ADC bits) comparators, are the next stage [8-11]. Then, DBLE is followed instead of typical FAT tree or ROM based encoders.

The nature of the difficulty is that most A/D converters support only the binary number system. Thus, binary codes should be converted to DLNS codes to be used in the DSP which adopts different number systems such as DBNS. This requires additional circuitry, which results in lowering the performance of entire systems in terms of area, power consumption and speed. Thus, we give a new flash ADC with DBLE to enhance the operation speed of DSP circuits. This paper proposes a new methodology to encode analog inputs into DLNS codes without binary conversion for flash ADC embedded DSP systems as shown in Fig. 2. This approach eliminates additional circuitry in DSPs for converting binary codes to DLNS codes by directly outputting DLNS codes from flash ADCs. Design and comparison of a ROM type encoder with typical binary encoders verifies the proposed method.

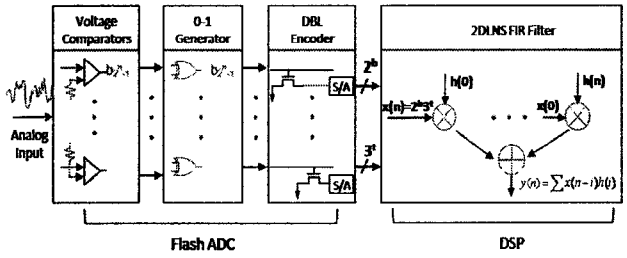


Fig. 2. Flash ADC and DSP

The remainder of this paper is organized as follows. In Section II, the basic idea of DLNS and the proposed algorithm are introduced. Section III gives the circuit implementation of 6 bits ADCs. In Section IV, we conclude with a summary and future works.

III. Double-base log Number System and Algorithm

The Log Number System (LNS) is useful for representing real numbers in computer and digital hardware. An arbitral number, X, represented by the logarithmic x has the following form in LNS;

$$X \rightarrow \{s,\ x = \log_b(|X|)\} \tag{2}$$

where s is a bit denoting the sign of X (s=0 if X> 0, s=1 if X< 0). The LNS can be expanded using the two bases of 2 and 3, called DLNS, as the modification of the DBNS [1-2]. That is, DLNS can be treated as a special case of DBNS. In other words, DLNS usually tries to use one term in representing any value X within allowable error range, while DBNS needs more term to represent any value X sometimes. In DLNS, a non-negative arbitral number y can be expressed with finite precision:

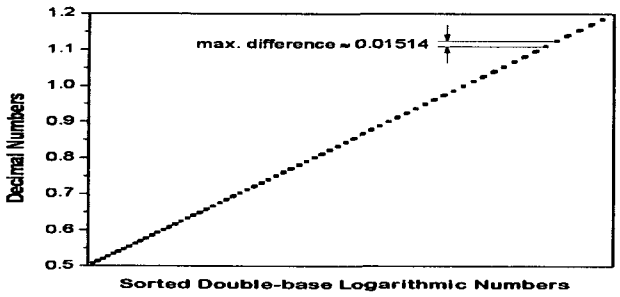
$$y \approx 2^b 3^t \tag{3}$$

where b and t are arbitrarily signed integers. This paper refers to b as the binary exponent and t as the ternary exponent. The precision of DNLS is defined as a half of the maximum difference between number y and 2^b3^t (DLNS representation). The precision of DNLS depends on the boundary of the exponents and the representing range of given numbers. As shown in Fig. 3, the precision of DLNS in the range of number of 0.5 ~1.2 is 0.00757 at 7 bits exponents, i.e. [-64, 64). The boundary of the exponents can be determined according to given error tolerance. The maximum error can be defined as the maximum difference between two contiguous DLNS representations. Thus the maximum difference is 0.01514 with 7 bits exponent boundaries in decimal values between 0.5 and 1.2. The maximum errors decrease exponentially as the boundary expands. Also, the boundary values can be determined to be as small as possible while satisfying the required ADC error tolerance. Fig. 4 shows the maximum errors of the numbers between 0.5 and 1.2 as the function of the boundary of the exponents.

Since LNS shows the effectiveness in floating point arithmetic, the expectation is to further reduce complexity in the digital filter design if filter inputs, generated by the A/D converter, are also real numbers. Furthermore, recent CMOS flash A/D converters use voltages from 0.5V to 1.2V as the analog inputs [8-11]. These voltage ranges can be easily represented by DLNS with small error rates as described earlier.

The set of b and t values can be found at the point that the difference between an analog input and a represented real number, y, is minimized. An example of a DBLE for a 6-bit A/D converter appears in Table 1. Notably, only 16 sets of the b and t values are present, rather than a full set of them. In this particular case, the boundary of the exponents is set to 2^9, i.e. [-256, 256), considering saturation of the maximum errors. Therefore, the outputs of the encoder can be designed

with 1 bit for sign and the remaining 8 bits for the number representation at 0.15 LSB (Least Significant Bit) error tolerance. The errors on average are only 0.053 LSB, which may be negligible considering the required linearity specification of ± 0.5 LSB in practical designs.



Pig 3. The precision of DNS

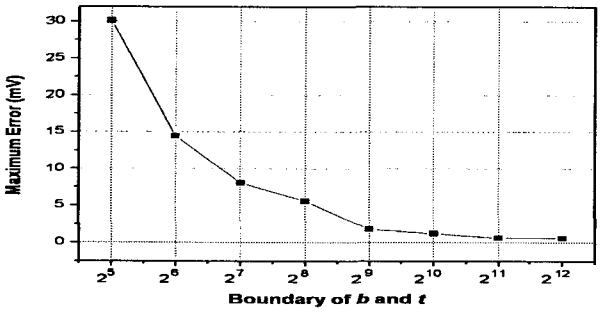


Fig 4. Maximum errors: A function of the boundary of b and t values

The results of table 1 has be obtained by conversion algorithm from analog input to DNLS code while accepting error tolerance. The pseudo conversion algorithm is described as follows:

1. Generate analog input into real number array
2. For each real number, find all pairs of binary and ternary, and its error rate
3. Find a set of minimum error rate at each real number input. Then, select only the maximum value of this set called error tolerance.
4. Choose pair of binary and ternary which error rate is less than error tolerance.

IV. Circuit Implementation and Simulation Results

The design and realization of the DBLE occurs with ROM encoder architecture in a 0.18 μm CMOS technology. The b and t values shown in the Table 1 can be easily implemented using a LUT (Look-Up Table) and a ROM array. In the DBLE using an NMOS ROM array, an analog input is digitized and converted to a thermometer code (TC) corresponding to the voltage level by the analog voltage comparators. The 0-1 generator produces a trigger signal for the ROM encoder from the TC; then, the ROM sends the preset binary values of the exponents to the Sense Amplifier. Fig. 5 presents the physical layout of DBLE using a 0.18 μm CMOS technology. Expectedly, the physical layout area is double that of typical binary ROM encoders because the DBLE uses both binary and ternary exponents. However, the maximum speed of the DBLE is 3 times faster than the binary ROM encoder, and is also faster up to 65% than the FAT tree encoder's speed. The speed of encoders depend on the load capacitance of each output pin [17-18]. The average load capacitance of each DBLE output is approximately 15% smaller than the binary ROM encoder's except the sense amplifiers, since the 565 gates of DBLE are distributed on 18 output pins, while the 222 gates of ROM are distributed on 6 pins. Therefore, the average power consumption of this encoder can be reduced according to the reduced load capacitance on the output pins. The area of this encoder is larger than the binary ROM and FAT tree encoders as shown in table 2, since this encoder needs more MOSFET gates than the ROM based and FAT tree encoders, even though it operates faster than the two types.

To verify the functionality of the DBLE design, authors supplied the output 01-generator to provide input for DBLE. Figure 6(a) and (b) show the HSPICE simulation output waveform of binary and ternary exponents of DBLE at 3.3Ghz frequency. In the waveform of Fig. 6, the output of 01-generator is shown at the top side, and 9 bits codes of binary and ternary exponents are in the remaining spaces. The MSBs are the upside and the LSBs are at the bottom side. This figure shows the correctness of output waveform of binary and ternary exponents of Table 1.

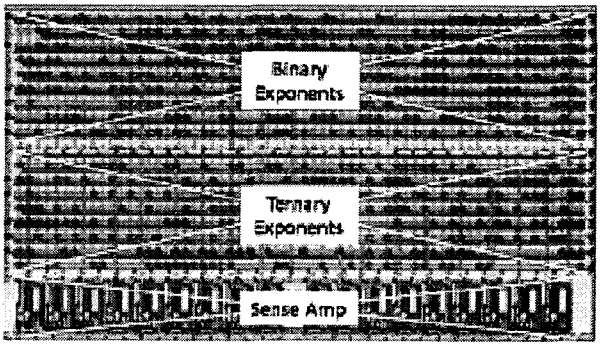


Fig 5. Physical layout of the DBLE

Table 1. Output of Conversion Algorithm

Input [mV]	DC*	b**	t**	CV***	Error [LSB]
550.00	1	-134	84	549.75	0.031
582.26	5	191	-121	582.18	0.010
614.52	9	115	-73	614.61	-0.011
646.77	13	207	-131	646.14	0.079
679.03	17	-186	117	678.59	0.055
711.29	21	-10	6	711.91	-0.077
743.55	25	-151	95	743.00	0.068
775.81	29	193	-122	776.24	-0.054
808.07	33	136	-86	808.45	-0.047
840.32	37	163	-103	840.23	0.011
872.58	41	190	-120	873.27	-0.085
904.84	45	-184	116	904.79	0.006
937.10	49	11	-7	936.44	0.081
969.36	53	206	-130	969.21	0.019
1001.61	57	-84	53	1002.09	-0.059
1033.87	61	195	-123	1034.99	-0.138
Average error (%)					0.053

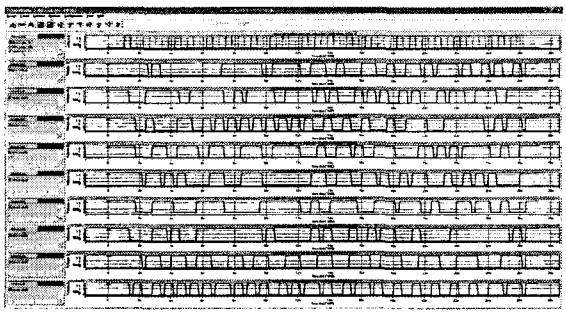
* digital values

** binary and ternary exponent values

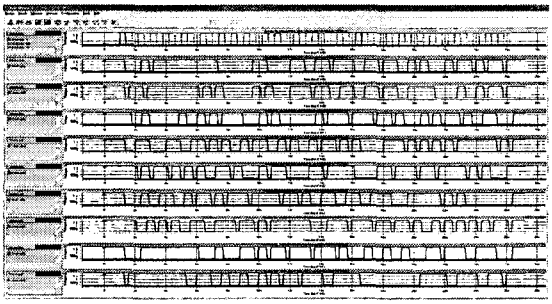
*** calculated decimal values with ** values

Table 2. - Layout Simulation Results

	DBLE proposed	Binary ROM encoder [9]	Fat tree encoder [9]
Technology	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.18 μm
Number of Bit	6	6	6
Max. Speed	3.3 GHz	1.11 GHz	2.00 GHz
Avg. Power	11.13 mW	32.64 mW	22.70 mW
Area	0.0161mm^2	0.0094mm^2	0.0074mm^2



(a) Output waveform of binary exponent



(b) Output waveform of ternary exponent

Fig 6. Output waveform of DBLE layout.

V. Conclusion and Future Work

This paper introduces a novel encoder algorithm and design based on DLNS for flash ADCs. The algorithm has been implemented in a 0.18 μm CMOS technology. The performance of the DBLE has been compared with typical binary encoders, and the results show better performance in speed and power consumption factors. The generated DLNS output can be easily processed in DSP circuitry due to simple operational characteristics. Future work will deal with incorporating multiplication and addition circuits to show the effectiveness of DLNS in DSPs at the same size of bit configuration. Besides, the processing speed and chip area of multiplication circuits based on the DLNS will be compared with more faster multipliers. Also the speed, area, and power consumption factors of the typical binary and the DBLE will be compared and analyzed.

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