High Security FeRAM-Based EPC C1G2 UHF (860 MHz-960 MHz) Passive RFID Tag Chip

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The metal-ferroelectric-metal (MFM) capacitor in the ferroelectric random access memory (FeRAM) embedded RFID chip is used in both the memory cell region and the peripheral analog and digital circuit area for capacitance parameter control. The capacitance value of the MFM capacitor is about 30 times larger than that of conventional capacitors, such as the poly-insulator-poly (PIP) capacitor and the metal-insulator-metal (MIM) capacitor. An MFM capacitor directly stacked over the analog and memory circuit region can share the layout area with the circuit region; thus, the chip size can be reduced by about 60%. The energy transformation efficiency using the MFM scheme is higher than that of the PIP scheme in RFID chips. The radio frequency operational signal properties using circuits with MFM capacitors are almost the same as or better than with PIP, MIM, and MOS capacitors. For the default value specification requirement, the default set cell is designed with an additional dummy cell.

Keywords: Passive RFID tag, FeRAM, EEPROM, MRAM, PRAM, MFM, PIP, MIM, CLK, demodulator, modulator, POR, voltage multiplier, Schottky diode.

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I. Introduction

Nonvolatile ferroelectric random access memory (FeRAM) products combine fast accessing read and write performance, nearly unlimited write endurance, and low power consumption [1]. The technical performance of the conventional nonvolatile electrically-erasable programmable read-only memory (EEPROM) and flash technologies [2] with high voltage, high current, and slow writing time is compared with that of FeRAM technologies in Table 1. The conventional PMOS based EEPROM cell is composed of three PMOS transistors and one poly-insulator-poly (PIP) capacitor with an industry-standard complementary metal oxide semiconductor (CMOS) process.

A one-transistor one-capacitor (1T1C) or two-transistor two-capacitor (2T2C) FeRAM cell is fabricated with a ferroelectric crystal film between two electrode plates to form a metal-ferroelectric-metal (MFM) capacitor, similar in construction to a DRAM capacitor as shown in Fig. 1. An MFM capacitor is placed over CMOS base layers with two additional process integration steps. Rather than storing data as a charge on the capacitor as volatile DRAM do, FeRAM stores the polarized charge data within the ferroelectric crystal. When an electric field is applied to a ferroelectric crystal the central ion atom moves in the direction of the electric field. As the ion atom moves within the crystal, it passes through an energy barrier. Its speed is faster than 3 GHz, and for all intents and purposes, it does not wear out. These properties make it adequate to write data at sufficient short time intervals to ensure the proper state is saved. A sense-amplifier circuit amplifies the bitline sensing voltage induced by the charge spike of the FeRAM cell caused by a charge displacement current at the two electrode plates of the MFM capacitor. If the electric field is removed from the

Table 1. Comparison of RFID nonvolatile memories.

Nonvolatile memories	Flash-type	PMOS 3T1C-EEPROM	1T1C-FeRAM
Cell size (μm^2 @ geometry)	0.5 @ 0.13 μm	4 @ 0.13 μm	1.5/0.75 @ 0.13 μm
Cell structure	1T	3T (PMOS) + 1C (PIP/MIM)	2T2C/1T1C
Additizonal masks to CMOS baseline	6-10	2 (PIP/MIM)	2 (MFM)
Program time (μs)	20 per word	300	0.02
Erase time (ms)	10	5	-
Program voltage/current	12 V / 12 mA	7 V / 10-20 μA per cell	1.5 V / < 0.01 μA per cell
Erase voltage	12-15 V	12 V	-
Endurance (cycle)	20k	20k	Unlimited
Data retention	10 years @ 85°C	10 years @ 85°C	10 years @ 85°C

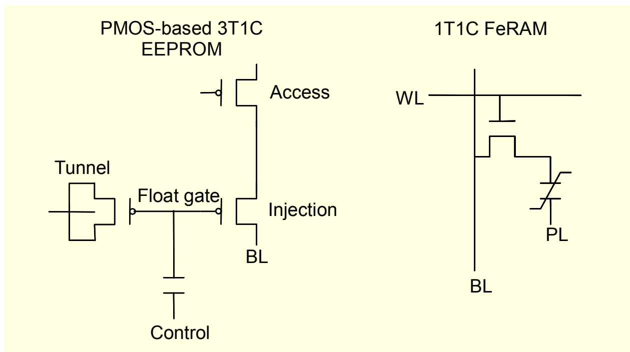


Fig. 1. PMOS-based EEPROM cell and FeRAM cell.

crystal, the central ion atom stays in position, preserving the state of the memory. Therefore, the nonvolatile FeRAM memory needs no periodic refreshing as DRAM memory does.

Fujitsu, TI, and Panasonic are developing FeRAM-embedded smart chips for contactless RF systems by taking advantage of FeRAM technologies. FeRAM is more resistant to data corruption by electric fields, radiation, and so on. It also offer state-of-the-art security functions. The extremely fast write times make it difficult for attackers. This avoids data-tearing, which is the partial writing of data which occurs when EEPROM-based smart ICs are removed from the RF field power source during a write cycle. Lower power consumption FeRAM make it a more difficult target to attack using differential power analysis techniques. Fujitsu's high-capacity 64 KB FeRAM-embedded RFID tag delivers high-speed data writing capability and high durability. It also meets fire retardant standards by satisfying the testing requirements for high-quality aviation parts.

Table 2. Characteristics of alternative nonvolatile memories for RFID tag chips.

	FeRAM	EEPROM	MRAM	PRAM
Cell structure				
1-bit cell write power (D/R=0.1 μm)	< 0.1 pW	> 0.1 mW	> 0.1 mW	> 1.0 mW
Write/read distance	write=read	write<read	write<read	write<read
RF capacitor	○	×	×	×
Sensor devices (MEMS, μPump, μMotor)	○	×	×	×

II. Chip Design Scheme and Measured Results

There are several alternative nonvolatile memories for RFID tag chips [3], [4] as shown in Table 2. The power consumption of EEPROM, MRAM, and PRAM in write mode is much higher than that in read mode. Especially in RFID tag chips, FeRAM is superior to EEPROM in terms of layout area and power consumption. The writing time for one byte of data on an FeRAM-embedded RFID tag chip is less than 100 ns with a low voltage of 1 V and low power consumption of less than 1 μW, unlike the large area charge pumping circuit for the high-voltage write operation in EEPROM. While the alternative nonvolatile memories of EEPROM, MRAM, and PRAM have higher power consumption in write mode than in read mode, the power consumption of FeRAM is the same in write mode and read mode. The energy consumption of FeRAM is less than 1% of that of EEPROM and is more suitable for long distance wireless communication. It is generally believed today that FeRAM is not cost-effective due to its large cell size in a high-density standalone memory; however, our study demonstrates that the FeRAM-embedded RFID tag chip is more cost-effective than any other memory-embedded RFID tag chip.

Compared to other memory technologies, FeRAM technology can be easily integrated with any process technology, such as CMOS, bipolar, and the like, with little additional process overhead. The nonvolatile memory density in RFID tag chips is about 512 bits; therefore, a major potion of the memory layout area is not on the memory cell array area itself. Rather, it is on the peripheral circuits, such as the high-voltage boosting charge pump circuits and control circuits. The peripheral circuit area of FeRAM is very small because there are no additional high voltage pump circuits as there are in EEPROM. The FeRAM1T1C or 2T2C FeRAM cell

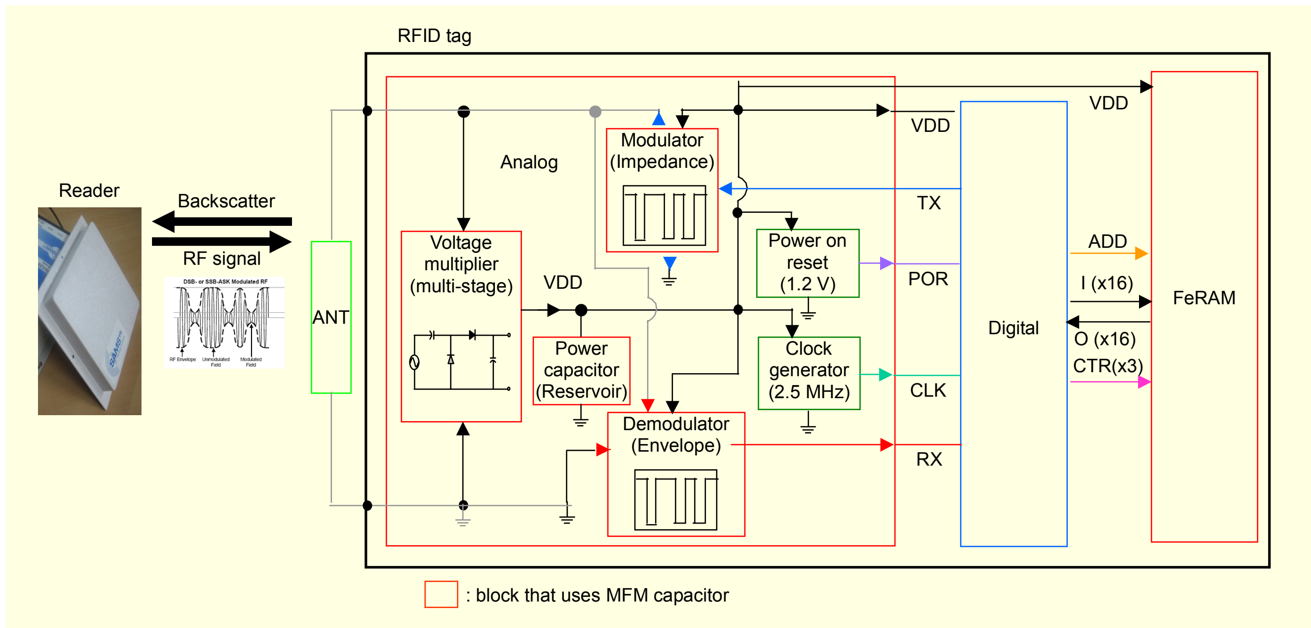
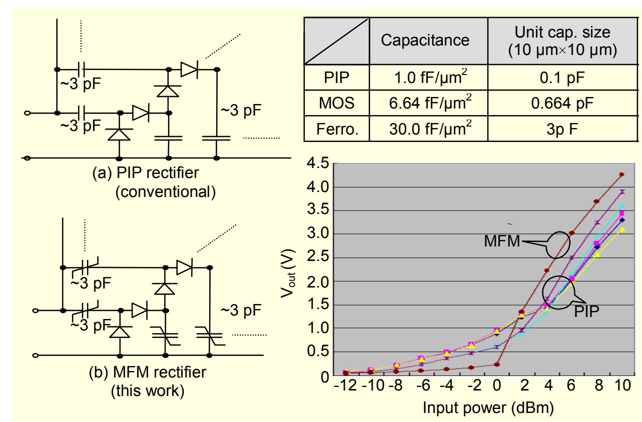


Fig. 2. Block diagram of the FeRAM-embedded RFID chip.

comprises a selecting switch device and the nonvolatile MFM charge-storing capacitor. The MFM capacitor in the FeRAM-embedded RFID chip is used in the memory cell region and in the peripheral analog and digital circuit area for capacitance parameter control. The capacitance value of the MFM is about 30 times larger than that of conventional capacitors, such as the PIP capacitor and the metal-insulator-metal (MIM) capacitor. MFM capacitors used for analog parameters are directly stacked over the analog and memory circuit region without consuming additional silicon area for capacitor implementation. Thus, the proposed stacked MFM technology is very cost-effective for implementing the EPC class-one generation-two (C1G2) 860 MHz-960 MHz ultra-high frequency (UHF) band RFID tag chip.

Figure 2 is a block diagram showing the implementation of the FeRAM-based RFID chip. The FeRAM-based RFID chip includes a digital block coupled between an analog block and a FeRAM block. The demodulator is configured to detect operation command signals from the transmission frequency signal, and a modulator circuit is configured to transmit requested information to the antenna. The power at the reset (POR) circuit is configured to generate a reset signal by detecting the RFID supply voltage VDD of 1.2 V. The clock generator (CLK) is configured to generate a clock signal of 2.5 MHz. The digital block is in communication with the FeRAM memory via address signals [5:0], data-out (×16), the data-in (×16) bus, the control signals of chip enable (CE), output enable (OE), and write enable (WE). A memory cell array of 4 banks, namely, RESERVED, electronic product code (EPC), transponder ID (TID), and USER, has 512 cells



	Capacitance	Unit cap. size (10 μm×10 μm)
PIP	1.0 fF/μm^2	0.1 pF
MOS	6.64 fF/μm^2	0.664 pF
Ferro.	30.0 fF/μm^2	3p F

Fig. 3. Comparison of the conversion properties of MFM and PIP capacitors in the voltage multiplier block and the demodulator circuit block.

arranged in 32 rows by 16 columns.

Figure 3 compares the electrical properties of the MFM and PIP capacitors used in the voltage multiplier block and the demodulator circuit block. The conventional voltage multiplier comprises multi-stages of PIP or MIM capacitors of 3 pF each and Schottky diodes measuring 3.6 μm×20 μm. The proposed voltage multiplier is only composed of multi-stages of MFM capacitors of 3 pF each and Schottky diodes measuring 3.6 μm × 20 μm. The voltage multiplier with 6-stage rectifiers is configured to generate power VDD of 1.0 V to 2.0 V for the RFID chip. The energy transformation efficiency using the MFM scheme is higher than that of the PIP scheme when the generated output voltage is around 1.2 V.

At the target voltage of 2.0 V, the MFM scheme has more

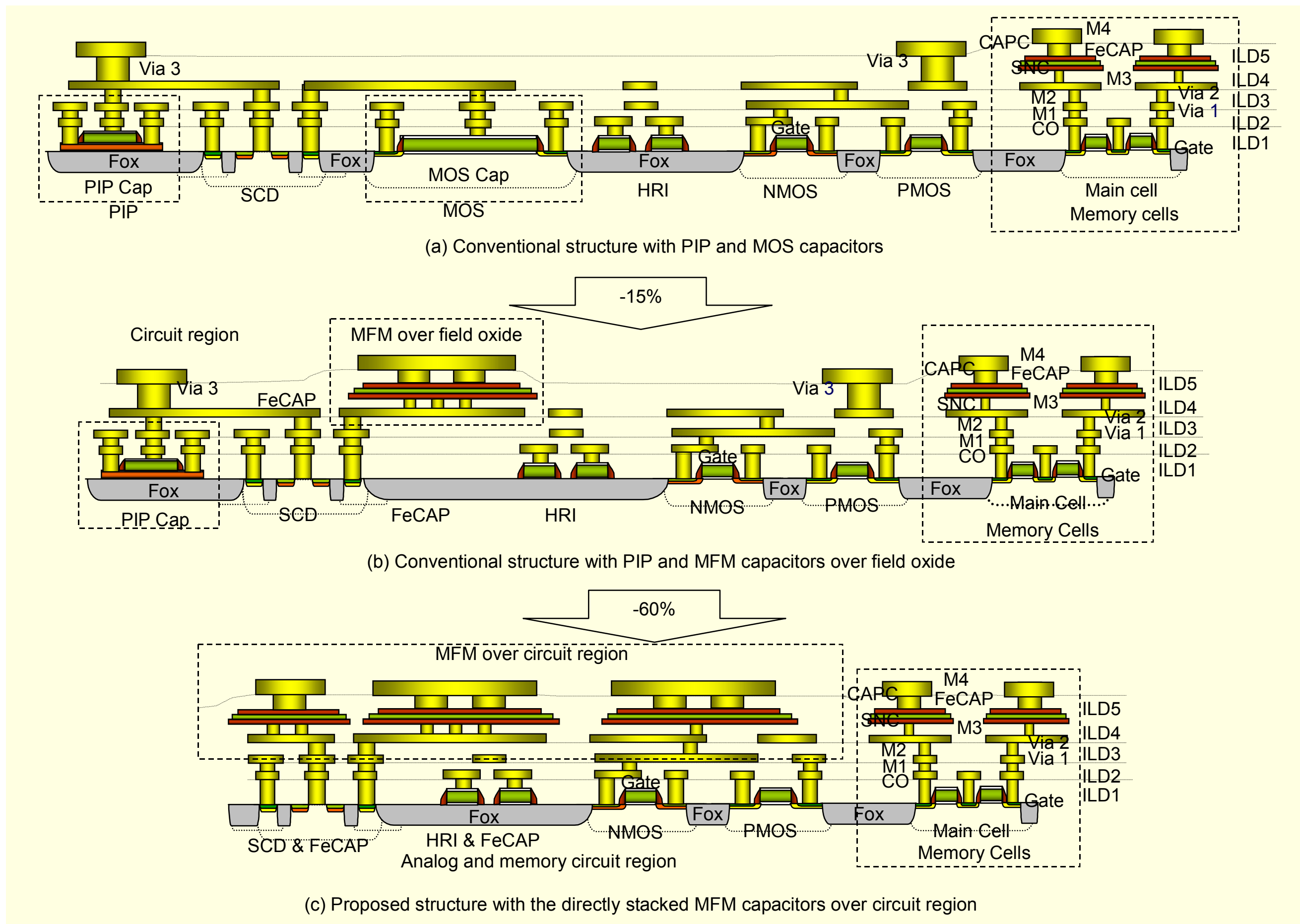


Fig. 4. Comparison between the conventional PIP structure and the MFM structure directly stacked over the circuit region.

efficient conversion properties in generating the power of RFID chip. The capacitance values of the voltage multiplier with 6-stage rectifiers, the demodulator with 5-stage rectifiers, the modulator, and the VDD power reservoir capacitor are 36 pF, 3 pF, 10 pF, and 300 pF, respectively. The total capacitance needed in the RFID chip is around 300 pF. The estimated capacitor layout area for the capacitance of 300 pF is relatively small, that is, 10,000 μm^2 with MFM compared to 300,000 μm^2 with PIP. The detailed design of the directly stacked MFM scheme is shown in Fig. 4. In the original design, conventional PIP and MOS structure design technology cannot share the layout area with the circuit region because the circuit region uses layers on the same level as the PIP and MOS capacitors. In the second design method, non-stacked PIP and MFM capacitors on the field oxide region also cannot share the layout area with circuit region, but because of the high capacitance of the MFM capacitor, the chip size is reduced by about 15%. In the final method, the MFM capacitor directly stacked over the analog and memory circuit region can share the layout area with the circuit region; thus, the chip size is reduced by about 60%. Figure 5 shows the layout design

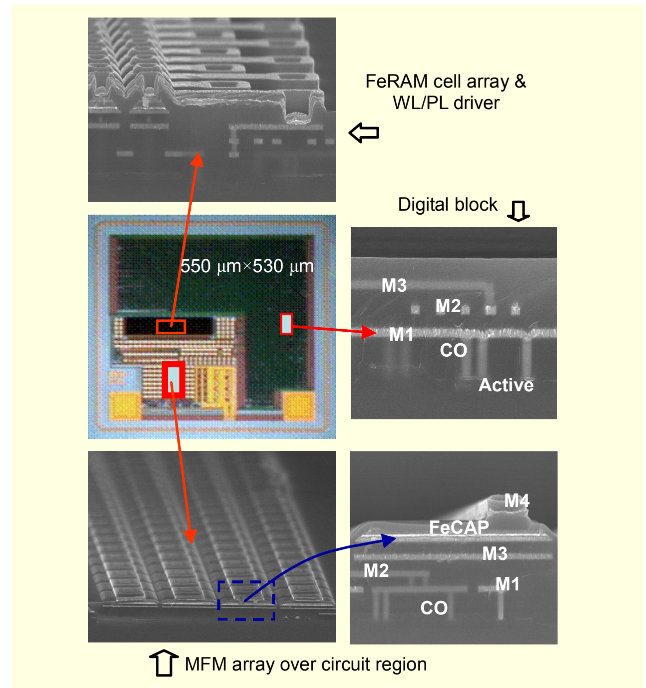
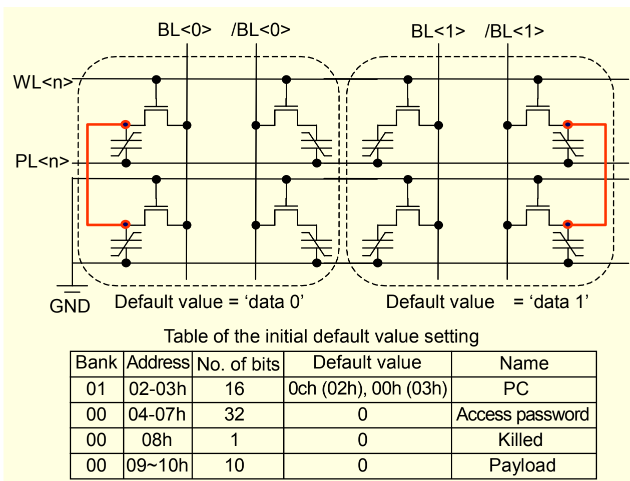


Fig. 5. Structural details of the MFM capacitor for RFID chips.



Bank	Address	No. of bits	Default value	Name
01	02-03h	16	0ch (02h), 00h (03h)	PC
00	04-07h	32	0	Access password
00	08h	1	0	Killed
00	09~10h	10	0	Payload

Fig. 6. Memory scheme to set default cell values.

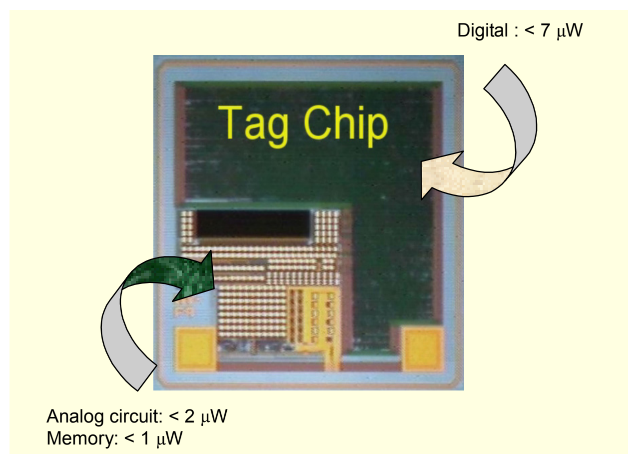


Fig. 8. Measured read and write power consumption of FeRAM-embedded RFID chip.

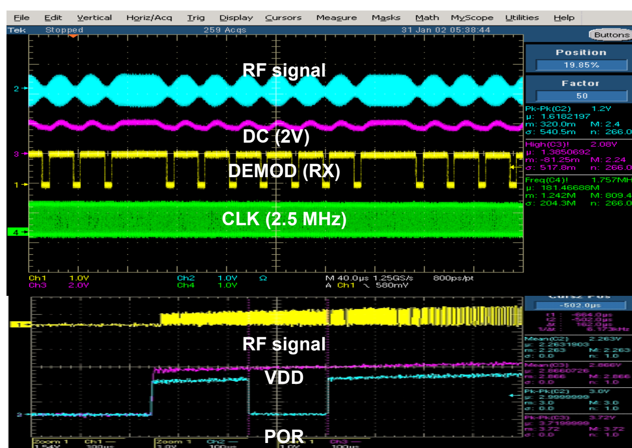


Fig. 7. Measured RF signal data of an RFID chip.

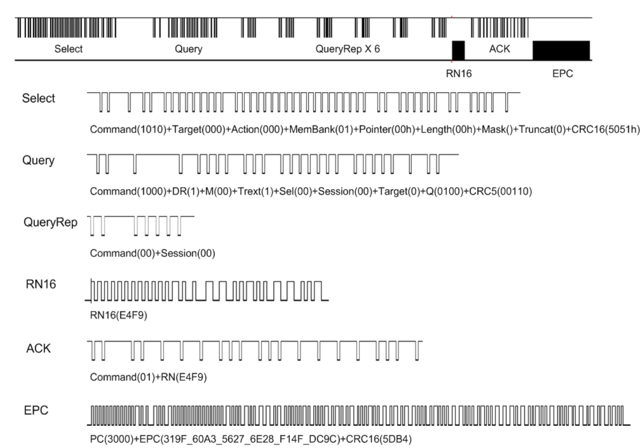


Fig. 9. RFID tag identification sequence.

details of the MFM structure in the RFID chip. The MFM capacitors are shown to be stacked over the analog, digital, and memory block region without additional layout area burden. On the other hand, the EPC C1G2 specification of the RFID chip requires the initial default data values in some addressing cells. There are two methods to set the initial default data values. In one method, all the initial default data values are set to 0. In the other method, some initial default data values are set to 0 and others are set to 1. Figure 6 shows the default cell setting scheme for PC, access password, killed, and payload values at the initial manufactured chip state.

Some bits are designed to be set to 0, and others are set to 1 in initial access mode. In normal operation, the set data can be changed. For the default value specification requirement, the default set cell includes an additional dummy cell. The word line (WL) and plate line (PL) of the dummy cells are fixed to the ground voltage. The dummy cell capacitor is connected to the main cell capacitor through the bottom layer (BL) of the cell capacitor. If the dummy cell capacitor is connected to the cell capacitor of the BL then the default value of the bit is 0. On the other hand, if the dummy capacitor is connected to the cell capacitor of the BL, then the default value of the bit is 1. The measured RF signal of some analog circuit blocks of the RFID chip is shown in Fig. 7.

The RF operational signal properties using circuits with MFM capacitors are almost the same or better than with PIP, MIM, and MOS capacitors. For example, the power voltage stability with an MFM reservoir capacitor is almost the same as that with an MOS transistor. The generated VDD power and clock pulse are stabilized above around 100 μs and 200 μs above the POR detection level of VDD 1.2 V. In general, the power consumption of an RFID tag chip should be less than 30 μW. The measured power consumption of the FeRAM-embedded RFID chip is about 10 μW, which includes 1 μW, 2 μW, and 7 μW, which are the total power dissipation values of the memory, analog, and digital circuit blocks, respectively, as shown in Fig. 8. The low power consumption is mainly a result of those circuit schemes, such as the low-current and

Table 3. Measured performance results of FeRAM-based RFID tag chip.

Memory type	FeRAM	EEPROM
Protocol	EPC Class1 Gen.2	-
Operation frequency	860 MHz - 960 MHz	-
Modulation (forward)	ASK	-
Power consumption	≤ 15 μW @ 1.5 V rectifier & 1.5 V programming	≤ 30 μW @ 2.0 V rectifier & 14 V programming
Data rate (forward)	40/80/160 kbps	-
Data rate (return)	40 - 640 kbps	-
Memory capacity	512 bit (4 bank)	-
Communication range	Read: >3 m (1 μW), Write: >3 m (1 μW)	Read: >3 m (2 μW), Write: >1 m (7 μW)
Technology	0.25 μm CMOS logic	-
Chip size	0.5 mm × 0.5 mm	0.8 mm × 0.8 mm (large area due to EEPROM programming)
RF identification test	Passed	-
Protocol identification test	Passed	-

low-voltage operation of the FeRAM cell in the memory block, the high resistance passive-elements-assisted low-current circuits in the analog block, and the low-power clock-control scheme in the digital block.

An RFID tag identification sequence is shown in Fig. 9. The upper signal streams are from the reader, and the lower signal streams are from the FeRAM-based RFID tag chip. A Select command is transmitted to the RFID tags, followed by a Query command, and a QueryRep command is repeated until the RN16 response is detected. After RN16 is detected by the reader, an ACK signal is transmitted to the RFID tag. Finally, EPC data is collected by the reader from the RFID tag.

The measured performance results of the FeRAM-based RFID tag chip are summarized in Table 3.

III. Conclusion

The total capacitance needed in an RFID chip is around 300 pF. The estimated capacitor layout area with MFM is relatively small, taking up just 10,000 μm^2 compared to 300,000 μm^2 with PIP. For a more cost-effective layout in terms of chip size, MFM is directly stacked over the analog, digital, and memory circuit region without electrical performance degradation. In the default memory cell value setting scheme, the default value setting cells include additional dummy cells which are connected to the main cell capacitors through the bottom layer of the cell capacitor. The measured power consumption of the FeRAM-embedded RFID chip is about 10 μW, and the transponder distance is between 4 m and 7 m.

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Suk-Kyoung Hong is a senior member of technical staff at Hynix Semiconductor Inc., Korea. Since 1997, he has worked on the development of FeRAM and PRAM. He received his BS in metallurgy in 1982 from Kookmin University, his MS in 1986 from Korea Advanced Institute of Science and Technology (KAIST), and his PhD in 1997 from Seoul National University, Korea, in materials science and engineering. From 1986 to 1997, he worked as a thin film device manager at Samsung Electronics Co., Ltd., Korea.

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