

Retina-Motivated CMOS Vision Chip Based on Column Parallel Architecture and Switch-Selective Resistive Network

Jae-Sung Kong, Hyo-Young Hyun, Sang-Ho Seo, and Jang-Kyoo Shin

A bio-inspired vision chip for edge detection was fabricated using 0.35 μm double-poly four-metal complementary metal-oxide-semiconductor technology. It mimics the edge detection mechanism of a biological retina. This type of vision chip offer several advantages including compact size, high speed, and dense system integration. Low resolution and relatively high power consumption are common limitations of these chips because of their complex circuit structure. We have tried to overcome these problems by rearranging and simplifying their circuits. A vision chip of 160×120 pixels has been fabricated in $5 \times 5 \text{ mm}^2$ silicon die. It shows less than 10 mW of power consumption.

Keywords: CMOS vision chip, resistive network, low power consumption, high resolution.

I. Introduction

Technology improvements in semiconductor processes and complementary metal-oxide-semiconductor (CMOS) image sensors (CIS) have led to the development of smart vision sensors, which consist of silicon-based photodetectors and analog/digital signal processing circuits [1], [2]. One such development is the CMOS vision chip for edge detection based on a resistive network, proposed by Mahowald and Mead [2], [3]. The functions of their photoreceptors, horizontal cells, and bipolar cells are modeled on the biological retina. All their operations are carried out in a parallel manner; thus, the final information can be obtained in real-time by integrating all the mentioned functions on a single chip.

The most common limitation of this type of vision chip is low resolution because its unit-pixels consist of many circuits for photosensing, signal processing, and noise suppression. In particular, several capacitors for the storage of analog signals contribute most to low resolution. Simplification of circuits, layout optimization, enlargement of chip size, and rearrangement of circuits have been considered as possible solutions [4], [5]. Rearranging circuits by using column parallel architecture might also be the best approach in terms of resolution improvement and cost. The simplification of circuits might also be a good solution. Vision chips for edge detection require a resistive network for the function of Gaussian filtering in digital image processing and a specialized circuit structure for the acquisition of both raw and smoothed images. These circuits require many metal-oxide-semiconductor field-effect-transistors (MOSFET); thus, it causes additional area consumption, power dissipation,

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Jae-Sung Kong (phone: +82 53 940 8631, email: kongjs@ee.knu.ac.kr), Hyo-Young Hyun (email: hyoungyed@nate.com), Sang-Ho Seo (email: bari79@ee.knu.ac.kr), and Jang-Kyoo Shin (phone: +82 53 950 5531, email: jkshin@ee.knu.ac.kr) are with the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Rep. of Korea.

and noise. Previously, two structures have been used, a voltage division structure based on horizontal and vertical resistive circuits [6] and a circuit structure using two analog buffers [7], [8]. These structures have their own structural disadvantages in terms of power and area consumption, signal aliasing and additional noise. To overcome these problems, we propose a switch-selective resistive network (SSRN). The SSRN uses a common buffer for both raw and smoothed images.

Column parallel architecture and SSRN have been tried [9], but the vision chip suffered from an electrical problem due to the sensitive structure of the resistive circuit and the low frame rate. The electrical problem was caused by leakage current of a gate/N-well tied MOSFET in the resistive circuit. The leakage current deteriorates the symmetry of the output swing. Operational problems result from the data bottleneck between a two-dimensionally arranged sensor array and a one-dimensionally arranged analog signal processor. It extends the frame time to approximately one minute; therefore, the practical application of this approach is limited. In this paper, we have tried to solve these problems by using reset control and a VDD/N-well tied MOSFET in the resistive circuit.

II. Theory

1. Edge Detection Mechanism of a Biological Retina

Photoreceptors, horizontal cells, and bipolar cells in a biological retina are related to edge extraction [10]. Figure 1 shows the signal flow of those cells. The information falling on the photoreceptors is not sent directly to the brain through the optic nerves; rather, it is first processed in a number of ways by a variety of interactions among neurons within the retina.

Figure 2 shows a simple example of edge extraction. The x-axis represents the position, and the y-axis represents the

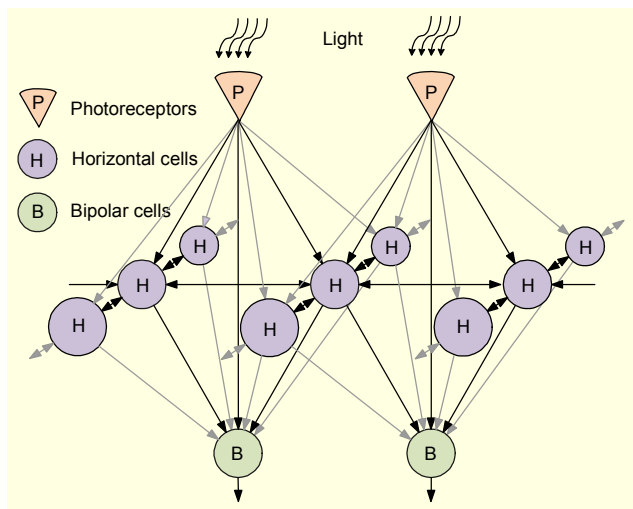


Fig. 1. Signal flow in a biological retina.

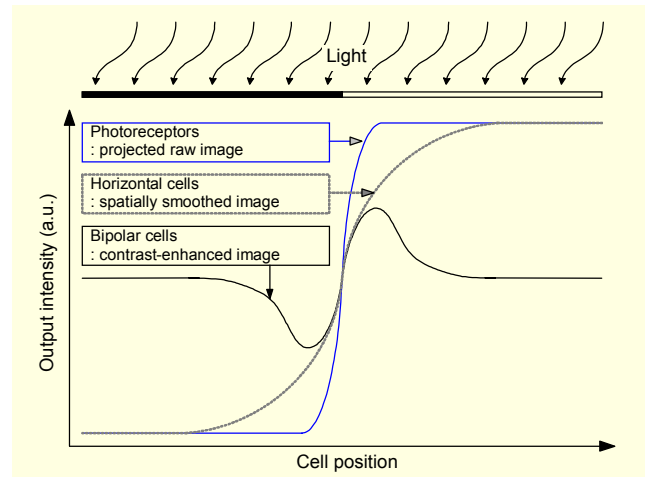


Fig. 2. Simple example of edge extraction.

normalized outputs of the photoreceptors, horizontal cells, and bipolar cells. If a bright light is projected only on the right side of the photoreceptor array, each photoreceptor sends a high-level signal. On the other hand, when a dim light is projected on the left side of the photoreceptor array, each photoreceptor sends a low-level signal. Horizontal cells receive signals from the photoreceptors and spatially smooth them. Edge signals resulting from the differences between outputs of photoreceptors and horizontal cells are yielded through the bipolar cells.

2. Modeling of a Retinal Structure in Electrical Devices

In a retina, photoreceptors, horizontal cells, and bipolar cells are the three key elements for edge extraction. First, raw image data is necessary. Because of on-chip integration, CIS technology is used for a CMOS vision chip instead of charge-coupled devices (CCD) [1]. The function of horizontal cells can be realized using a resistive network proposed by Mead [2]. All photodetectors in a chip are connected horizontally and vertically through resistive circuits to build the resistive network. The current flows, which move from higher potential areas to lower potential areas, contribute to smoothing. Smoothing is carried out in a spatially parallel manner; therefore, the mechanism is suitable for real-time applications. In this type of vision chip, the electrical property of the resistive network is the most important parameter for characterizing the final output. The function of the bipolar cells can be realized using differential circuits. In addition, noise reduction and addressing circuits are required for practical design.

III. Circuit Design

1. Unit Pixel

Figure 3 shows the circuit schematic of a designed unit pixel.

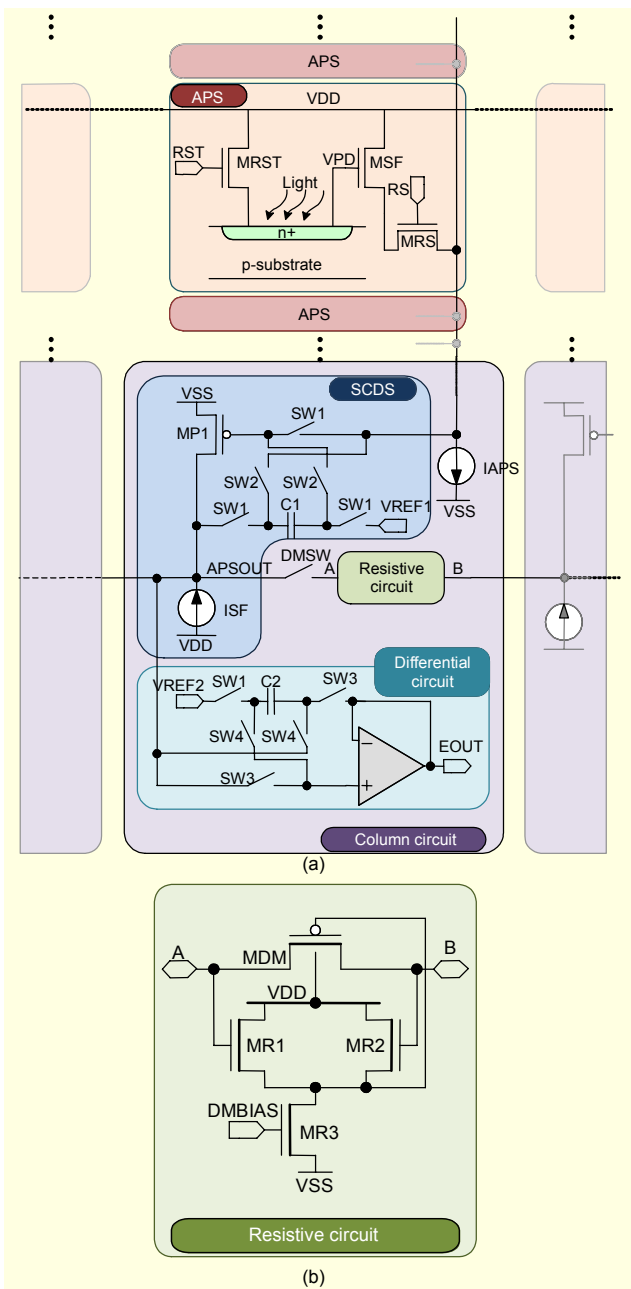


Fig. 3. Circuit schematic of the proposed unit pixel: (a) unit pixel and (b) a resistive circuit based on a VDD/N-well tied MOSFET.

The circuit contains an active pixel sensor (APS) to capture images, two simplified correlated-double-sampling (SCDS) circuits to reduce fixed pattern noise (FPN) and yield the difference between raw and smoothed image data, and a pixel-level adaptive resistive circuit (PLARC), which consists of four MOSFETs. The PLARC comprises an electrically stable VDD/N-well tied MOSFET and a biasing circuit; thus, it could reduce current leakage and unexpected electrical problems.

Figure 4 shows a timing diagram to control the proposed circuit.

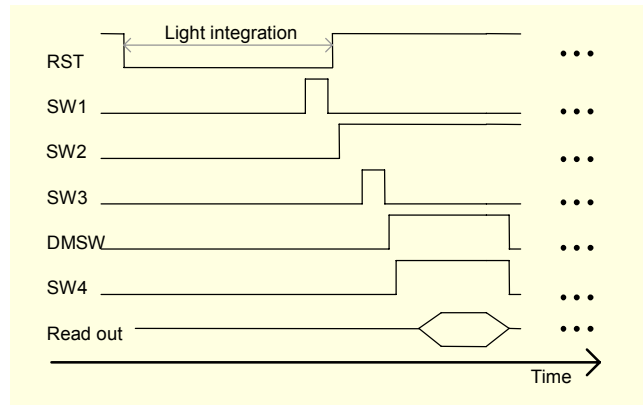


Fig. 4. Operation timing diagram.

Three-transistor APS and SCDS circuits are used for image capture and noise reduction, respectively. The photodiode capacitance is charged to a reset voltage by turning on the RST. During the integration time, electrons are accumulated in the photodiode capacitance according to the light intensity. After the integration time, the light signal is sampled when SW1 is turned on.

The sampled signal has FPN due to the mismatch of MOSFETs. To reduce the FPN, a correlated-double-sampling (CDS) technique is required. The SCDS method proposed by Kavadias is very effective for noise reduction [11]. The key advantage is that the circuit only requires one capacitor; therefore, area consumption can easily be minimized. Unlike SCDS, conventional CDS uses two capacitors to memorize both the image and reference signals. The light signal and reset signal are sampled when SW1 and SW2 are turned on, respectively, and then the reset signal is subtracted from the light signal.

The designed circuit has only one source follower for both raw and smoothed images. Each image can be selected by a switch, DMSW. This circuit structure is a so-called SSRN. This resistive network is built by connecting MP1/ISF source followers via resistive circuits (see Fig. 3(b)). When the DMSW is open, APSOUT sends a raw image from the APS and the SCDS. Otherwise, when the DMSW is closed, APSOUT sends a spatially smoothed image due to the distribution current through the resistive circuits. The distribution current flows from higher potential nodes into lower potential nodes, and it can be controlled by using DMBIAS. Because the output node for raw and smoothed images is the same, there is no additional noise due to MOSFET mismatch. The area consumption is also reduced because the added switch can be fabricated by using one MOSFET in very small area. The differential circuit extracts the edge signal from the raw and smoothed images by switching SW3 and SW4.

This SSRN has advantages in power consumption and area consumption. In analog CMOS chips, most power is dissipated

in the biasing circuits for chip operation. Compared with previous structures, such as the voltage-division type [6] and the two-buffer type [8], SSRN has fewer biasing circuits. For example, the voltage-division type requires one resistive circuit for the vertical direction and one for the horizontal direction. Each resistive circuit requires its own biasing circuit. The two-buffer type requires two buffers for raw and smoothed images. Each buffer requires its own biasing current. Those biasing circuits are required for every unit pixel. This indicates that the power consumption strictly increases according to the increase in resolution. Unlike the first type, SSRN requires only a horizontal resistive circuit; thus, one biasing circuit for a unit pixel can be eliminated. Unlike the second type, SSRN uses a common buffer for both raw and smoothed images.

To realize a resistive network, a proper resistive circuit is required. Mead proposed a resistive network using linear resistors. A linear resistor requires a large area when using a standard CMOS process; therefore, a new approach should be considered. A resistive circuit using a single MOSFET was also described in [8]. A single voltage was applied to the all the gates of the MOSFETs for its resistive circuits. The results showed information loss caused by regionally improper biasing [1].

The proposed resistive circuit is shown in Fig. 3(b). The circuit consists of four MOSFETs: MDM, MR1, MR2, and MR3. The source and drain nodes of MDM are connected between two neighboring pixels. The states of the source and drain are exchanged according to their node potentials. The biasing circuit, which comprises MR1, MR2, and MR3, maintains the source-gate potential difference at a particular level, although the source-drain potential difference is regionally varied. The uniform source-gate potential differences maintain the resistivity of the resistive circuits, which helps reduce information loss. In [9], a different type of resistive circuit using a gate/N-well tied MOSFET was applied to reduce the body effect in the resistive network. However, its experimental results showed seriously asymmetric output due to the leakage current in the process-sensitive resistive circuit. Figure 5 shows the current voltage characteristics of the PLARC. Compared with the characteristics of the previous resistive circuit in [9], the proposed resistive circuit shows electrically and optically stable properties. V_{DS} and I_{DS} are the source-drain potential difference and the current flow of the MOSFET MDM, respectively. The current variation shown in Fig. 5 is caused by the body effect, which results from the potential difference between the source node and the body node of the MOSFET MDM. By reducing the body effect, it is expected that the current uniformity can be improved. The size of the manufactured circuit is $13.5 \times 17 \mu\text{m}^2$ using a $0.35 \mu\text{m}$ standard CMOS process. Compared with a linear resistor,

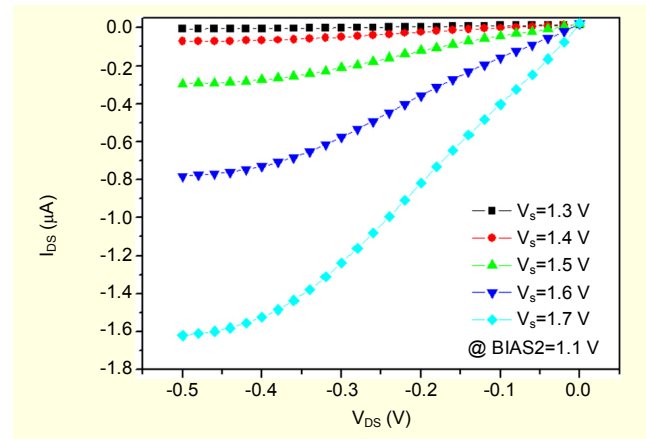


Fig. 5. I_{DS} - V_{DS} curves of the PLARC.

the PLARC requires a very small area. Compared with a single MOSFET, the data loss could be significantly reduced.

2. Column Parallel Architecture and Reset Control

Conventional vision chips are used to build a two-dimensional (2-D) resistive network for high operation speed and to mimic a more retina-like model [1], [2]. A unit pixel of this kind of chip contains a photodetector, a noise suppression circuit, resistive circuits, and a differential circuit. Both the noise suppression and the differential circuit require a capacitor for storage of analog data; therefore, the unit pixel requires a large area. Consequently, this type of vision chip suffers from a critical lack of resolution [1]. It was proposed as an attempt to solve the problem of low resolution by rearranging the circuits for photosensing and image processing. The signal processing circuits (SPC) were separated from the photosensing circuit, and then the SPCs were used in row-parallel. This arrangement has two advantages, namely, high resolution and low power dissipation. High resolution is due to the small size of the unit pixel. The power dissipation is low because there are fewer current paths through the overall chip. Possible disadvantages are data loss and low operation speed. Data loss can appear at the horizontal or vertical edge depending on the direction of the resistive network. However, the problem can be compensated when the resolution is sufficiently improved. The other disadvantage is low operation speed due to the data bottleneck problem. One attempt to solve this problem proposes using a reset control.

Figure 6 shows timing diagram for two methods of controlling vision chips. Without the reset control, a row data was achieved as a frame. This approach cannot effectively utilize SPC. The SP and RD for each row must not meet each other, but the electron charging operation (LI) of each APS can be performed in parallel. This control could be realized by

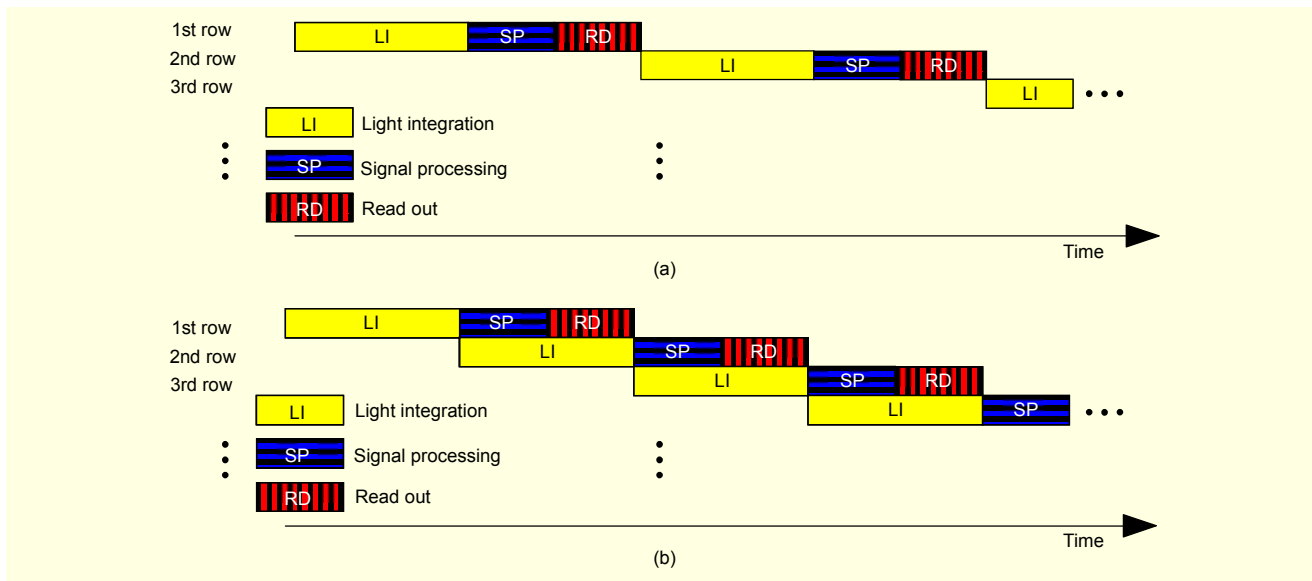


Fig. 6. Timing diagram: (a) without reset control and (b) with reset control.

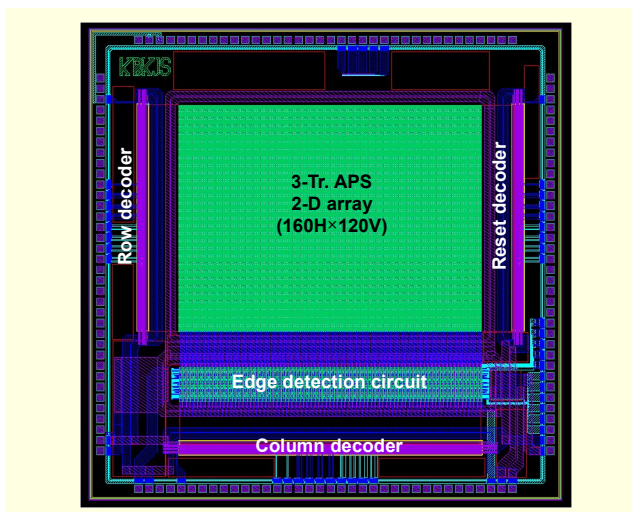


Fig. 7. Layout of the designed chip.

adding a decoder.

IV. Experimental Procedure

We fabricated a vision chip with a 160×120 pixel array using a $0.35 \mu\text{m}$ double-poly four-metal (2P4M) standard CMOS process. The chip size was $5 \times 5 \text{ mm}^2$. Figure 7 shows the layout of the chip. A data acquisition (DAQ) card and LabVIEW of the National Instrument Company were used to generate control signals and achieve an output signal. An optical lens (focal length 16 mm, f number 1.4) was mounted in a C-mount format to project an incident image onto the chip surface. The readout clock was 100 kHz. No external devices for output improvement were employed.

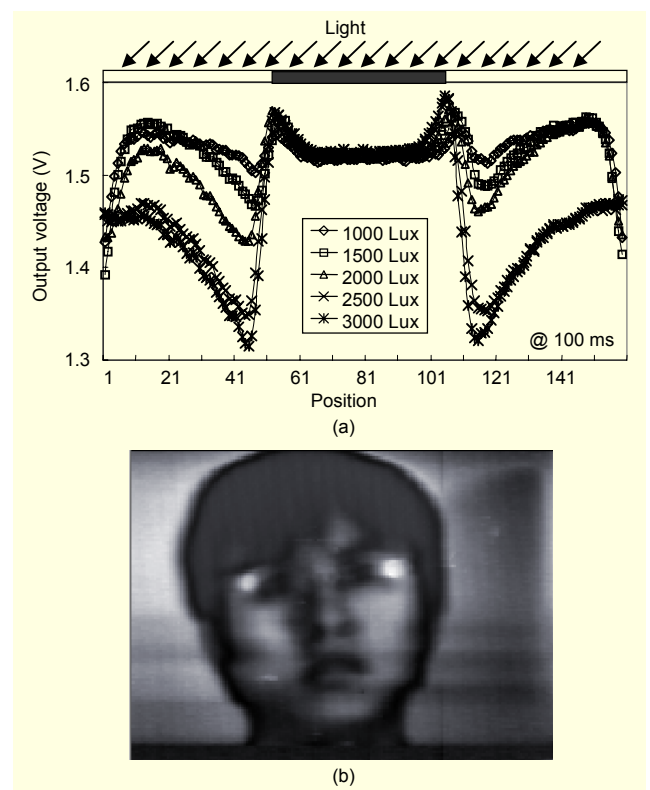


Fig. 8. Experimental results: (a) one-dimensional results under various light conditions and (b) a two-dimensional output image.

Figure 8 shows experimental results for the fabricated chip. The fabricated chip was evaluated under several illumination conditions. As shown in Fig. 8(a), the voltage at the non-edge region was approximately 1.53 V, and the value did not change

Table 1. Specifications of the proposed chip compared to chip presented in [4].

	Chip in [4]	Proposed chip
Process	Standard CMOS 0.35 μm double-poly four-metal process	
Die size	4 \times 4 mm ²	5 \times 5 mm ²
Resolution	128 (H) \times 128 (V)	160 (H) \times 120 (V)
Unit-pixel	21.3 \times 24.9 μm^2	20 \times 20 μm^2
Fill-factor	2.2%	35%
Supply voltage	3.3 V	3.3 V
Output swing	520 mV with an external amplifier	Over 250 mV peak-to-peak
FPN	80 mV (15.4% of V_{sat})	12 mV (4.8% of V_{sat})
Power consumption	-	Less than 10 mW

although the illumination condition changed. At the edge, the chip could send over 250 mV of peak-to-peak voltage swing, and the average measured FPN was 12 mV.

The output image was distorted at both sides of the edge detection circuit. For real applications, this distortion should be carefully considered. When this edge condition is strong, the diffusion current may overflow the entire resistive network; thus, signal aliasing could occur. To prevent this problem, the exposure time should be accurately controlled. Compared with the experimental results in [9], the swing of overshoot is close to the swing of undershoot. However, the output swing decreases and the average noise increases.

Figure 8(b) shows an output image of a human face. The gray scale represents the output voltage. White and black represent 1.26 V and 1.63 V, respectively. Power consumption could be optimized to less than 10 mW.

V. Conclusion

A bio-inspired vision chip was proposed for the computation of image information. It offers several advantages including compact size, high speed, low power dissipation, and dense system integration. Previously proposed vision chips suffer from low resolution and relatively high power consumption because of their complex circuit structure. Because of these problems, their applications have been limited to simple images. To overcome these challenges, column parallel architecture and SSRN were proposed and then realized using a standard CMOS process. Reset control can compensate the operation speed problem of the column parallel architecture. In addition, information loss can be suppressed by using the resistive network with PLARCs. A vision chip for edge detection with a 160 \times 120 pixel array was fabricated using a

0.35 μm 2P4M standard CMOS process. Its output was evaluated under several illumination conditions. From the results, we conclude that the proposed column parallel architecture can greatly improve the resolution at a minimum cost. Moreover, SSRN can effectively send raw and smoothed images with low power consumption and low noise. The fabricated chip may be implemented in several applications which require sufficient resolution, such as fingerprint recognition or iris pattern recognition. Furthermore, the fabricated chip could be used in mobile applications which require low power consumption, such as smart sensor systems.

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Jae-Sung Kong received the BE degree in electronic engineering from Kyungpook National University, Daegu, Korea in 2002, and the ME degree in electronics from the same university in 2005. He is now working for the PhD degree at Kyungpook National University. His current fields of interest are CMOS image

sensors, the bio-inspired vision chip, and its applications.



Hyo-Young Hyun received the BE degree in bio-industrial machinery engineering from Kyungpook National University, Daegu, Korea in 2005. He is now working for the ME degree at Kyungpook National University. His current field of interest is the CMOS vision chip and its applications.



Sang-Ho Seo received the BE degree in electronic engineering from Kyungpook National University, Daegu, Korea in 2002, and the ME degree in electronics from the same university in 2004. He is now working for the PhD degree at Kyungpook National University. His current field of interest is CMOS image

sensors.



Jang-Kyoo Shin received his BE degree in electronic engineering from Seoul National University, Seoul, Korea, in 1978, and the MS degree in electrical engineering from Korea Advanced Institute of Science and Technology, Korea, in 1980. He received the PhD degree in electrical engineering from Colorado State

University, Fort Collins, USA in 1991. He is now a professor in the School of Electrical Engineering and Computer Science at Kyungpook National University, Daegu, Korea. His current fields of interest are semiconductor sensors and intelligent sensor systems.