A Low-Voltage High-Performance CMOS Feedforward AGC Circuit for Wideband Wireless Receivers

Juan Pablo Alegre, Belén Calvo, and Santiago Celma

Wireless communication systems, such as WLAN or Bluetooth receivers, employ preamble data to estimate the channel characteristics, introducing stringent settling-time constraints. This makes the use of traditional closed-loop feedback automatic gain control (AGC) circuits impractical for these applications. In this paper, a compact feedforward AGC circuit is proposed to obtain a fast-settling response. The AGC has been implemented in a 0.35 µm standard CMOS technology. Supplied at 1.8 V, it operates with a power consumption of 1.6 mW at frequencies as high as 100 MHz, while its gain ranges from 0 dB to 21 dB in 3 dB steps through a digital word. The settling time of the circuit is below 0.25 µs.

Keywords: Automatic gain control, CMOS mixed-mode integrated circuits, IF strip, programmable gain amplifier, wireless LAN.

I. Introduction

Automatic gain control (AGC) is an essential function in all wireless communication systems [1], [2]. Therefore, many AGC circuits have been proposed to date, attention being currently focused on their implementation in deep-submicron CMOS technologies to attain large integration and chip-cost reduction.

The AGC circuitry adjusts the output signal of the embedded variable or programmable gain amplifier to a constant level which optimizes the dynamic range of the succeeding circuits independently of the input signal strengths. Conventional AGCs use a closed-loop feedback technique to settle the desired output signal amplitude, as shown in Fig. 1. However, in applications such as WLAN or Bluetooth, the timing constraints of receivers preclude the use of such closed-loop AGC schemes. Meanwhile, novel feedforward and open-loop gain control techniques have proven to be adequate to shorten the settling time and reduce the acquisition time of AGCs [3]-[5].

This paper presents an AGC circuit based on a feedforward approach to achieve very fast convergence of the amplifier

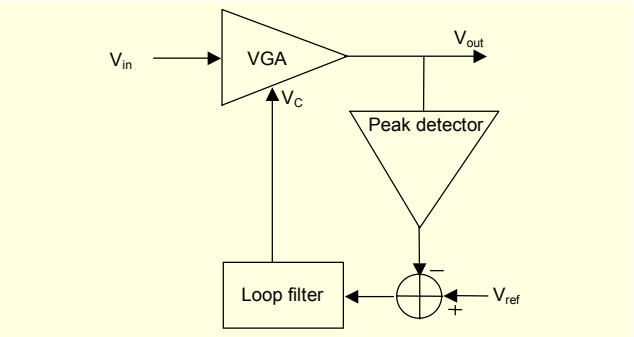

Fig. 1. Conventional feedback AGC loop.

Manuscript received Feb. 5, 2008; revised Aug. 19, 2008; accepted Aug. 22, 2008.

Juan Pablo Alegre (phone: +34976761000 ext. 3427, email: juanpa@unizar.es), Belén Calvo (email: becalvo@unizar.es), and Santiago Celma (email: scelma@unizar.es) are with the Group of Electronic Design, University of Zaragoza, Zaragoza, Spain.

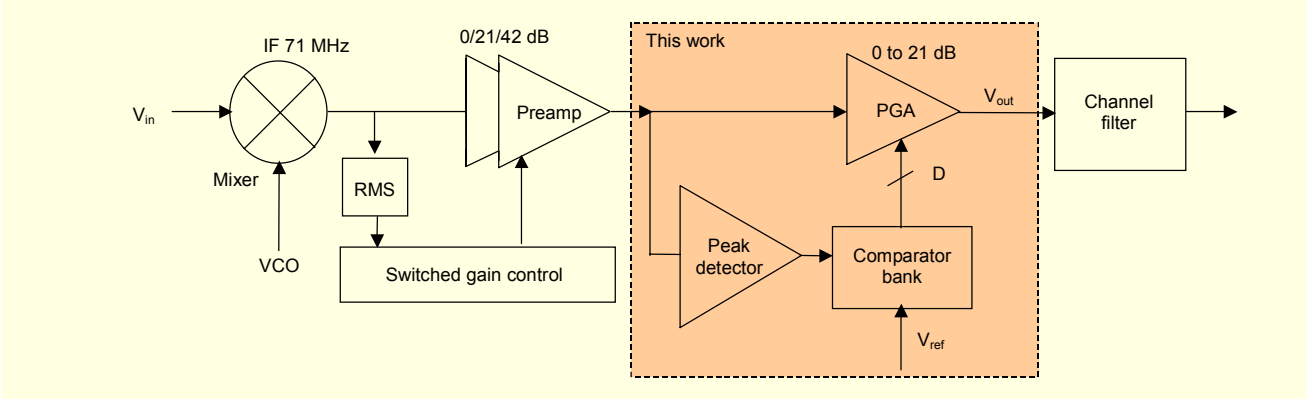

Fig. 2. IF 71 MHz strip.

gain setting. The proposed AGC circuitry consists of a digitally programmable gain amplifier, a peak detector, and a 4-bit flash ADC using thermometer code. It offers low-voltage (1.8 V), low-power operation (1.6 mW), low-distortion (< –70 dB IM3), and an inherent rapid convergence of the amplifier gain (attack time < 40 ns and settling time < 250 ns). Section II describes the proposed AGC architecture and the circuit design of the key function blocks. The main performance features are summarized in section III. Finally, conclusions are drawn in section IV.

II. System Architecture

The AGC described in this paper is the last stage of the complete IF AGC shown in Fig. 2. The full background AGC consists of two coarse fixed-gain preamplifiers controlled by simple pass-switches with a digitally programmable gain amplifier (PGA) at the end that allows final fine gain adjustment [6]. With this common gain distribution architecture, the total input range variation in the last stage cannot exceed the gain of one of the previous amplifiers. Establishing V_{out} = 0.4 $V_{P\text{-}P}$ as a typical output voltage and by using preamplifiers of 21 dB as depicted in Fig. 2, the expected input dynamic range extends from –25 to –4 dBm (21 dBm). This range is small enough to relax the design specifications of the peak detector.

To reach the desired constant output amplitude, a peak detector (PD) extracts the signal amplitude at the input of the PGA as shown in Fig. 2. This signal amplitude is then introduced in a simple comparator array like a flash ADC, which directly generates the digital word to control the PGA gain. The circuit description and implementation of these main blocks constituting the proposed AGC, namely, the digitally programmable gain amplifier, the peak detector, and a 4-bit comparator bank are given in the following subsections.

1. Programmable Gain Amplifier

Figure 3 shows the complete PGA scheme with the specified transistor sizes and biasing conditions. The scheme is based on a very simple negative feedback g_m-boosted differential pair with output resistive loads. The gain is varied by combining two techniques: a switchable array of source degenerating hybrid polysilicon-MOS resistors and a programmable output current mirror [7]. Biasing currents are implemented through cascode configurations.

Focusing on the transconductor core, transistors M_1-M_2 form a two-pole negative-feedback loop, which reduces the equivalent source resistance of the input voltage buffer M_1 to approximately 50 Ω. The source resistance value is given as in [8] by

$$r_s \approx \frac{1}{g_{m1} r_{o1} g_{m2}}, \tag{1}$$

where g_{mi} and r_{oi} are respectively the transconductance and the output conductance of transistor M_i. Therefore, for a source-degenerated pair exploiting this approach, the differential transconductance can be expressed as

$$G_m = \frac{\alpha}{R}, \tag{2}$$

where R denotes one-half the degeneration resistance, and α denotes the M_1 gate-to-source DC voltage gain:

$$\alpha \approx \frac{g_{m1}}{g_{m1} + g_{mb1}}, \tag{3}$$

which is somewhat less than unity due to the body effect of the input pair transistors (NMOS in a P-substrate single-well CMOS technology).

Next, the linearized differential signal current, copied out by loading each M_2 gate terminal with a matched NMOS device, is converted to voltage through load resistors R_L. Thereby, the

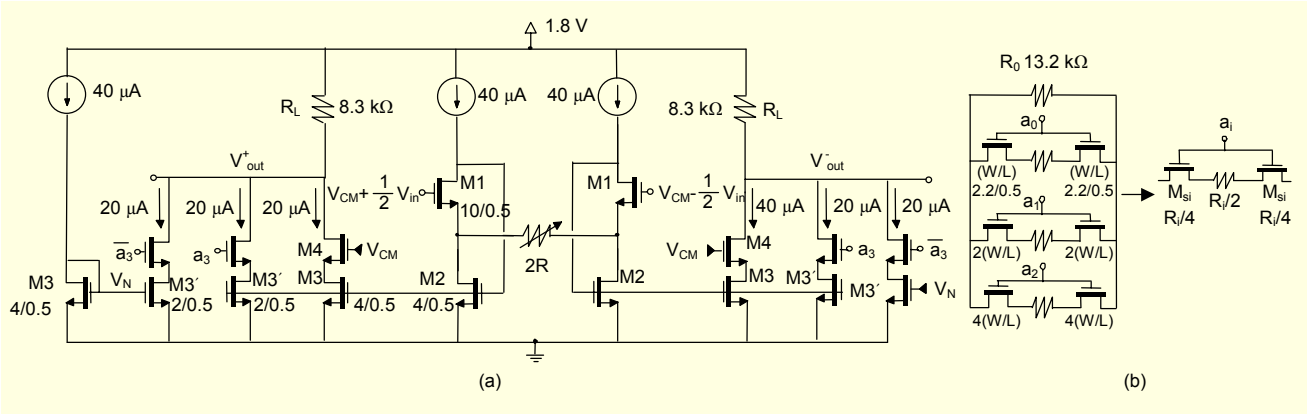

Fig. 3. Programmable gain amplifier cell: (a) amplifier core and (b) programmable degeneration resistance.

differential gain of this stage is given by

$$\text{Gain} = G_m \cdot R_L = \alpha \frac{R_L}{R}. \tag{4}$$

The gain is adjusted by using a variable degeneration resistor while maintaining a constant load resistor. This choice results in a fixed dominant pole at the PGA output nodes:

$$f_d = \frac{1}{2\pi R_L C_L}, \tag{5}$$

which is determined by the load resistor R_L and the load capacitance C_L; therefore, a constant bandwidth is maintained throughout all the gain stages [9]. For high-frequency applications, noise specifications limit the value of the load and degeneration resistors to the kΩ range. Further, high resistivity polysilicon (HRP) loads R_L will be implemented to avoid degrading the linearity performance. All these considerations lead to choosing a HRP load resistor R_L=8.3 kΩ, which results in an expected intrinsic constant bandwidth in the 100 MHz range.

With respect to the degeneration resistance, to preserve good linearity and moderate area consumption while facilitating digital gain control, we settled for an approach which merges, in equal parts, HRP resistors and MOS transistors biased in the triode region. These act simultaneously as resistors and switches. Following this strategy, the degeneration scheme is shown in Fig. 3(b). The minimum gain setting is imposed by a fixed HRP resistor R_o. The gain is then digitally increased by adding in parallel a new linear resistor in series with two M_{Si} NMOS switches biased in the triode region, whose on-resistance is one half of the total conversion impedance. An additional gain programmability degree of freedom can be provided at the output current mirrors implemented through M_2-M_3 by adding identical output stages in parallel as shown in Fig. 3(a) with the M_3 cascode transistors acting as the switching elements. In this case, the total differential gain is equal to the following expression:

$$\text{Gain} = K\alpha \frac{R_L}{R}, \tag{6}$$

where K is the current mirror gain:

$$K = \frac{(W/L)_3}{(W/L)_2}, \tag{7}$$

while all the other parameters have the meaning previously defined.

In particular, the programmable degeneration impedance consists of a 3-bit array [a_2 a_1 a_0] of hybrid HRP-NMOS resistors in parallel which are binary weighted to obtain a logarithmic gain distribution ranging from 0 to 18 dB in 6 dB steps through a thermometer code control. A fourth bit, a_3, allows the output current mirror gain K to be set either at 1 or 1.5. This enables the scaling of each 6 dB step so that the scheme covers an overall range of 0 dB to 21 dB gain programmability in 3 dB steps using a 4-bit discrete coarse tuning. Fine gain tuning can be performed if necessary through slight gate voltage variations for the switching transistors in order to improve accuracy.

To generate a suitable common-mode output voltage equal to that of the input (V_{CM}=1.3 V), an additional current source controlled through the complementary of a_3 is introduced. In this way, when the output current mirror gain K=1, the current source switches on, but when K=1.5 it switches off, enabling the output DC current to be kept constant.

2. Peak Detector

Figure 4 shows the peak detector structure and specifies transistor sizes, component values, and biasing conditions. It is a differential positive scheme in which, instead of a rectifier diode, a unidirectional current mirror is employed with a transconductor to implement the rectifier circuit [10]. One detector is employed for each balanced signal, and both signals

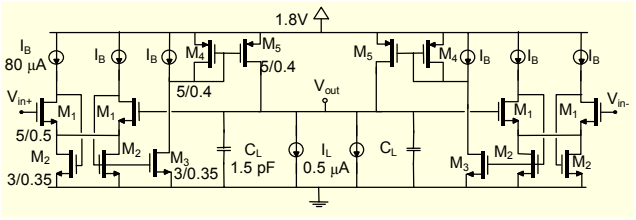

Fig. 4. Peak detector cell.

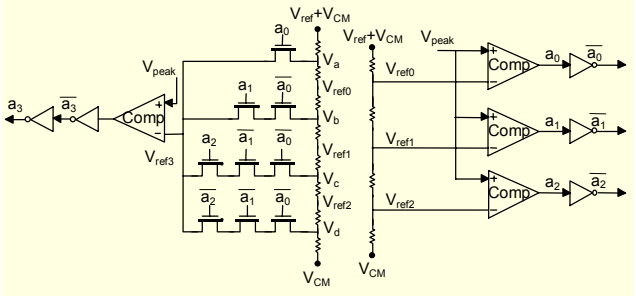

Fig. 5. Comparator bank cell.

are added at a single output. The excess current flowing through current mirror charges the hold capacitor C_L when V_{in} is larger than V_{peak}. When V_{in} is smaller than V_{peak}, the capacitor is slowly discharged by the current I_L. Therefore, the capacitor discharge follows this equation:

$$dV_{out}(t) = \frac{dQ(t)}{C_L} = \frac{I_L}{C_L}dt, \tag{8}$$

where, since I_L is a constant current, the capacitor discharge is linear with I_L/C_L:

$$V_{out}(t) = V_{out}(0) - \frac{I_L}{C_L}t. \tag{9}$$

As a result, the peak detector settling time increases with the detected input signal amplitude, and it must be calculated for the worst case, that is, when the signal amplitude is the maximum.

Rather than using a simple transconductor as in [10], we employ a high performance G_m cell based on the same core cell as the PGA of Fig. 3. Thus, with a very compact design, the peak detector exhibits higher linearity at higher frequencies with lower power consumption.

3. Gain Computation Block

The output of the envelope detector is carried to a comparator bank (simple differential pairs) where it is compared to a reference level V_{ref} as shown in Fig. 5. To take into account any change in the input common-mode level V_{CM}, and since the peak detector is not balanced, the reference level is generated with respect to V_{CM}. The first 3 bits [a_2, a_1, a_0] that control the degeneration resistance providing the logarithmic gain distribution ranging from 0 to 18 dB in 6 dB steps are obtained simply by comparing the detected amplitude to the reference voltages V_{ref0}, V_{ref1}, and V_{ref2} derived from a resistor ladder.

The fourth bit, a_3, allows the 3 dB step gain resolution through the control of the output current mirror. It is generated by using a single comparator, which contrasts the detected amplitude to a reference voltage, V_{ref3}, obtained by using simple logic (see Fig. 5):

$$V_{ref3} = \begin{cases} V_a, & \text{if } a_0 = 1 \\ V_b, & \text{if } \mathrm{AND}(a_1, \overline{a_0}) = 1 \\ V_c, & \text{if } \mathrm{AND}(a_2, \overline{a_1}, \overline{a_0}) = 1 \\ V_d, & \text{if } \mathrm{AND}(\overline{a_2}, \overline{a_1}, \overline{a_0}) = 1. \end{cases} \tag{10}$$

That is, V_{ref3} equals one of the reference voltages V_a, V_b, V_c, and V_d depending on the value of the first three bits. For example, should V_{peak} be between V_{ref0} and V_{ref1}, the corresponding digital word would be [0 0 1], and following (10), the comparison reference voltage V_{ref3} to generate a_3 would be equal to V_a. Two different resistor banks are employed to avoid undesired feedback which would spoil the performance of the circuit.

III. Performance

The proposed AGC was designed in AMS 0.35 μm CMOS technology and simulated using SPECTRE with a BSIM3 v3.2 level 53 transistor model. The overall circuit comprises the digitally programmable gain amplifier, the peak detector, and the 4-bit comparator bank. It consumes 1.6 mW from a single 1.8 V supply voltage. Through a 4-bit thermometer code control, the gain can be varied linearly in decibels from 0 dB to 21 dB in 3 dB steps. The frequency response of the main gain settings is shown in Fig. 6. The –3 dB bandwidth is kept

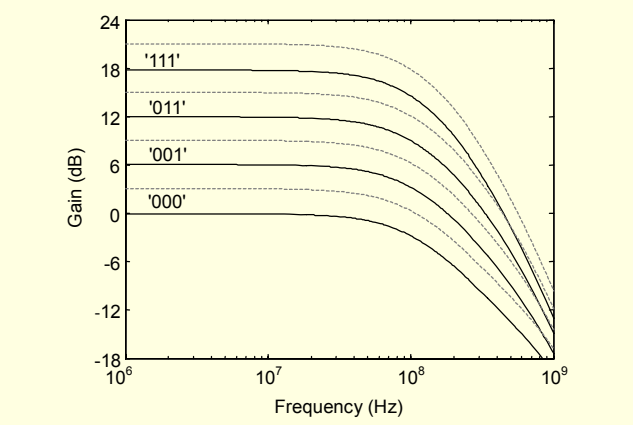

Fig. 6. PGA frequency response. Solid line: K=1, dashed line: K=1.5.

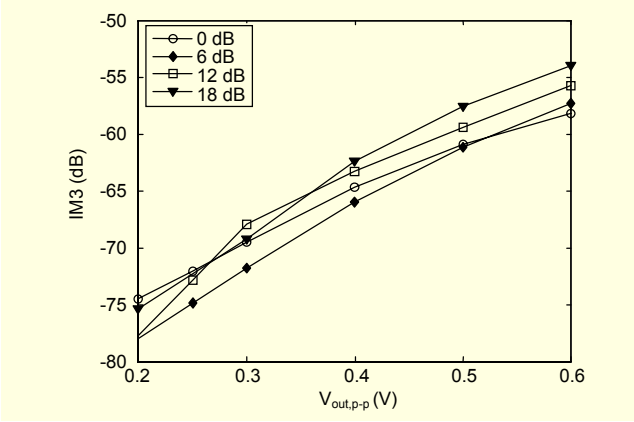

Fig. 7. IM3 levels at 71 MHz for the main gain settings versus output voltage V_{out}.

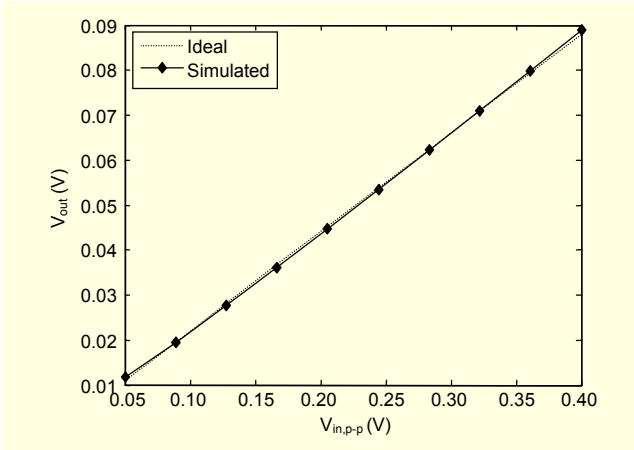

Fig. 8. Input-output linearity of the peak detector.

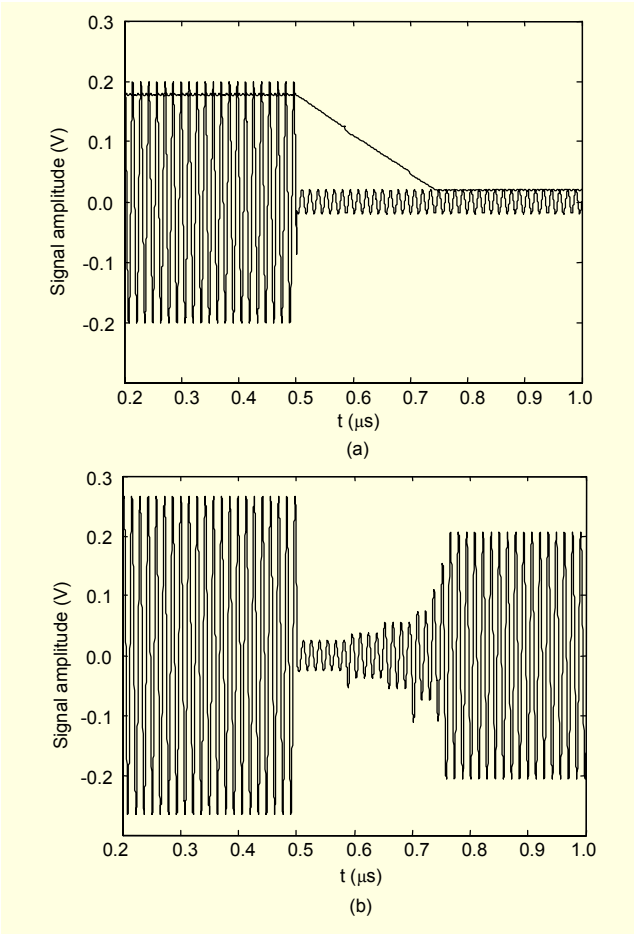

Fig. 9. AGC convergence performance with a 21 dB stepwise change input signal at 71 MHz: (a) input and envelope signal and (b) the worst case AGC output.

constant around 100 MHz over the whole gain range, assuming output capacitive loads of 150 fF.

The third-order inter-modulation (IM3) behavior for two signals at frequencies of 70 MHz and 71 MHz is shown in Fig. 7 considering constant differential output levels. Figures are below –70 dB over the whole gain setting range with a differential output signal level of 0.2 V_{p-p}. The value increases to –60 dB for 0.4 V_{p-p}.

The input-output performance with sinusoidal input for the implemented envelope detector is shown in Fig. 8. Deviations from ideal behavior are below ±0.5 dB for the whole input range. Therefore, although the accuracy for the AGC employed in this work is 3 dB with 4 bits, if necessary, it is possible to increase it up to 1 dB by increasing the bit resolution.

The convergence of the AGC was tested in the worst case condition. A 21 dB stepwise signal was introduced, which is the maximum change that the AGC can observe due to the switching of one of the fixed gain amplifiers just before the PGA. To measure the attack time, the input signal was increased by 21 dB, and the AGC converged in less than 40 ns. On the other hand, to measure the settling time the input signal was reduced. The results for the latter are shown in Fig. 9. The AGC adjusts signals to the desired output level (0.4 V_{p-p}) in less than 0.25 μs. Since the AGC has a feedforward loop, the settling time required by the AGC is equal to that required by the envelope detector.

Finally, as shown in Table 1, compared with several AGCs previous realizations [1], [9], the proposed low-voltage AGC exhibits faster settling time with lower power consumption and employs a lower performance technology. Furthermore, other characteristics, such as in-band noise, are still similar to those reported previously. Thus, the very competitive performance exhibited by the proposed AGC makes it a preferable choice for present day low-voltage low-power wireless communication applications where a reduced settling time is absolutely essential.

IV. Conclusion

This paper presented a 1.8 V 0.35 μm CMOS AGC circuit

Table 1. Summary of AGC performance.

Parameter	[3]	[11]	This work
Technology	0.18 µm CMOS	0.25 µm BiCMOS	0.35 µm CMOS
Supply voltage	1.6 to 2 V	3 to 5.2 V	1.8 V
AGC output voltage	500 $mV_{pp,diff}$	110 $mV_{pp,diff}$	400 $mV_{pp,diff}$
Bandwidth	18 MHz	400 MHz	100 MHz
AGC gain range	-8 to 32 dB (±1 dB)	0 to 45 dB	0 to 21 dB (±3 dB)
AGC settling time	4.8 µs	0.3 µs*	0.25 µs
Distortion	< –37 dB**	–	< –60 dB***
In-band noise @ 0 dB	77.5 nV/√Hz	40 nV/√Hz	51 nV/√Hz
Current consumption	5.8 mA	20 mA	0.9 mA

(*) Attack time, (**) THD 1 MHz, (***) IM3 71 MHz .

based on a feedforward approach which converges to the desired level within 0.25 µs. The proposed architecture is very simple and compact and can be implemented with basic cells, while achieving a high level of performance. Therefore, this AGC can be very useful in applications such as WLAN or Bluetooth receivers, where the use of traditional closed-loop feedback amplifiers forms a boundary due to the stringent settling-time constraints.

References

[1] B. Park et al., "A 3.1 to 5 GHz CMOS Transceiver for DS-UWB Systems," *ETRI Journal*, vol. 29, no. 4, Aug. 2007, pp. 421-429.

[2] S.B. Hyun et al., "A Dual-Mode 2.4-GHz CMOS Transceiver for High-Rate Bluetooth Systems," *ETRI Journal*, vol. 26, no. 3, June 2004, pp. 229-240.

[3] O. Jeon, R.M. Fox, and B.A. Myers, "Analog AGC Circuitry for a CMOS WLAN Receiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, 2006, pp. 2291-2300.

[4] T. Oshima et al., "Automatic Tuning of RC Filters and Fast Automatic Gain Control for CMOS Low-IF Transceiver," *IEEE Custom Integrated Circuits Conference*, 2003, pp. 5-8.

[5] C.W. Lin, Y.Z. Liu, and K.Y.J. Hsu, "A Low-Distortion and Fast-Settling Automatic Gain Control in CMOS Technology," *IEEE 2004 Intern. Symp. Circuits and Systems*, vol. 1, 2004, pp. 541-544.

[6] C.P. Wu and H.W. Tsao, "A 110-MHz 84-dB CMOS Programmable Gain Amplifier With Integrated RSSI Function," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, 2005, pp. 1249-1258.

[7] B. Calvo, S. Celma, and M.T. Sanz, "Low-Voltage Low-Power CMOS IF Programmable Gain Amplifier," *49th IEEE Midwest Symp. Circuits and Systems*, vol. 2, 2006, pp. 276-280.

[8] R.G. Carvajal et al., "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Trans. Circuits and Systems I*, vol. 52, no. 7, July 2005, pp. 1276-1291.

[9] J.J.F. Rijns, "CMOS Low-Distortion High-Frequency Variable-Gain Amplifier," *IEEE J. Solid-State Circuits*, vol. 31, July 1996, pp. 1029-1034.

[10] S.B. Park, J.E. Wilson, and M. Ismail, "Peak Detectors for Multistandard Wireless Receivers," *Circuits and Devices Magazine*, vol. 22, Nov./Dec. 2006, pp. 6-9.

[11] T. Drenski et al., "A BiCMOS 300 ns Attack-Time AGC Amplifier with Peak-Detect and Hold Feature for High-Speed Wireless ATM Systems," *IEEE Int'L Solid-State Circuits Conference, Digest of Technical Papers*, 1999, pp. 166-167.

Juan Pablo Alegre received the BS degree in physics from the University of Zaragoza, Spain, in 2003. He worked at the Aragon Institute of Technology in Electromagnetic Compatibility (EMC). Currently, he is pursuing a PhD degree and is a member of the Group of Electronic Design (GDE-I3A) of the University of Zaragoza. His research interests include mixed analog-digital microelectronic circuit design, auto-tuning circuits, device modeling and electronics for high frequency communications.

Belén Calvo received the BS degree in physics in 1999 and the PhD degree in electronic engineering in 2004, both from the University of Zaragoza, Spain. She is a member of the Group of Electronic Design at the Aragon Institute for Engineering Research (GDE-I3A) of the University of Zaragoza. Her research interests are in the areas of analog and mixed-mode CMOS IC design, high performance amplifiers, on-chip programmable circuits, and sensor interfaces.

Santiago Celma received the BS degree in 1987, the MS degree in 1989, and the PhD degree in 1993, all in physics, from the University of Zaragoza, Spain. Currently, he is a full professor in the Department of Electronic Engineering and Communications at the University of Zaragoza and heads the Group of Electronic Design at the Aragon Institute for Engineering Research (GDE-I3A) of the University of Zaragoza. He has co-authored more than 50 technical papers and 170 international conference contributions. His research interests include circuit theory, mixed-signal integrated circuits, wireless sensor networks, and intelligent instrumentation.