1.5 V Sub-mW CMOS Interface Circuit for Capacitive Sensor Applications in Ubiquitous Sensor Networks

Sungsik Lee, Ahra Lee, Chang-Han Je, Myung-Lae Lee, Gunn Hwang, and Chang-Auck Choi

In this paper, a low-power CMOS interface circuit is designed and demonstrated for capacitive sensor applications, which is implemented using a standard 0.35-μm CMOS logic technology. To achieve low-power performance, the low-voltage capacitance-to-pulse-width converter based on a self-reset operation at a supply voltage of 1.5 V is designed and incorporated into a new interface circuit. Moreover, the external pulse signal for the reset operation is made unnecessary by the employment of the self-reset operation. At a low supply voltage of 1.5 V, the new circuit requires a total power consumption of 0.47 mW with ultra-low power dissipation of 157 μW of the interface-circuit core. These results demonstrate that the new interface circuit with self-reset operation successfully reduces power consumption. In addition, a prototype wireless sensor-module with the proposed circuit is successfully implemented for practical applications. Consequently, the new CMOS interface circuit can be used for the sensor applications in ubiquitous sensor networks, where low-power performance is essential.

Keywords: Low-power CMOS interface circuit, readout integrated circuit (ROIC), capacitive MEMS sensor, ubiquitous sensor network (USN).

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Sungsik Lee (phone: + 82 42 860 5763, email: lss@etri.re.kr), Ahra Lee (email: ara1018@etri.re.kr), Chang-Han Je (email: chje@etri.re.kr), Myung-Lae Lee (email: mllee@etri.re.kr), Gunn Hwang (email: hwangun@etri.re.kr), and Chang-Auck Choi (email: cachoi@etri.re.kr) are with the Convergence Components & Materials Research Laboratory, ETRI, Daejeon, Rep. of Korea.

I. Introduction

Recently, the low-voltage operation of CMOS signal-processing circuitry for sensor applications has been a key performance requirement for portable and wireless devices, such as PDAs, cell phones, navigation systems, and structural health monitoring systems in sensor networks including ubiquitous sensor networks (USNs) [1]-[3]. In sensor networks, capacitive sensors can show relatively low power characteristics due to the reduction of the leakage current level in the sensor part, compared to resistive sensors [2]. Moreover, low-power CMOS circuits for various sensors need to be designed for reduction of power dissipation in the circuit part [3]. In this respect, the interface circuitry for the signal-readout of sensors is an important part of low-power sensor systems [4]-[6].

Prior interface circuit designs for capacitive sensing were mainly focused on high sensitivity and low noise, but low-power performance has not been achieved [5]. For example, battery powered wireless sensor applications in USNs normally are required to consume at most hundreds of microwatts for long-time operation. Therefore, the design of interface circuits with medium to high performance at very low power consumption is very important [6].

Depending on requirements of low power consumption, some advanced interface circuits and low-power circuit techniques have been proposed and can be used to measure the sensor capacitance at low supply voltages [7]. At a low supply voltage, capacitance-to-voltage conversion can be performed using the switched-capacitor (SC) charge amplifier [8].

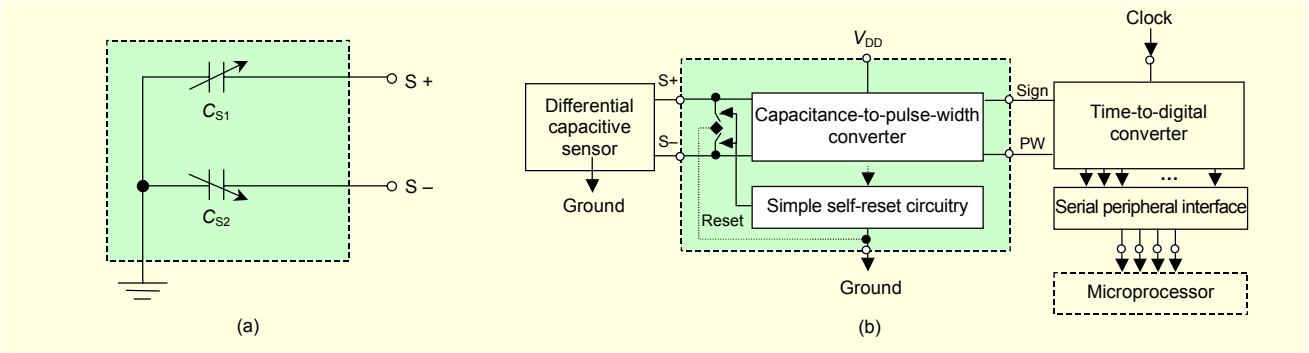

Fig. 1. (a) Conceptual circuit diagram of the differential capacitive sensor and (b) block diagram of the proposed interface circuit, including the capacitance-to-pulse-width converter with simple self-reset circuitry.

However, the low-voltage operational amplifier for the SC amplifier is difficult to design while maintaining both a wide output voltage-swing and high slew-rate at a low supply voltage [6]-[8]. This leads to degraded performance in terms of low signal-to-noise ratio (SNR) and low dynamic-range. To reduce the power consumption of capacitive sensor systems, boost-trapped signaling techniques have been proposed [9], [10].

While boosting the signal level, a noise signal with a relatively high voltage level also can be amplified. Moreover, a drawback of the boost-trapping technique is that it can give rise to hot-carrier related reliability problems, especially in a sub-micrometer technology, and this significantly reduces the circuit lifetime [10].

As another approach, quasi-digital interface circuits have been proposed with capacitance-to-frequency (phase) conversion operation [11]. The signal of the capacitance-to-frequency (phase) converter can be easily read out by the microcontroller unit with a reference frequency. However, it should be observed that the output frequency or phase is strongly dependent on the device parameters, such as the passive elements values (resistances and capacitances) and the transistor DC performance, which can be affected by threshold voltage variation associated with process variations and difficulties of low-voltage operation due to the down-scaling of the supply voltage [12]. In this respect, this implementation is also difficult to operate at low voltages.

In this paper, a 1.5 V sub-mW CMOS interface circuit based on a capacitance-to-pulse-width conversion operation is demonstrated for capacitive sensor applications. It is implemented using a standard 0.35 μm CMOS logic technology. To achieve this, a low-power capacitance-to-pulse-width converter based on self-reset operation is incorporated into the new circuit design. The details of the new circuit structure, simulated results, and measured performance characteristics are discussed in the following sections.

II. Architecture of the Proposed Interface Circuit

Figure 1(a) shows the conceptual circuit diagram of the capacitive differential sensor. A block diagram of the proposed interface circuit is shown in Fig. 1(b). To drive the differential capacitive sensor, the low-voltage capacitive-to-pulse-width converter is incorporated into the new circuit design, which consists of low-voltage Schmitt trigger circuits with a maximized upper trigger point (UTP) below the supply voltage (V_{DD}). In addition, a simple self-reset circuit is employed for the reset operation. For the pulse-width-to-digital conversion operation, a time-to-digital converter is also designed and employed with the serial peripheral interface (SPI) as shown in Fig. 1(b). The details of the circuit structure and operating principle are presented in the following subsection.

1. Capacitance-to-Pulse-Width Conversion Operation

Figure 2 shows the schematic diagram of the new interface circuit-core including the capacitance-to-pulse-width converter, self-reset circuit, and bidirectional readout circuit [13]. The equivalent capacitors C_{S1} and C_{S2} of the capacitive sensor are connected to the interfacing nodes S+ and S–, respectively. The proposed circuit is operated with the capacitance-to-pulse-width conversion operation based on self-reset operation for the differential capacitive sensors [13].

Figure 3 shows the conceptual voltage waveforms of the new interface circuit for the capacitance-to-pulse-width conversion operation. When the new circuit is turned on, the reset signal is initially and automatically applied at the reset signal node (V_{RST}) through the pull-up resistor (R_P) connecting to the supply voltage (V_{DD}). Then, the transistors (M1, M3) are automatically turned-on, which leads to the low voltage levels of V_{S1} and V_{S2}. In addition, low voltage levels simultaneously appear at the output nodes (V_{O1}, V_{O2}) of the Schmitt trigger circuit (U2, U4). Under these conditions, the PMOS transistors (M2, M4) are turned on, which results in an increase in the voltage levels (V_{S1}, V_{S2}) arising from the charging current

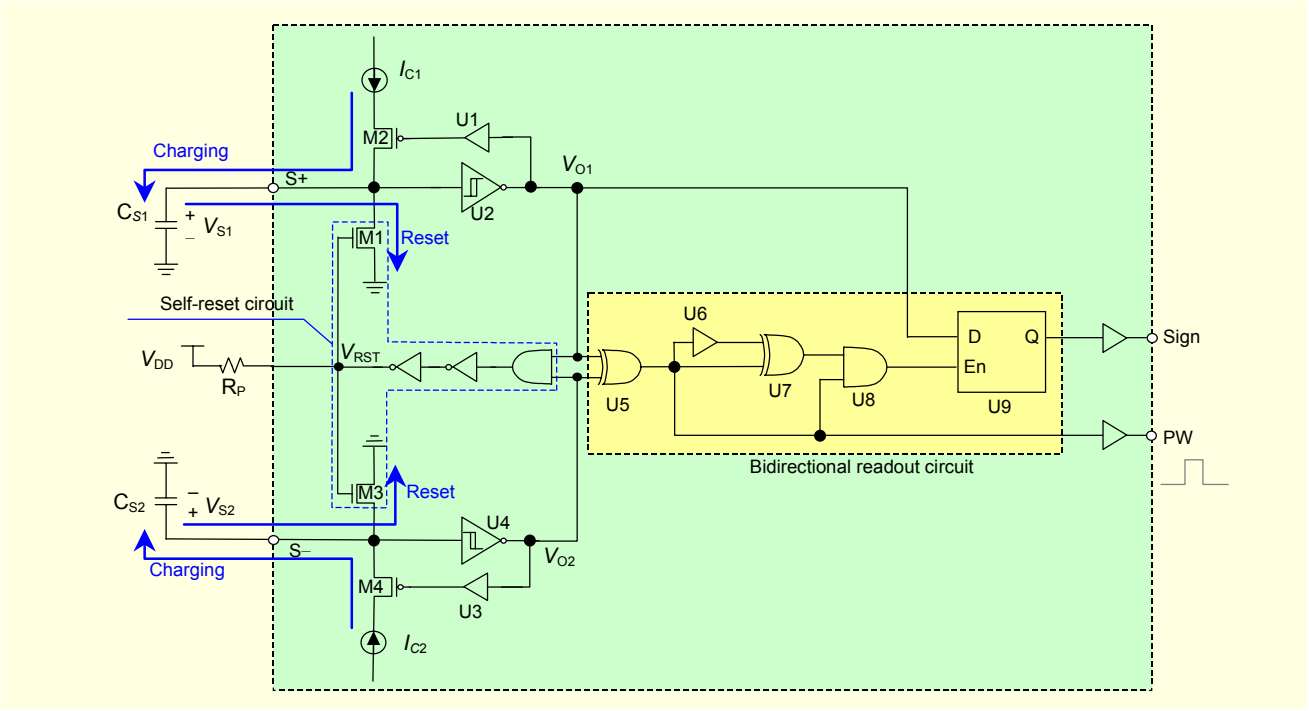

Fig. 2. Schematic diagram of the proposed interface-circuit core for capacitance-to-pulse-width conversion with simple self-reset circuitry.

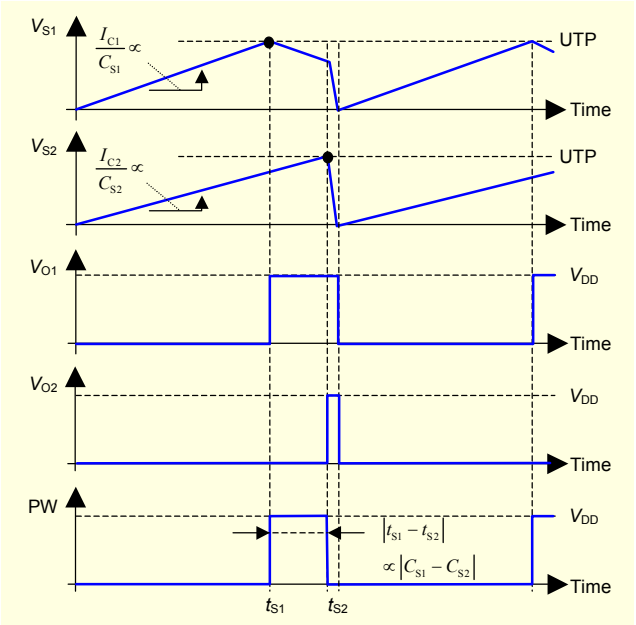

Fig. 3. Conceptual timing diagram for the capacitance-to-pulse-width conversion operation of the proposed interface circuit.

(I_{C1}, I_{C2}).

As shown in Fig. 3, the voltage levels (V_{S1}, V_{S2}) of the sensor capacitors linearly increase to the UTP of the low-voltage Schmitt trigger circuit. In this readout-operation, the step signals (V_{O1}, V_{O2}) are generated at the starting time of t_{S1} and t_{S2}, which are proportional to the sensor capacitances (C_{S1}, C_{S2}), respectively, as

$$t_{S1} = \frac{\int_0^{UTP} C_{S1} dV_{S1}}{I_{C1}} \approx \frac{C_{S1} \cdot UTP}{I_{C1}}, \quad (1)$$

$$t_{S2} = \frac{\int_0^{UTP} C_{S2} dV_{S2}}{I_{C2}} \approx \frac{C_{S2} \cdot UTP}{I_{C2}}. \quad (2)$$

On the one hand, two rectangular pulse-signals (V_{O1}, V_{O2}) are used for the generation of the pulse width (PW) signal as shown in Fig. 3. Using the exclusive-OR gate (U5) with two input signals of V_{O1} and V_{O2}, the PW signal appears at the output node of U5 as shown in Figs. 2 and 3. In this operation, the PW $|t_{S1}–t_{S2}|$ of the PW signal is made, which is proportional to the difference between C_{S1} and C_{S2}:

$$|t_{S1} - t_{S2}| = \frac{|C_{S1} - C_{S2}| \cdot UTP}{I_C}, \quad (3)$$

where I_C is the charging current, assuming $I_{C1}=I_{C2}\equiv I_C$. Equation (3) shows the theoretical and mathematical principle of the capacitance-to-pulse-width conversion operation. Therefore, the capacitance difference $|C_{S1}–C_{S2}|$ of the sensor can be read out by the new conversion operation.

When the voltage levels (V_{S1}, V_{S2}) of the sensor capacitors reach the voltage level of the UTP, the transistors M2 and M4,

which are charging-current (I_{C1}, I_{C2}) paths for the charging process, are automatically turned-off by the high voltage levels at the outputs (V_{O1}, V_{O2}) of the Schmitt trigger circuit. The additional and unnecessary current-consumption arising from the charging process can be minimized and reduced. Hence, low-power performance can be achieved by the reduction of this charging current and time.

In addition, the Schmitt trigger circuit is employed to operate at the low supply voltage of 1.5 V as shown in Fig. 4(a) [15], [16]. The basic operating principle of the Schmitt trigger circuit is the same as that of the conventional circuit [15]. In the new circuit configuration, the UTP level is especially designed and tuned for low-voltage operation, which is determined by a threshold voltage level shift due to the body-bias conditions and a factor R associated with transistor-sizing (W/L) [14]-[16] as

$$UTP = \frac{V_{DD} - V_{TP} + R \cdot V_{TN}}{R+1}, \quad (4)$$

$$R \equiv \sqrt{\frac{\beta_N}{\beta_P}} = \sqrt{\frac{\mu_N L_P W_N}{\mu_P L_N W_P}}, \quad (5)$$

where V_{TP} is the threshold voltage of the pMOSFET, V_{TN} is the threshold voltage of the nMOSFET, μ_N is the electron mobility in the channel of the nMOSFET, μ_P is the hole mobility in the channel of the pMOSFET, L_N is the channel length of the nMOSFET, L_P is the channel length of the pMOSFET, W_N is the channel width of the nMOSFET, W_P is the channel width of the pMOSFET, and R is the design factor for the UTP level.

For the design of the UTP, the body-bias conditions are very important and directly affect the threshold voltages (V_{TP}, V_{TN}) [14]. In particular, the UTP is determined by the high-level input (V_I). When the high-level signal is applied to V_I, V_O reaches the high level due to the inverter operation. The high level of V_O provides a forward body-bias to the transistor M_{N1}–M_{N2} and a zero body-bias to the transistor M_{P1}–M_{P2}. Under these body-bias conditions, the threshold voltages of V_{TP} and V_{TN} are determined. For 1.5 V operation, in the proposed interface circuit, UTP is set to 1.2 V by choosing proper values for R and threshold voltages.

2. Self-Reset Operation

Figure 4(b) shows the self-reset circuit, which consists of a NAND gate, two inverters, and two nMOSFETs. Two inverters are used for intensive time-delay.

The operating sequence for the self-reset operation is shown in Fig. 5. During the time period of $|t_{S1}–t_{S2}|$, the PW stays at the high level, and both V_{O1} and V_{O2} are set to the high level as shown in Fig. 5. Hence, the high level of the self-reset signal

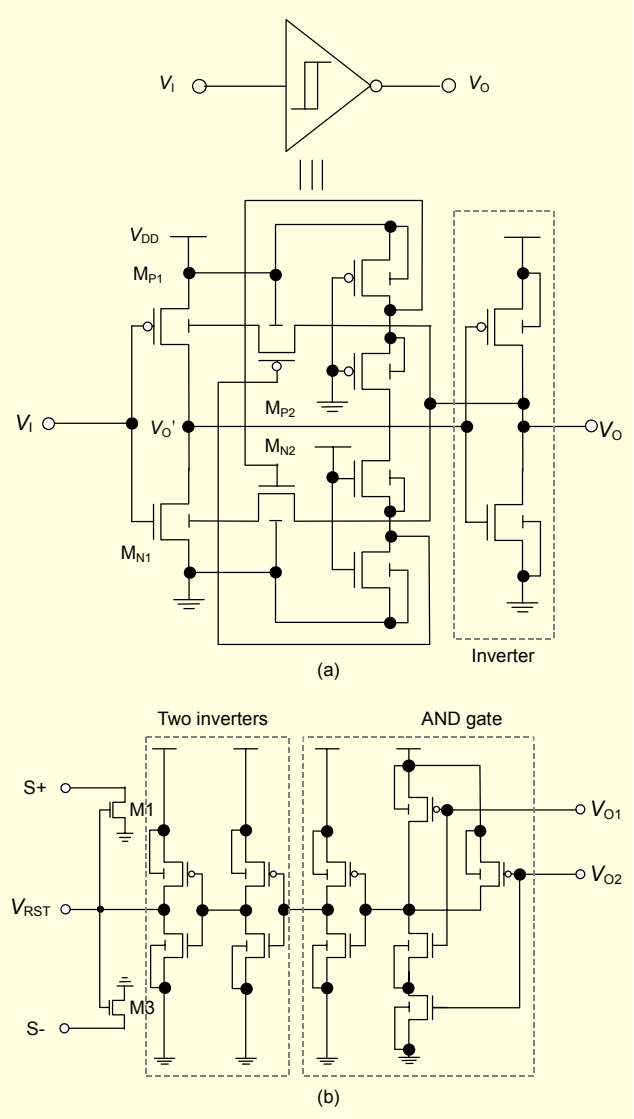

Fig. 4. Diagrams of (a) the low voltage Schmitt trigger circuit (U2, U4) and (b) the proposed self-reset circuit with two inverters.

(V_{RST}) appears at the output of the AND-gate, generated by the high level of both V_{O1} and V_{O2} (①). Next, the high level of V_{RST} is applied at the transistors (M1, M3) for the self-reset operation, which results in $V_{S1} = V_{S2} = V_{O1} = V_{O2} = 0$ (② and ③). Then, V_{RST} is set to the low voltage level because of AND-gate operation between V_{O1} and V_{O2} (④). Hence, the proposed interface circuit is automatically reset and restarted by this self-reset operation.

The self-reset operation makes the external pulse signal for the reset operation in the interface circuit unnecessary. This can reduce the power consumption that is incurred by the large circuit complexity and bias circuitry for the external reset signal. In addition, the minimum time-consumption for the reset and restart processes can be achieved by timely and effective self-

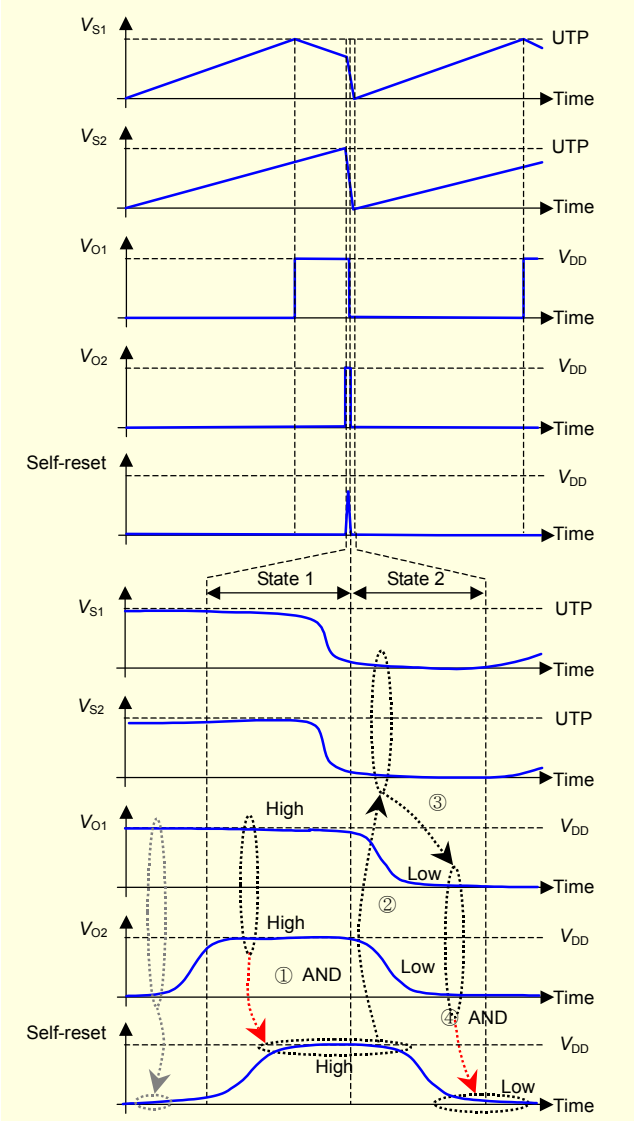

Fig. 5. Timing and sequential diagram of the proposed interface circuit for the self-reset operation.

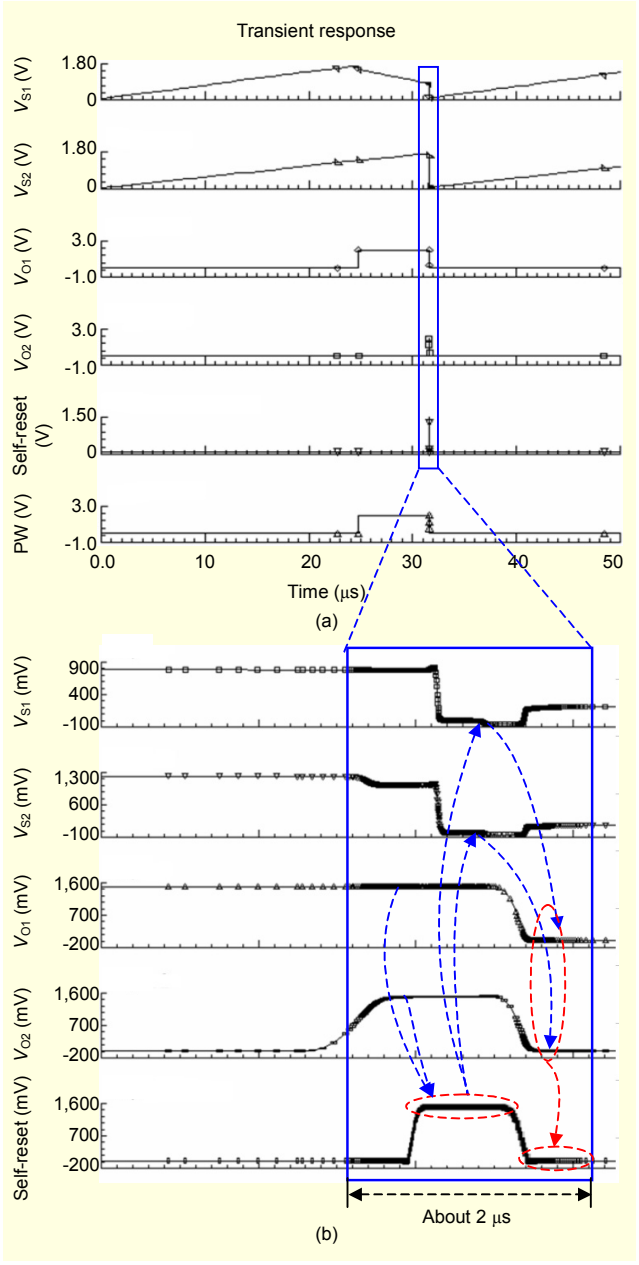

Fig. 6. Simulated results of (a) the proposed capacitance-to-pulse-width conversion and (b) the self-reset operation.

reset pulse generation as a result of the self-reset operation, and this also results in low-power performance. Hence, the new interface circuit achieves low-voltage operation and low-power performance by using low-voltage capacitance-to-pulse-width conversion based on the self-reset operation. The simulated results are discussed in the following sub-section.

3. Simulation Results

The new interface circuit was simulated and analyzed by using high precision circuit-simulators (SPECTRE and HSPICE). For the capacitive sensor simulation, capacitors of 0.2 pF and 0.3 pF were used for the sensor parts, and a supply voltage of 1.5 V was applied to the overall circuit. Figure 6 shows the simulated results. The PW ($|t_{S1}–t_{S2}|$) was observed to be proportional to the difference between C_{S1} and C_{S2} as shown in Fig. 6(a). In addition, the proposed interface circuit was automatically reset and restarted by the desired self-reset operation as shown in Fig. 6(b). The results show that the UTP was about 1.2 V. Thus, the new interface-circuit operation at the low supply voltage of 1.5 V is verified by circuit simulation. In the next section, the experimental results are discussed.

III. Experimental Results and Discussion

Figure 7(a) shows a die-photo of the fabricated chip with the

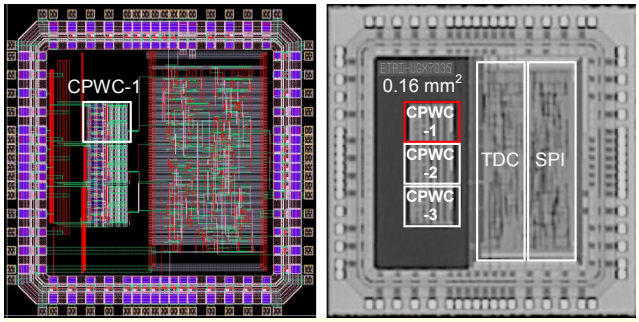

Fig. 7. (a) Layout of the proposed IC and (b) die-photo of the fabricated chip with the proposed interface circuits (CPWC-1, 2, and 3) for a 3-axis accelerometer application with the proposed interface-circuit core with the small chip size of 0.16 mm^2.

proposed interface circuits (CPWC-1, 2, and 3) for three capacitive sensors. A microphotograph of the new small circuit-core of 0.16 mm^2 is shown in Fig. 7(b). The fabricated interface circuit was implemented using a standard 0.35 μm CMOS logic technology due to its low cost. For the experimental test and measurement, the fabricated IC was made by using the standard 64-LQFP package. Capacitive sensors were used for the dynamic test and power-related measurements. The overall measurements were performed at a low supply voltage of 1.5 V. In addition, MEMS capacitive sensors with a rest capacitance of 1 pF and acceleration sensitivity of 0.2 pF/g were used in the overall measurements. To verify the capacitance-to-pulse-width conversion and self-reset operation, the transient responses were measured.

Figure 8 shows the measured results for the transient responses. The PW $|t_{S1}–t_{S2}|$ was generated, which appeared with the desired triangular signal at the capacitive sensor nodes. In addition, the desired self-reset operation was observed with timely self-reset pulse as shown in Fig. 8. Therefore, the new proposed circuit and its operation were successfully demonstrated by the transient measurements. The measured UTP is 1.2 V during operation at the given supply voltage. However, the slope of the ramp signal is not constant as shown in Fig. 8. This is mainly due to the parasitic resistance and capacitance in the test board. For the characterization of SNR, the power-spectral-density was measured.

The PW was converted to a digital value obtained by the TDC block and the SPI block. In the SPI block, the parallel data of the TDC was converted to serial samples. By using these serial samples, the power density was found by performing an 8,192-point fast Fourier transformation (FFT). Figure 9(a) shows the power spectral density which was measured at an input signal of 1-g acceleration with 20 Hz sinusoidal. The signal power and noise power, which were

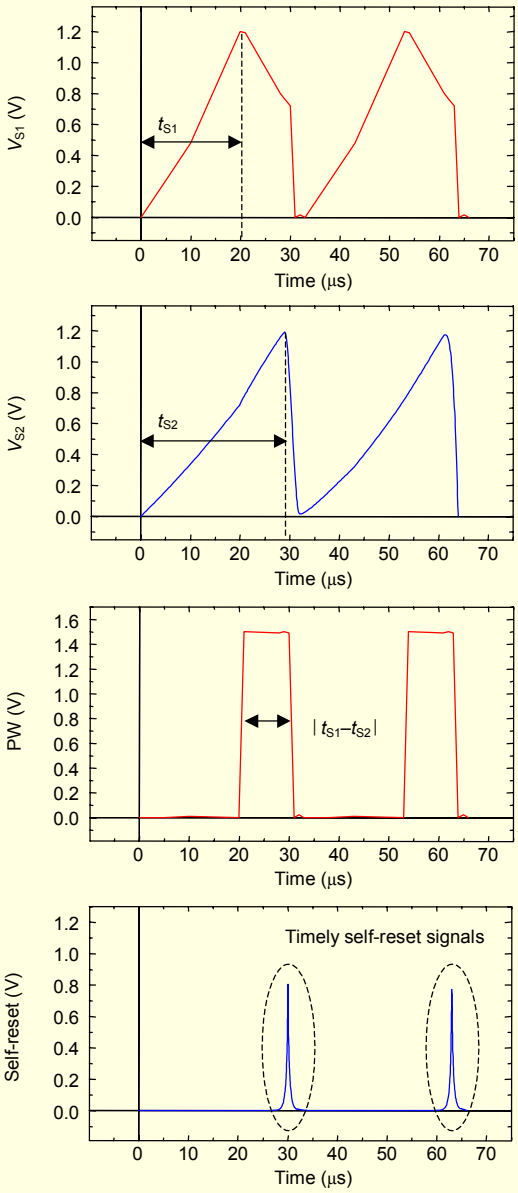

Fig. 8. Measured transient response for the desired operations of the proposed interface circuit.

measured and characterized at the bandwidth of 200 Hz, were -4.1 dB and -79.4 dB, respectively. Therefore, the SNR was characterized to 75.3 dB, which is equivalent to 12.5-bit resolution. To characterize the sensitivity of the new interface circuit, the PW was measured as a function of the capacitance difference of $|C_{S1}–C_{S2}|$. Figure 9(b) shows the measured PW versus the capacitance difference. The measured mean sensitivity was 42 μs/pF, which is comparable to other results [17]. To verify the power performance of the new interface circuit, the total biasing current was measured at the supply voltage of 1.5 V. Figure 9(c) shows the power consumption versus V_{DD}. At the supply voltage of 1.5 V, the measured DC

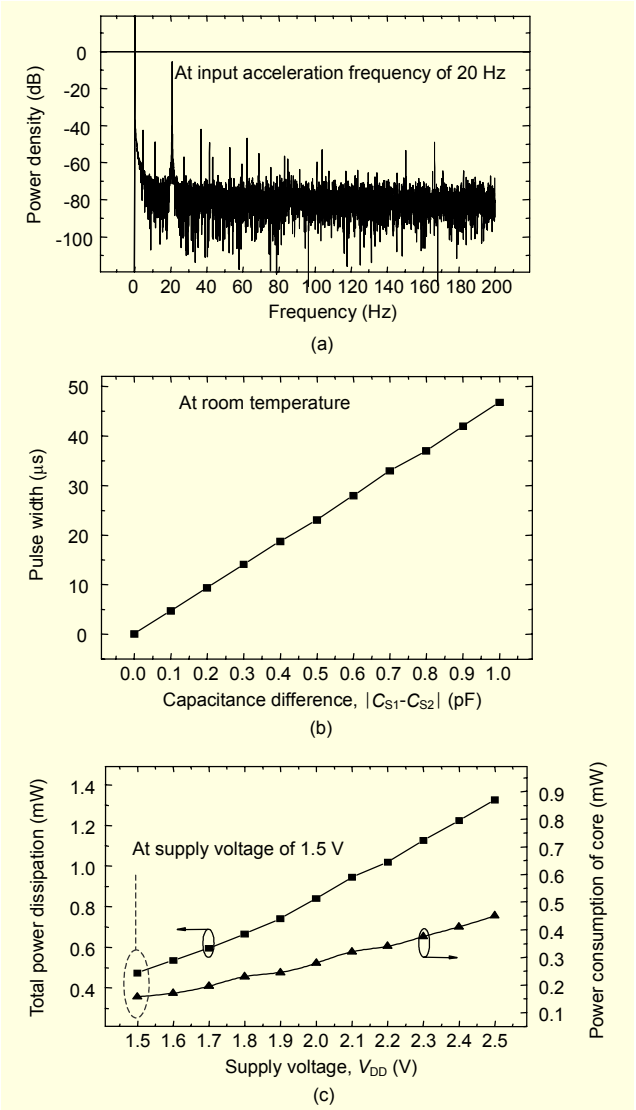

Fig. 9. Experimental results of the proposed IC for (a) power spectral density, (b) transfer characteristics for PW vs. capacitance difference, and (c) power dissipation measured at room temperature (300 K).

current was about 0.31 mA and the biasing current of the core circuit was about 0.1 mA, which is significantly reduced due to the low-voltage operation and small size of 0.16 mm^2. These results correspond to total power consumption and core-circuit power dissipations of 0.47 mW and 157 μW, respectively, which are mainly due to the low level of the bias current. The power consumption of the new interface circuit was significantly reduced by more than 40% compared to that of other interface circuits operating at the supply voltage of 1.5 V [18].

The major performance characteristics are summarized in Table 1. The summarized results indicate that the proposed interface circuit provides the desired low-voltage capacitance-to-pulse-width conversion based on the desired self-reset

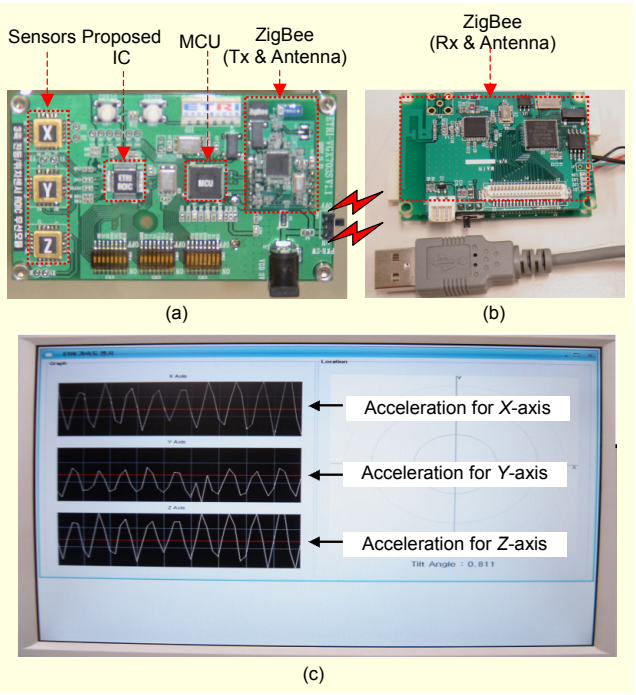

Fig. 10. Photos of the implemented (a) wireless sensor-node, (b) USB-type receiver module, and (c) acceleration monitoring screen.

Table 1. Performance summary and comparison.

Parameters		Value		
Technology		Chartered 0.35-μm CMOS logic process		
Chip size		2.8 mm × 2.8 mm		
Sensor rest-capacitance		3 pF		
Sensor sensitivity		0.2 pF/g		
Core size		0.16 mm^2		
IC sensitivity		42 μs/pF		
Sensor + IC sensitivity		8.4 μs/g		
Power density	Signal	-4.1 dB		
	Noise	-79.4 dB		
		This work	Ref. [17]	Ref. [18]
Supply voltage		1.5 V	3.3 V	1.5 V
Power consumption of the core circuit		157 μW	895 μW	270 μW

operation with sub-mW power consumption while operating at the low supply voltage of 1.5 V, which is relatively low power consumption compared to previously reported interface circuit structures [17], [18].

As shown in Fig. 10, the prototype wireless sensor module with the new interface circuit was implemented for 3-axis (*X*, *Y*, and *Z*) accelerometers, which is one of the wireless sensor

network applications [19], [20]. Figure 10(a) shows a photo of the implemented wireless sensor-node with a ZigBee transmitter. The ZigBee receiver for the wireless sensor-node is shown in Fig. 10(b), which has a USB-type port. The sensed data, obtained from the 3-axis acceleration sensors and interface circuit was transmitted to the ZigBee receiver. In the PCs of local users, the received data was plotted as signal-waveforms of the acceleration for 3 axes as shown in Fig. 10(c). Hence, this implemented sensor-node with the proposed IC chip is suitable for practical applications, such as structural health monitoring for buildings and bridges [21], [22].

IV. Conclusion

A low-power low-cost CMOS interface circuit based on standard 0.35 μm CMOS logic technology was proposed and demonstrated. At a low supply voltage of 1.5 V, the new interface-circuit provides a total power consumption of 0.47 mW. Moreover, the interface-circuit core shows the ultra-low power dissipation of 157 μW due to the desired capacitance-to-pulse-width conversion operation based on self-reset operation at a supply voltage of 1.5 V and the reduction of the circuit area. The results demonstrate that the new interface circuit with self-reset operation successfully reduces power consumption. The proposed CMOS interface circuit provides a low-power performance compatible with microsystems and capable of interfacing with a large variety of capacitive sensors. It is very promising for low-voltage sensor applications in ultra-low-power USNs.

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Sungsik Lee graduated from Korea Advanced Institute of Science and Technology (KAIST) in 2006 and is now with ETRI as a researcher in the research area of integrated circuit design for various sensors, such as capacitive and resistive sensors. He has been the first author of major SCI journal papers related to CMOS image sensors, published in journals such as *IEEE Electron Device Letters* and *IEEE Transactions on Electron Devices*. He has presented many international conference papers and holds many patents as the first author. His research interests include a novel and high performance interface circuit and system design for various physical sensors, including ubiquitous sensors in ubiquitous sensor networks.

Ahra Lee received the BS degree in electronic and electrical engineering from Kyungpook National University, Korea, in 2003. She completed an integrated MS/PhD course with the School of Electrical Engineering and Computer Science at Seoul National University in 2007. She is currently a PhD candidate with the Advanced Device Engineering division of the University of Science and Technology-ETRI. Her research interests include MEMS inertial sensors.

Chang-Han Je received the BS degree in mechanical engineering from Yonsei University, Seoul, Korea, in 2002, and the MS degree in mechanical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2004. Since 2004, he has been with ETRI, Daejeon, Korea, as a member of engineering staff, where he has been with the Microsystems Research Department. He is currently a PhD candidate with the Department of Mechanical Engineering at KAIST. His research interests include the design, fabrication, and characterization of MEMS devices and MEMS packaging.

Myung-Lae Lee received his BS degree in Physics from Dong-A University, Busan, Korea, in 1989, and his MS and PhD degrees in Physics from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1992 and 1998, respectively. Since 1998, he has been working for ETRI. His research interests include the design, fabrication, and characterization of MEMS devices with signal processing ICs for applications in the areas of optics, RF, and USN.

Gunn Hwang received the BS degree from Korea University, Seoul, Korea in 1983, and the MS and PhD degrees in mechanical engineering from Korea Advanced Institute of Science and Technology, Daejeon, in 1985 and 1999, respectively. He is a senior member of engineering staff with the Advanced I-MEMS Team of ETRI, Daejeon, Korea, where he has been employed for 22 years. His current work centers on developing MEMS devices, especially accelerometers with MEMS technology.

Chang-Auck Choi received his MS and PhD degrees in electronic engineering from Kyungpook National University, Taegu, Korea, in 1988 and 1999, respectively. Since 1980, he has worked for ETRI in the area of developing micro-electro-mechanical system (MEMS) devices and advanced semiconductor process technology. He is currently the project manager of MEMS sensor technology development. He is currently researching physical sensors and integrated MEMS sensors for ubiquitous sensor networks.